Generic Counter (Pulse Generator)

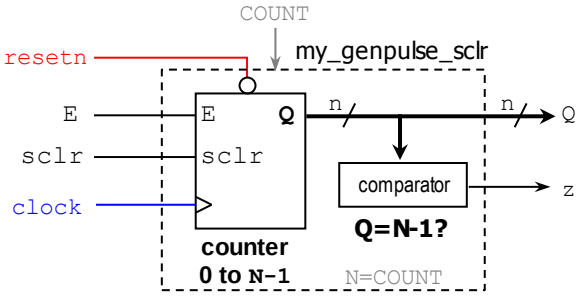
INTRODUCTION

- It is a common requirement to reduce the rate at which sequential digital circuits' transitions occur. This usually involves:
  - ✓ Reducing the rate of FSMs (Finite State Machines)
  - ✓ Reducing the rate or registers in a Datapath Circuit.
- A straightforward option is to reduce the frequency of the input clock. This can turn into a very complicated problem if a high precision clock is required.
- Alternatively, we can include an enable signal on every flip flop of our system (for both the FSM and the Datapath Circuit). Then, we assert the enable signal only when we need it. The effect is the same as reducing the frequency of the input clock.

GENERIC COUNTER CIRCUIT (my_genpulse_sclr.vhd)

- This counter (or pulse generator) has the following features:
  - ✓ It is a counter modulo-N (count: 0 to N-1). The number of bits of the counter is $n = \lceil \log_2 N \rceil$.
  - ✓ It has an n-bit comparator (Q = N-1?) that generates a one-cycle pulse z every time the counter hits the count N-1.
  - ✓ Operation:
    - User must setup the parameter COUNT = N.
    - If E = 1 then:

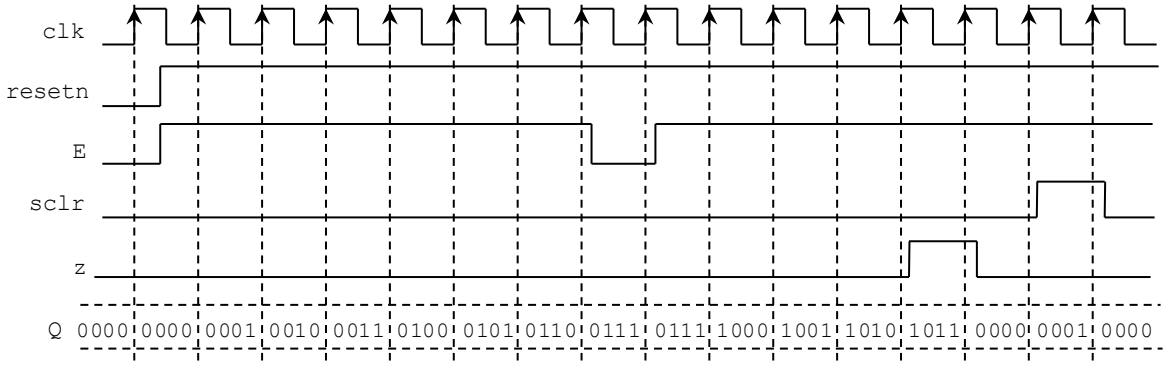
      if sclr = 1 then Q = 0, else Q ← Q+1.



- The output z can then be connected to every flip flop, counter, and register whose rate of operation we would like to modify. This way, we get the same effect at modifying the clock frequency to f/N, where f is the frequency of the input clock.

TIMING DIAGRAM (N=12)

- The figure shows the timing diagram of a counter from 0 to 11 (N=12). z is asserted when the count reaches 1011 (11). This z signal can then control the enable of any counter, register, or FSM whose rate of operation we would like to reduce by 12. This has the same effect as reducing the frequency by 12.



EXAMPLE

- **BCD counter**: we would like the 4-bit count to change every one second. However, the input clock is 100 MHz. We can use the pulse generator (my_genpulse_sclr) circuit that generates a one-clock period (10 ns) pulse every 1 second:
  - ✓ The COUNT parameter is given by: COUNT×10 ns = 1 s → COUNT = 10^8. This counter needs $n = \lceil \log_2 10^8 \rceil = 27$ bits.
  - ✓ E and sclr signals: They can be used to further control this pulse generator (usually E=1, sclr=1)