Embedded System Design for Zynq™ SoC

INSTRUCTOR	Daniel Llamocca
CONTACT INFO	email: llamocca@oakland.edu
WEBPAGE	www.secs.oakland.edu/~llamocca/EmbSysZynq.html
REFERENCES	▪ Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, "T*he Zynq Book Tutorials"*, Aug. 2015. ✓ Free download: http://www.zynqbook.com/
MATERIALS	ZYBO Z7-10 (or ZYBO) Zynq™-7000 Development Board Vivado™ Design Suite 2019.1 – Webpack Edition Xilinx Software Development Kit 2019.1
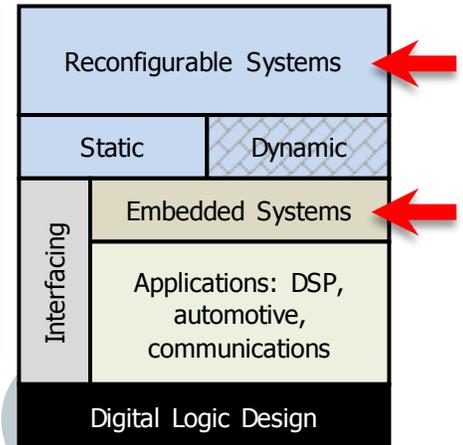
DESCRIPTION

▪ Embedded System Design with Vivado™ Design Suite software for Zynq™ System-on Chip. Software implementation with the Software Development Kit (SDK). Hardware/software co-design: creation of custom-defined VHDL IP cores, interfacing with the AXI bus, and creating software applications to control the VHDL IP cores.

OUTLINE OF TOPICS

Introduction to Vivado	▪ Hardware Design Flow: Design Entry, Functional Simulation, Mapping, Timing Simulation, Implementation ▪ Case example: Counter with enable controlled by a pulse generator ✓ I/O assignment: XDC file ✓ VHDL Testbench Generation and Testing
Introduction to Hardware/Software Design	▪ Using both the PL (Programmable Logic) and PS (Processing System). ▪ Vivado: Create a block-based project. Use of AXI GPIO peripheral to control LEDs ▪ SDK: Create a software application.
AXI4-Lite: Custom Peripheral	▪ Case examples: Pixel Processor, Pipelined Divider, Pipelined 2D Convolution Kernel ▪ Vivado: Create IP, AXI4-Lite interface. Create block-based project. ▪ SDK: Load custom drivers. Create software application and test with UART.
AXI4-Full: Custom Peripheral	▪ Case example: Pixel Processor, Pipelined Divider, Pipelined 2D Convolution Kernel ▪ Vivado: Create IP, AXI4-Full interface. Create block-based project. ▪ SDK: Load custom drivers. Create software application and test with UART.
	▪ Case example: DCT or Matrix multiplier (with a constant matrix) ▪ Vivado: Create IP, complex AXI4-Full interface. Create block-based project. ▪ SDK: Load custom drivers. Create software application and test with UART.
Using the SD Card (in PS)	▪ Software drivers ▪ Reading/writing binary and text files.
Dynamic Partial Reconfiguration (PL)	▪ Vivado Design Flow using TCL scripts. ▪ Case example: LED Pattern controller: 1 RPs and 2 RPs ▪ Testing with JTAG interface.
Dynamic Partial Reconfiguration (PL+PS)	▪ Vivado Design Flow using TCL script for PS+PL ▪ Case examples: Pixel Processor, DCT 2D. ▪ SDK: Write partial bitstreams using the PCAP port.
Using DMA	▪ Memory to memory transfers, Memory to PL transfers. ▪ Using interrupts to signal DMA Transfer completion.
Using Interrupts	▪ Case example: Pixel Processor with interrupt outputs. ▪ Vivado: Create IP, AXI4-Full interface with interrupt. Create block-based project and connect interrupt signals to PS. ▪ SDK: Create software application to enable, assert, and de-assert PL interrupts.