Adaptive Wiring Panels using Cell-based Architectures: A First Approach

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Outline

- Introduction.
- Conceptual Architecture.
- Existing Technologies & Previous Efforts.
- Implementation of Adaptive Wiring Panel.
- Example of connecting the cells.
- Prototype 1 pictures (and video).
- Conclusions and Future Planned Work.

Introduction

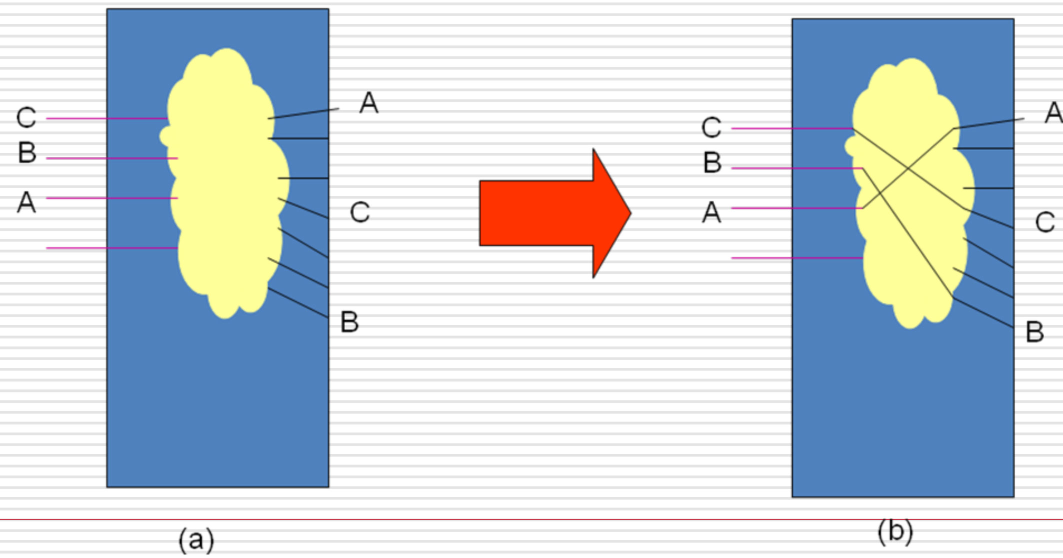
- Programmable wiring harness is being built.
- Soft-configured at the time of use.
- Useful properties
  - Self-healing
  - Error diagnostics capabilities
- Software-defined probe signals facilitate the high level instructions of configuring the soft-wires and connections.
- Modules connected to cells through a defined but flexible interface.

Introduction (cont'd)

- Reconfigurable switch fabric enables dynamic routing of signals in many possible applications:
  - Power
  - Digital Signals
  - Analog Signals
  - High frequency transmissions
  - RF
- Applications ranging from space to terrestrial.
- Particularly useful for time sensitive development schedules.

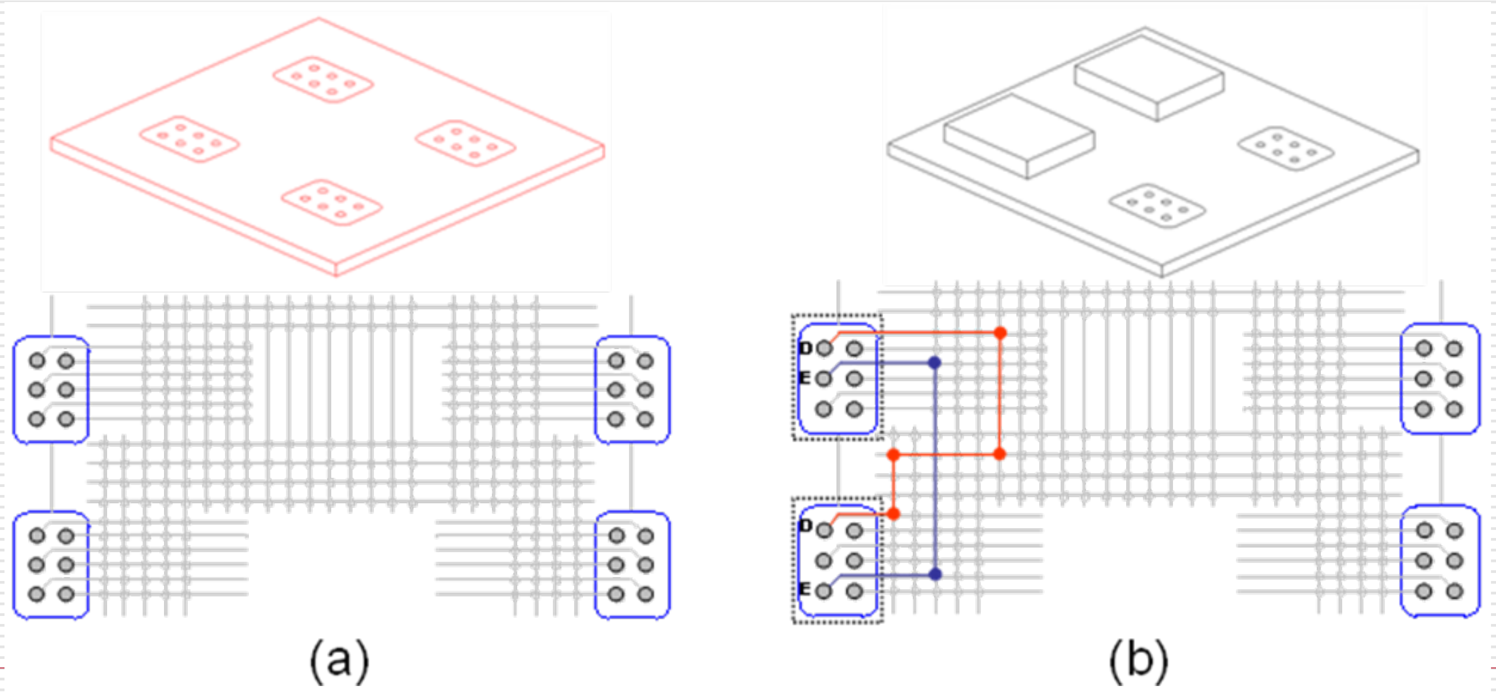
Conceptual Architecture

- Basic idea is of adaptive wiring structure as substrate
  - Contains input and output termini.
  - Refer to termini as wiring "problem" to connect termini together based on **rule set** – similar to netlist.



Conceptual Architecture (cont'd)

- Notional Implementation
  - "Cloud" substrate is now physical panel with wire matrix and switches.

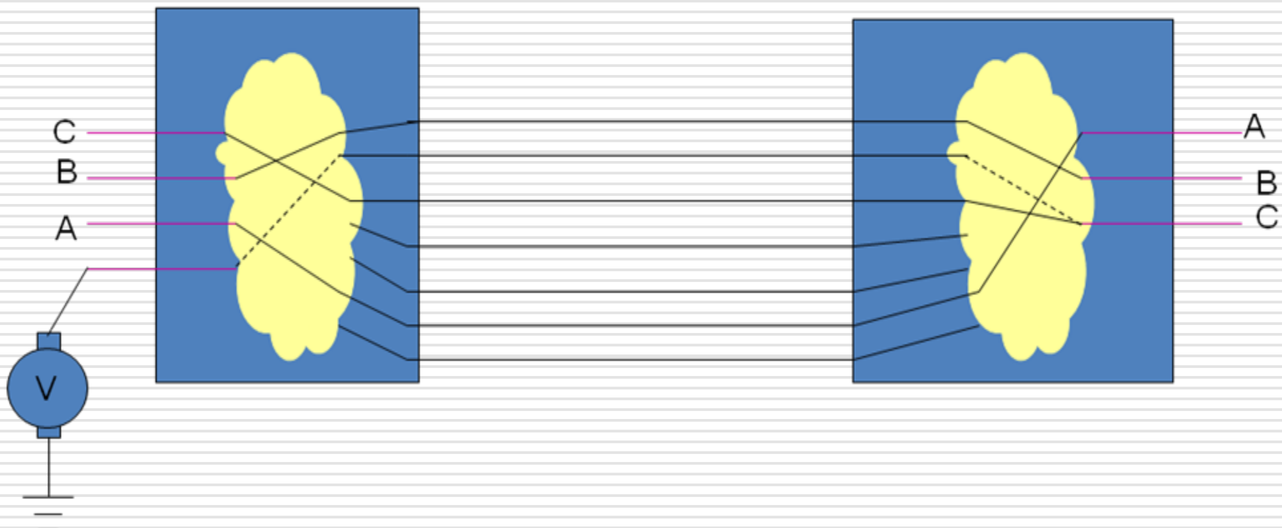


Conceptual Architecture (cont'd)

- Benefits of Adaptive Wiring
  - Wiring panels can be pre-built and inventoried.
  - Panel can be modified as needed during build.
- Unique Advantages
  - Adaptation to Faults – Circumlocution of Defects.

Conceptual Architecture (cont'd)

- Benefits of Adaptive Wiring
- Unique Advantages
  - Ability to create probe connections, thus we can create "self-healing" system
    - Diagnostic self-healing
    - Restorative self-healing
    - O(n) computation time



Existing Technologies

- Changes late in design cycle are costly.
- Changes while deployed are often impossible.

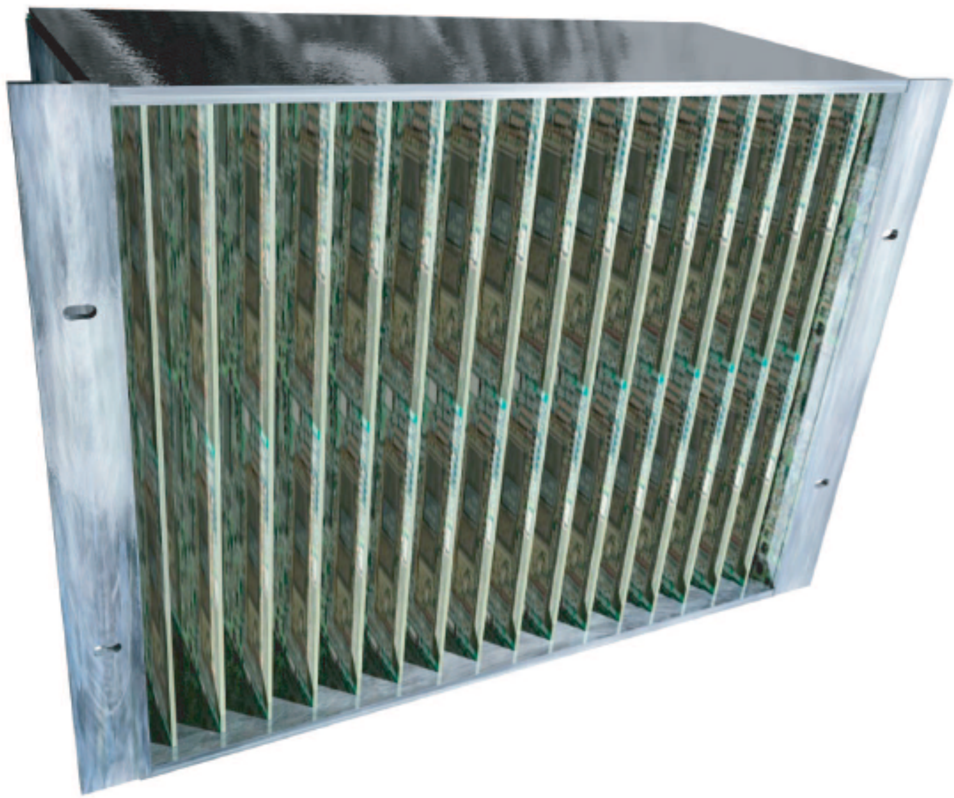
Existing Technologies (cont'd)

Traditional Wiring Harness Implementations

- Fixed Wiring Architecture – Automotive, Industrial, Aerospace
- Physical Cable Bundles

Existing Technologies (cont'd)

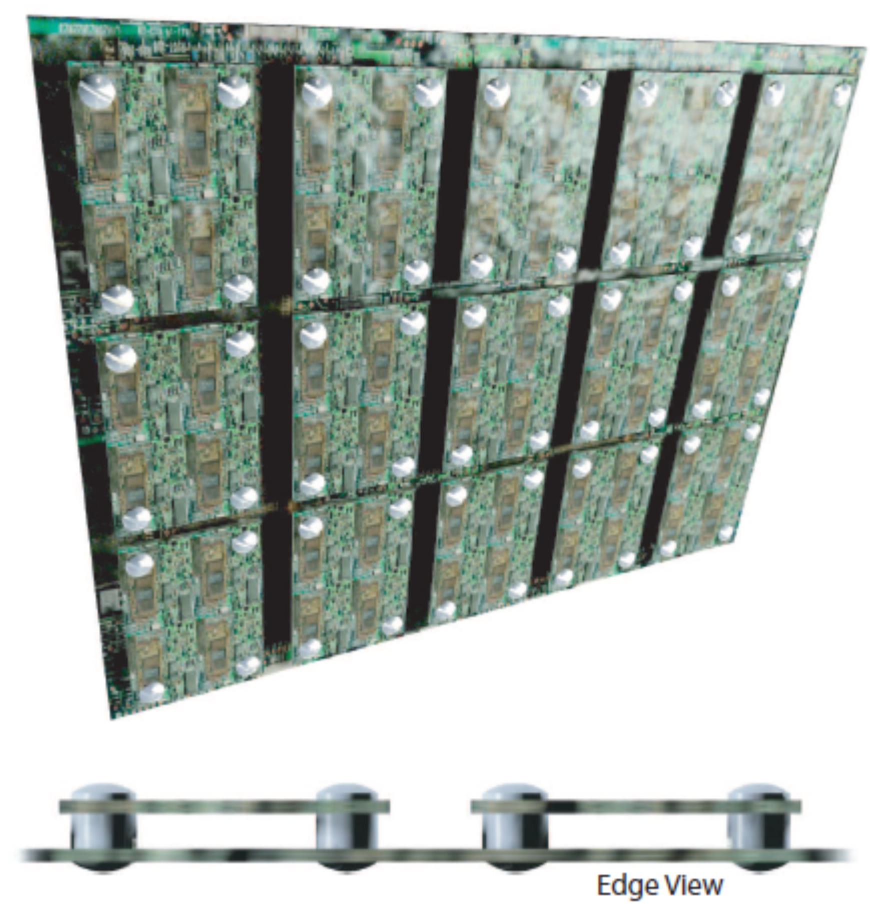
- Wiring Harnesses in Space: Card frame with passive backplane



Images from: Sarah Thompson and Alan Mycroft, "Reconfigurable Manifolds," Final Report, 2006.
[Online] http://www.dtic.mil/cgi-bin/GetTRDoc?Location=U2&doc=GetTRDoc.pdf&AD=ADA463036

Existing Technologies (cont'd)

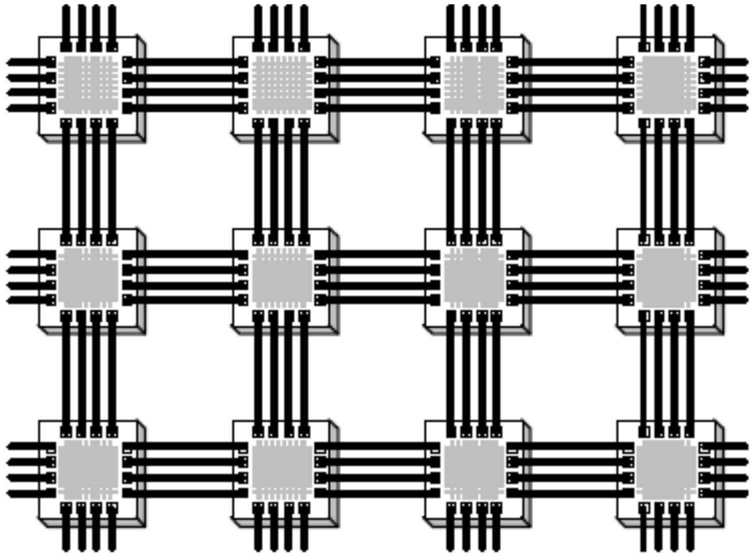
- Wiring Harnesses in Space: Motherboard/Daughterboard

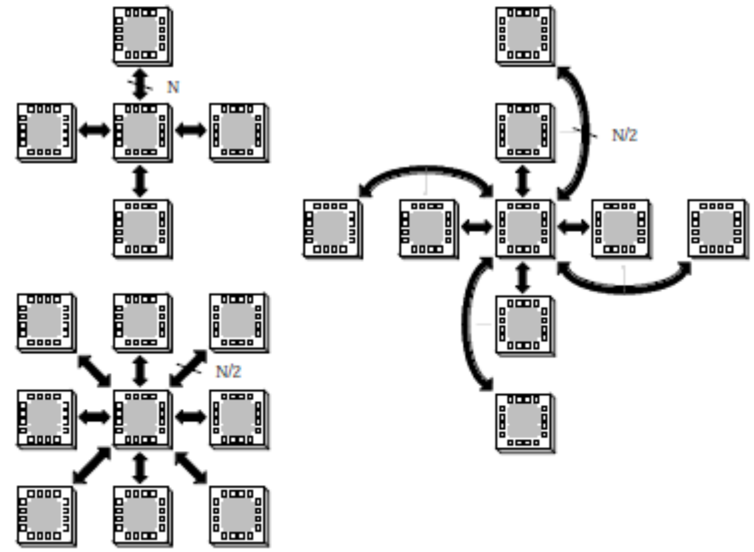


Images from: Sarah Thompson and Alan Mycroft, "Reconfigurable Manifolds," Final Report, 2006. [Online] http://www.dtic.mil/cgi-bin/GetTRDoc?Location=U2&doc=GetTRDoc.pdf&AD=ADA463036

Review of previous work in Reconfigurable Wiring

- S. Hauck – Mesh Topology
  - Connection schemes with grid-like array of FPGAs.
  - Studied speedup for purposes of logic emulation.





Images from: Hauck, S.; Borriello, G.; Ebeling, C.; , "Mesh routing topologies for multi-FPGA systems," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.6, no.3, pp.400-408, Sep 1998

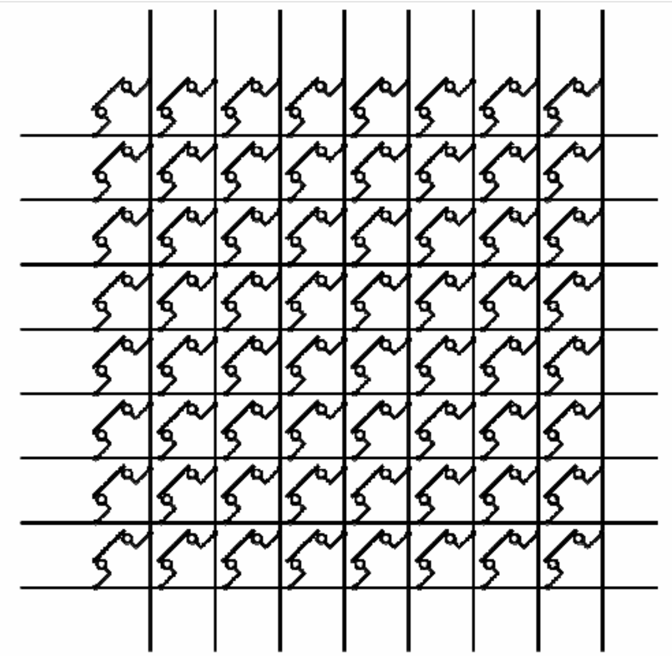
Review of previous work in Reconfigurable Wiring (cont'd)

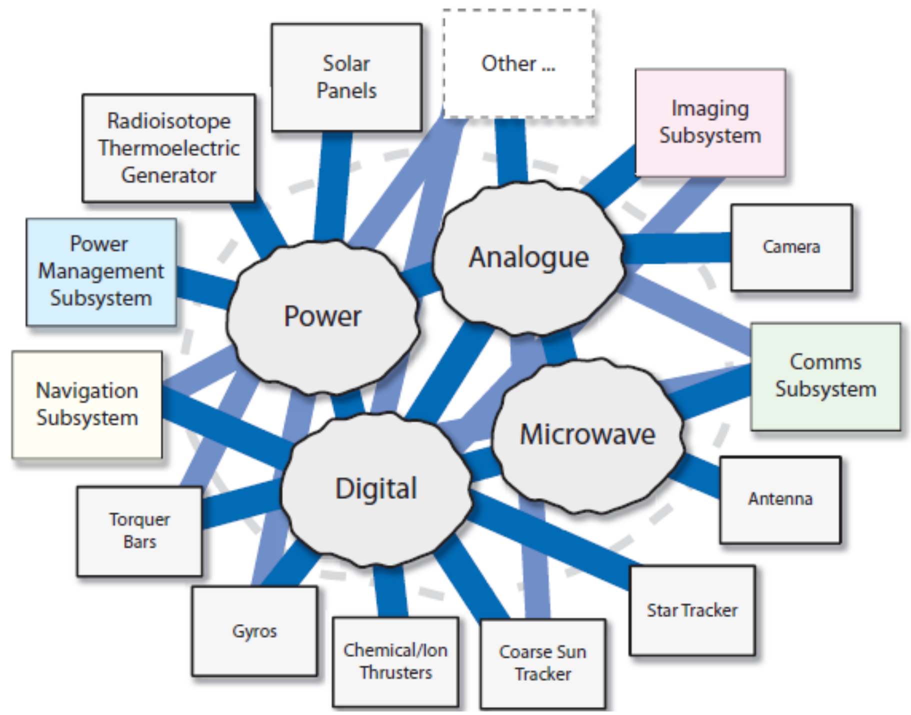
- A. DeHon
  - Trade-offs between computational elements, interconnect count, and bandwidth.
  - Interconnects dominate area.

- All studies with FPGA-based grids focus on logic emulation and system speedup – NOT analog (or non-digital media) routing.

Review of previous work in Reconfigurable Wiring (cont'd)

- S. Thompson
  - Significant work in Adaptive wiring.
  - Advances crossbar concept for other types of signals.
  - Fault tolerance.





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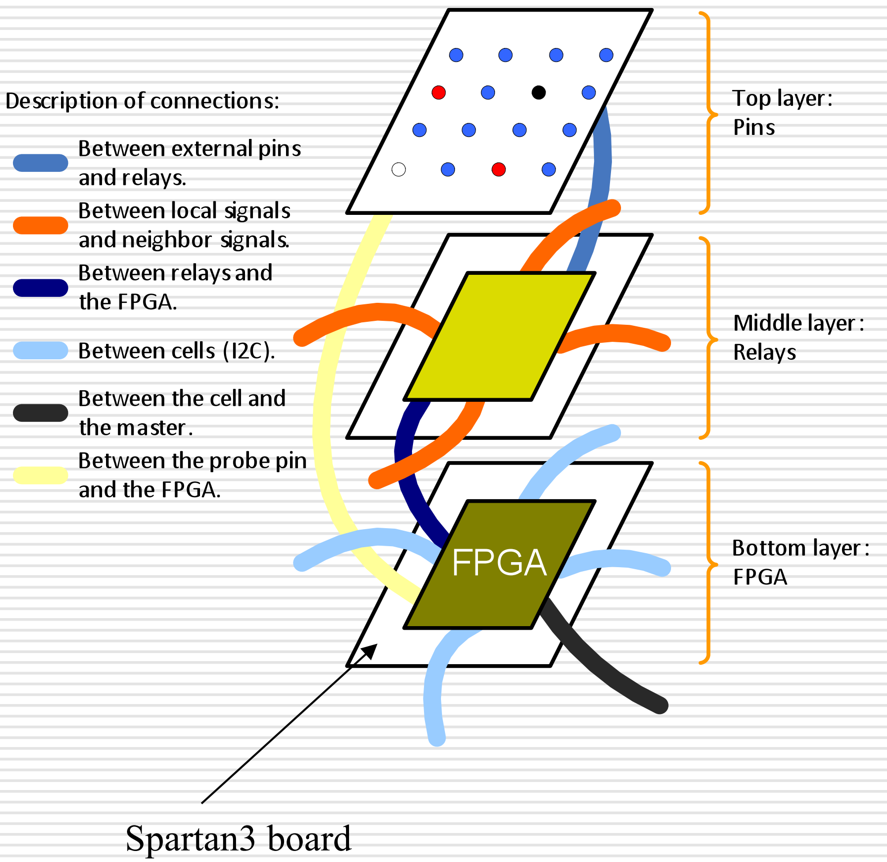
Scalable Cellular Implementation of the AWP

- Adaptive Wiring Panel (AWP) can be cast as a single overall panel.
- Three components:
  - Cell Units
  - Cell Management Unit (or, Master Controller)
  - Modules

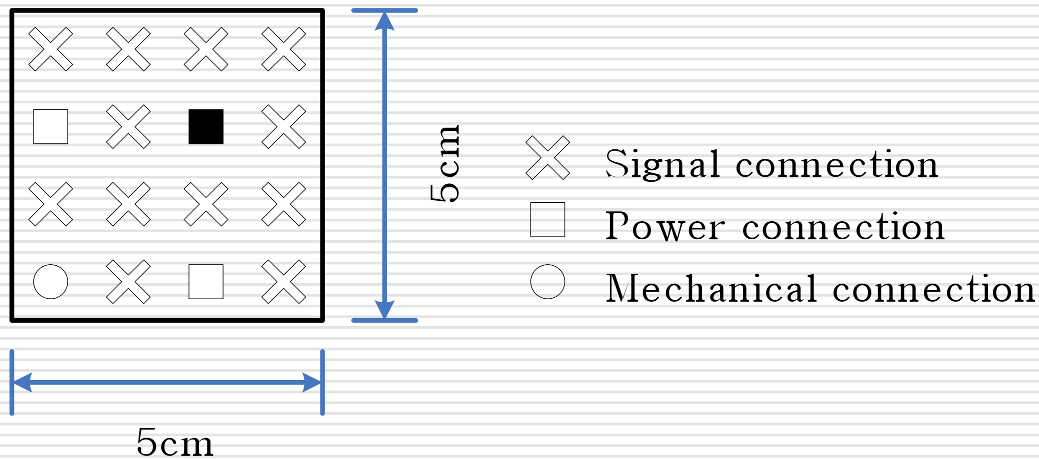
Scalable Cellular Implementation of the AWP

- Control Programmable Connections (i.e., switch states).
- Communicate with up to four neighbors.
- Read netlist information from modules via probe pins.
- Power modules.
- Communications with Cell Management Unit (CMU).

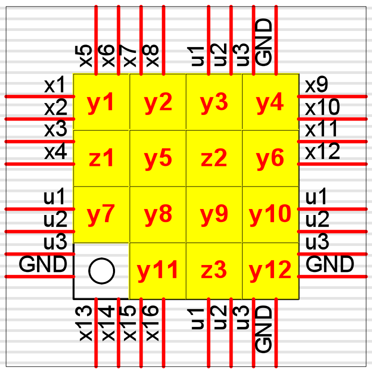


Cell Unit

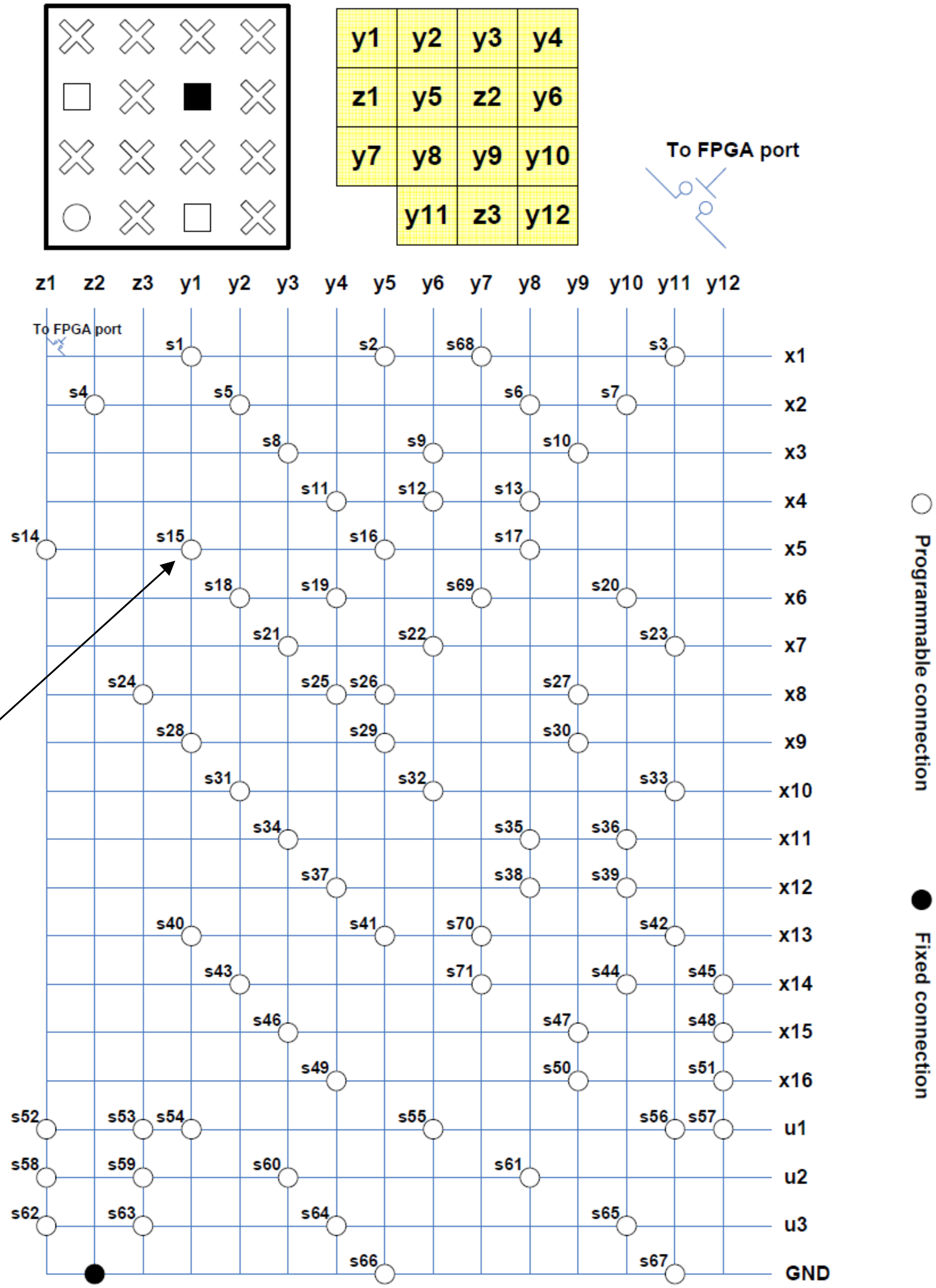
- Minimum independent unit to create AWP.
- Top view:



Cell Unit Switch Positions relative to I/O

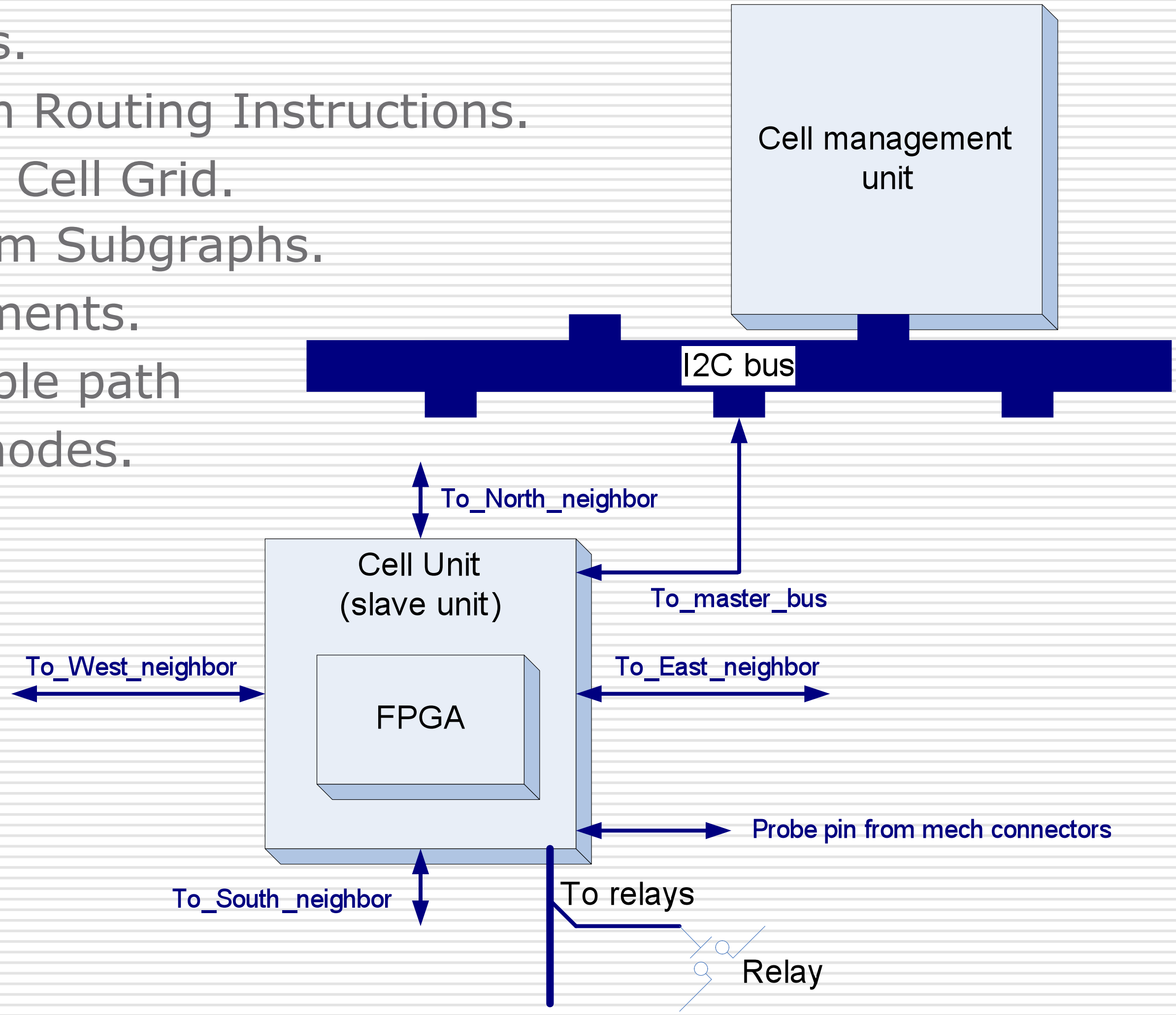


PhotoMOS Relay



Cell Management Unit

-Manages Communications.
-Commands Cell Units with Routing Instructions.
-Assembles and Organizes Cell Grid.
-Creates Master Graph from Subgraphs.
-Interprets netlist requirements.
-Calculates Shortest Feasible path between connection nodes.

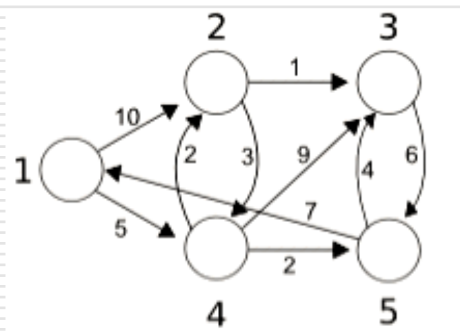


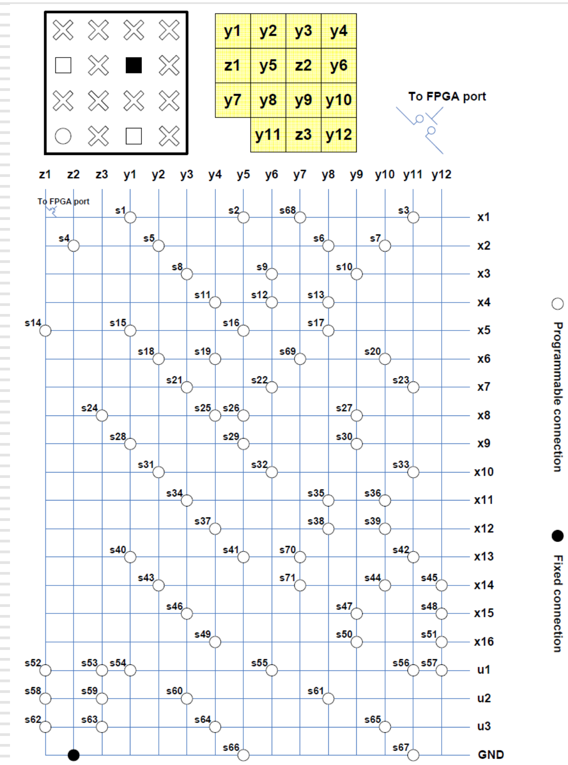
CMU Communication: Example Encodings

Address						
Decimal	Hexadecimal	Binary	Command	Type	Data	Notes
0	00	00000000				First available command address.
68	44	01000100	Read Cell ID	II	Cell ID	
69	45	01000101	Read North Neighbor ID	II	North ID	
70	46	01000110	Read East Neighbor ID	II	East ID	
71	47	01000111	Read South Neighbor ID	II	South ID	
72	48	01001000	Read West Neighbor ID	II	West ID	
73	49	01001001	Read Module ID byte	II	Module ID	
90	5A	01011010	Write relay	I	Open/Close relay	Bits(7 to 1): number of relay. Bit(0) is '0' when open and '1' otherwise.
91	5B	01011011	Read relay status	IV	Relay number	Write command, write relay number, read status
94	5E	01011110	Read datasheet	III	Datasheet	Number of bytes, datasheet
255	FF	11111111				Last available command address.

Cell Management Unit: Dijkstra’s Algorithm

- Calculates Minimum Shortest Path for Weighted, Directed Graph.
- Speed varies from $O(n \lg(n))$ to $O(n^2)$.
- Graph Theory Nodes = Wires in AWP.
- Graph Theory Paths = Switches in AWP.

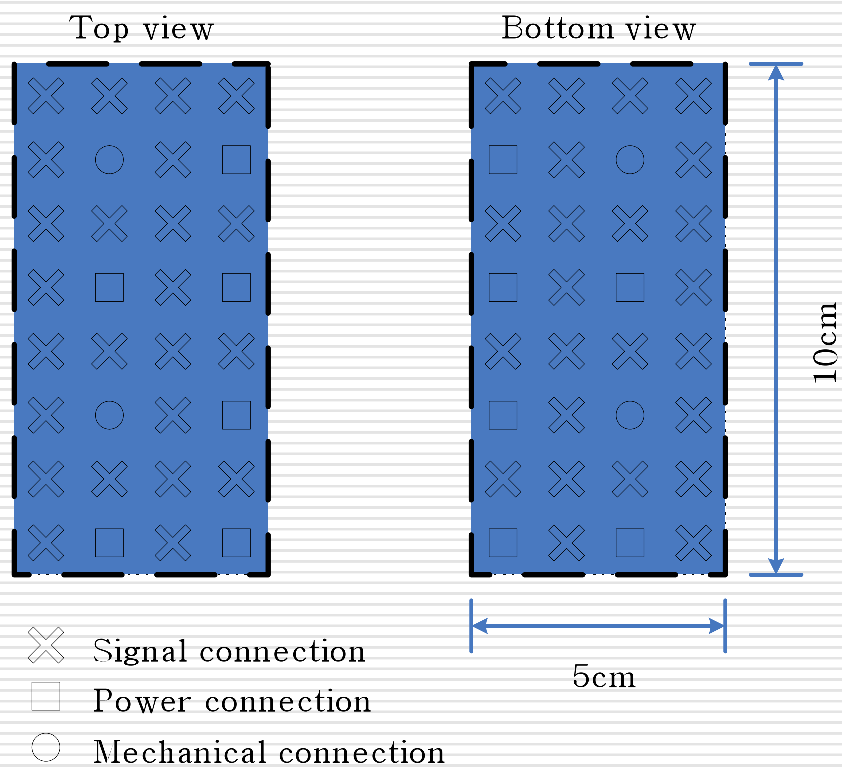


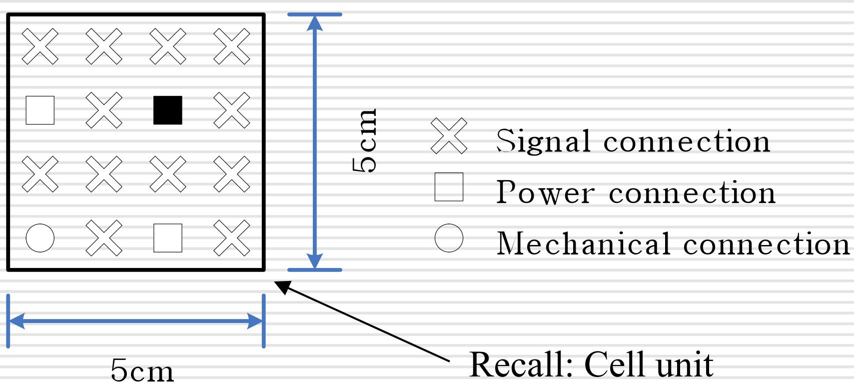


Left Image from: Gregory Feucht, “Design and control of a cellular architecture-based adaptive wiring manifold,” Master Thesis, University of New Mexico, 2010.

Modules

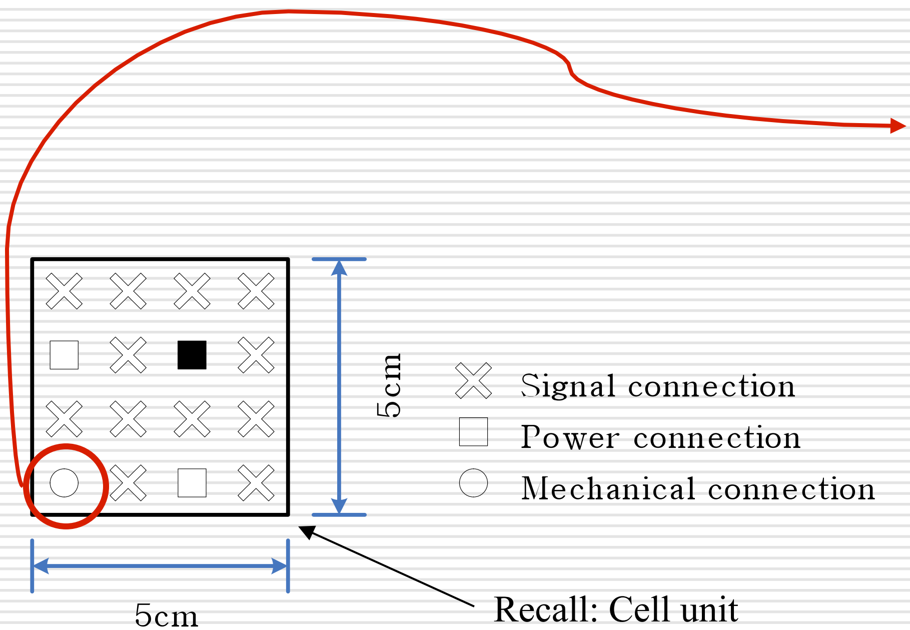
- Components to be Wired.
- Traversal over (at least) two cells and mechanical mount points.

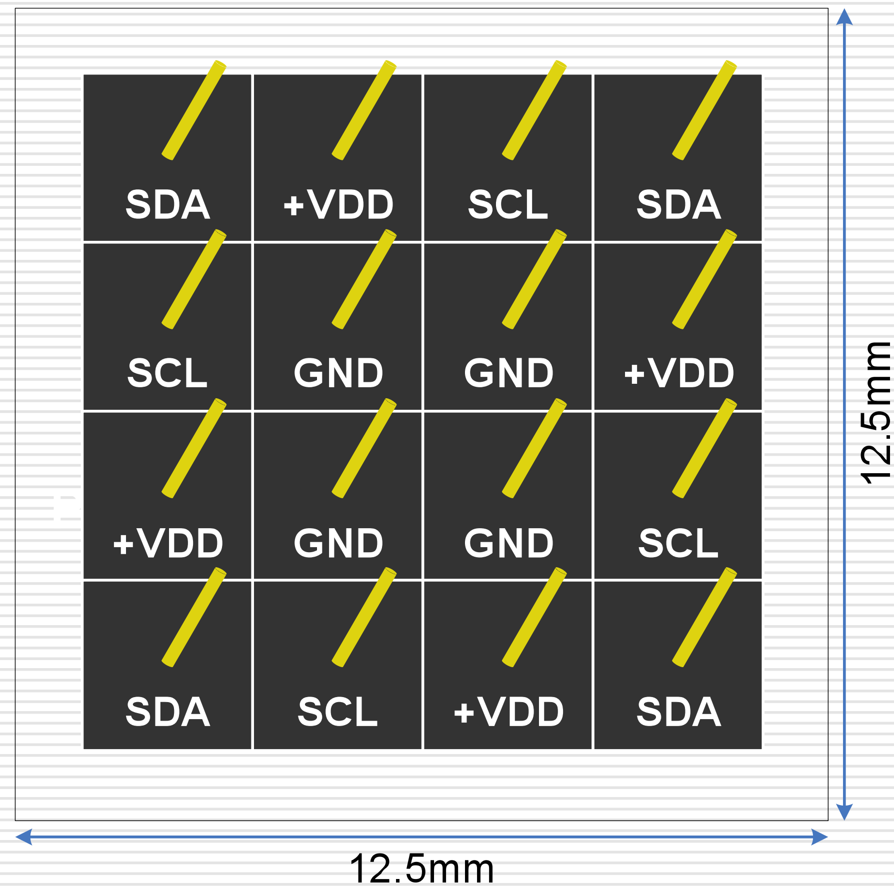




Module Probing Connector

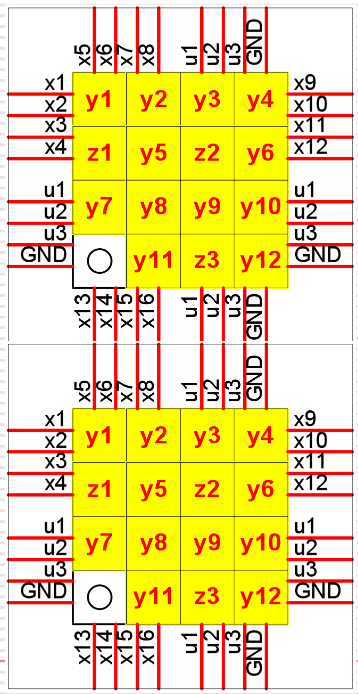
- Redundant pins allow for modules to be plugged in with any 90 degree rotation of device.

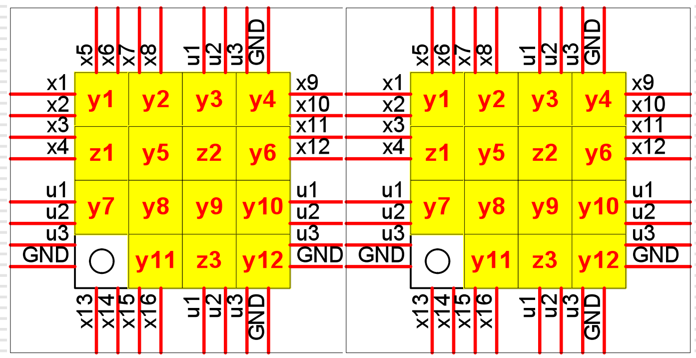




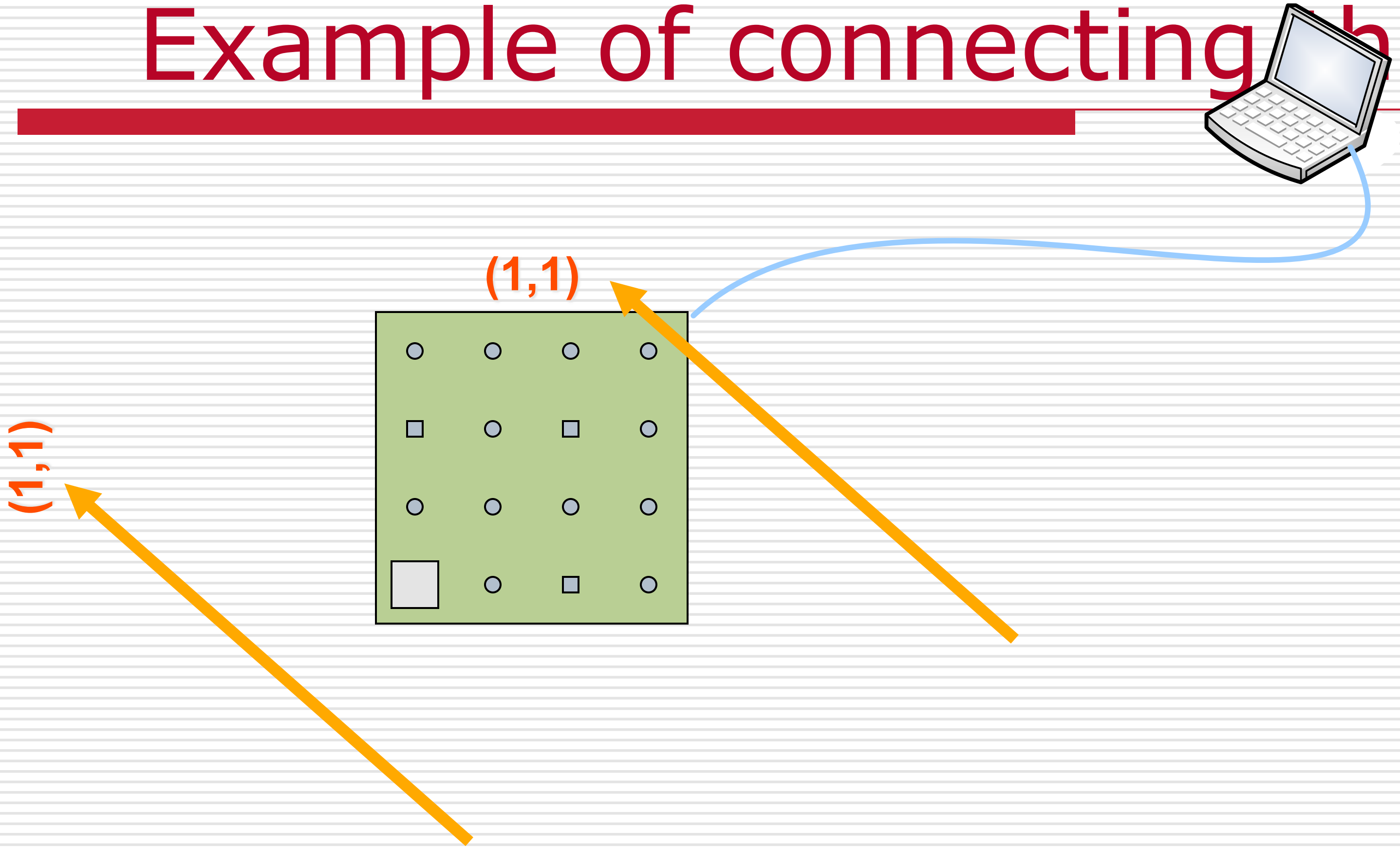
Cell Grid Assembly

- Protocol is breadth first search.
- Finishes with both all neighbors have been checked for other neighbors, and all identified cells added.
- Subgraph joining depends on orientation.



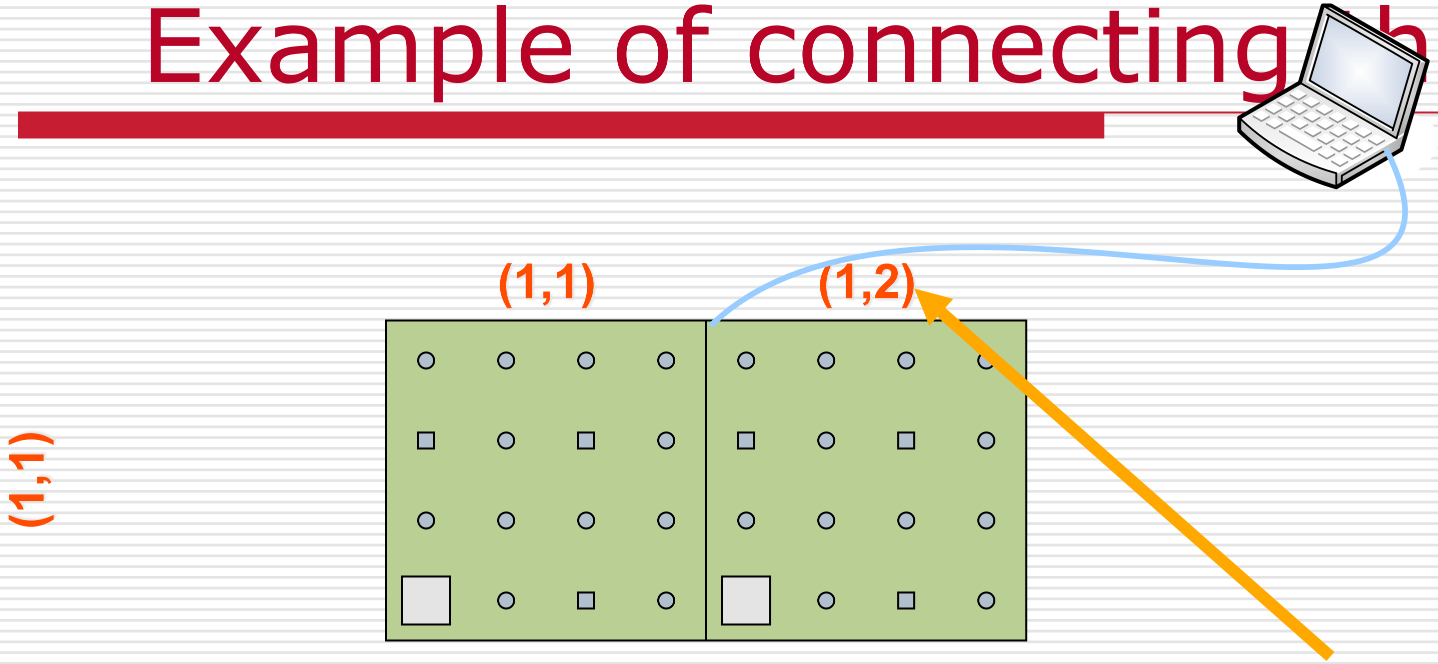


Example of connecting the cells



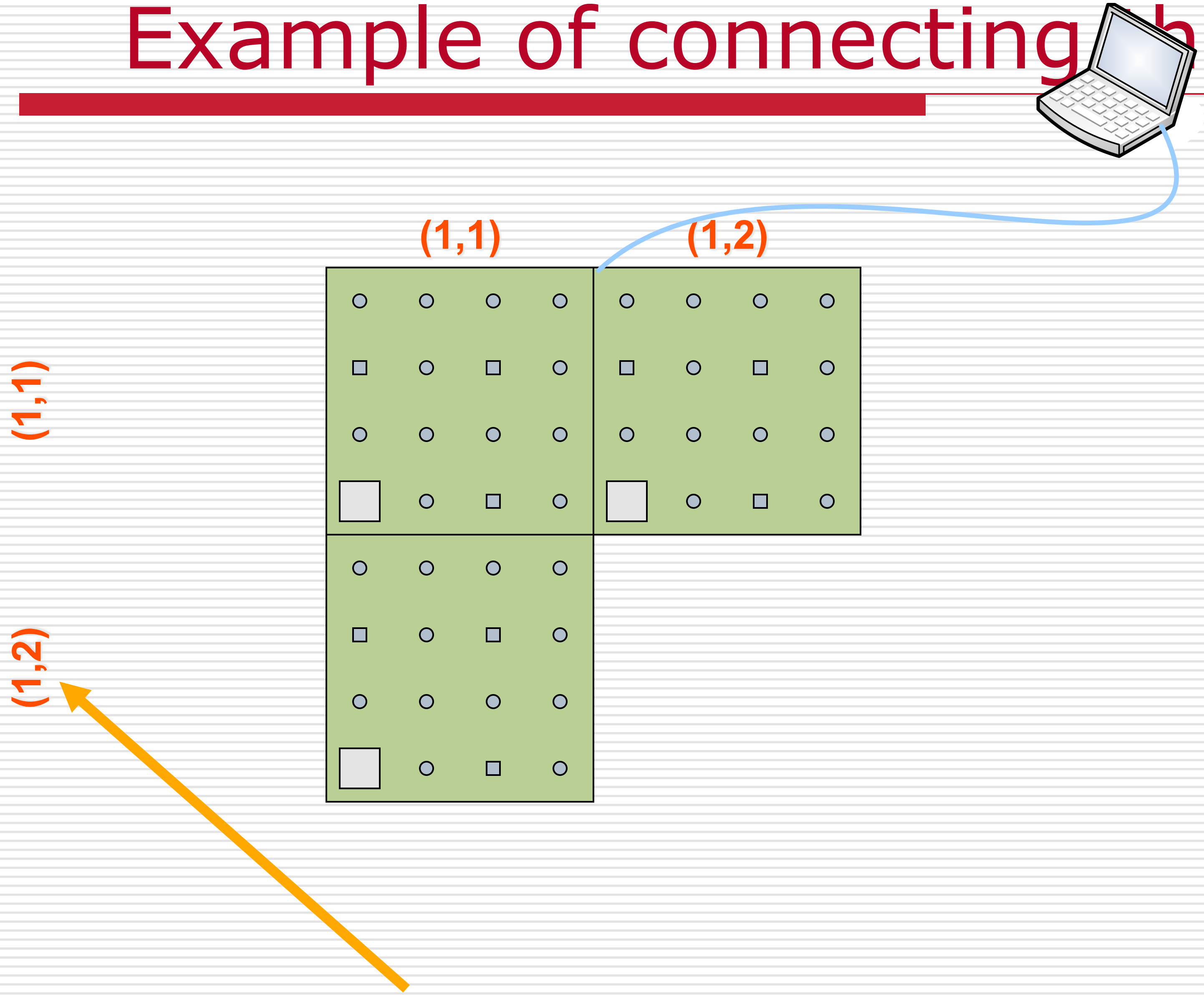
AWP: 1 cell

Example of connecting the cells



AWP: 2 cells

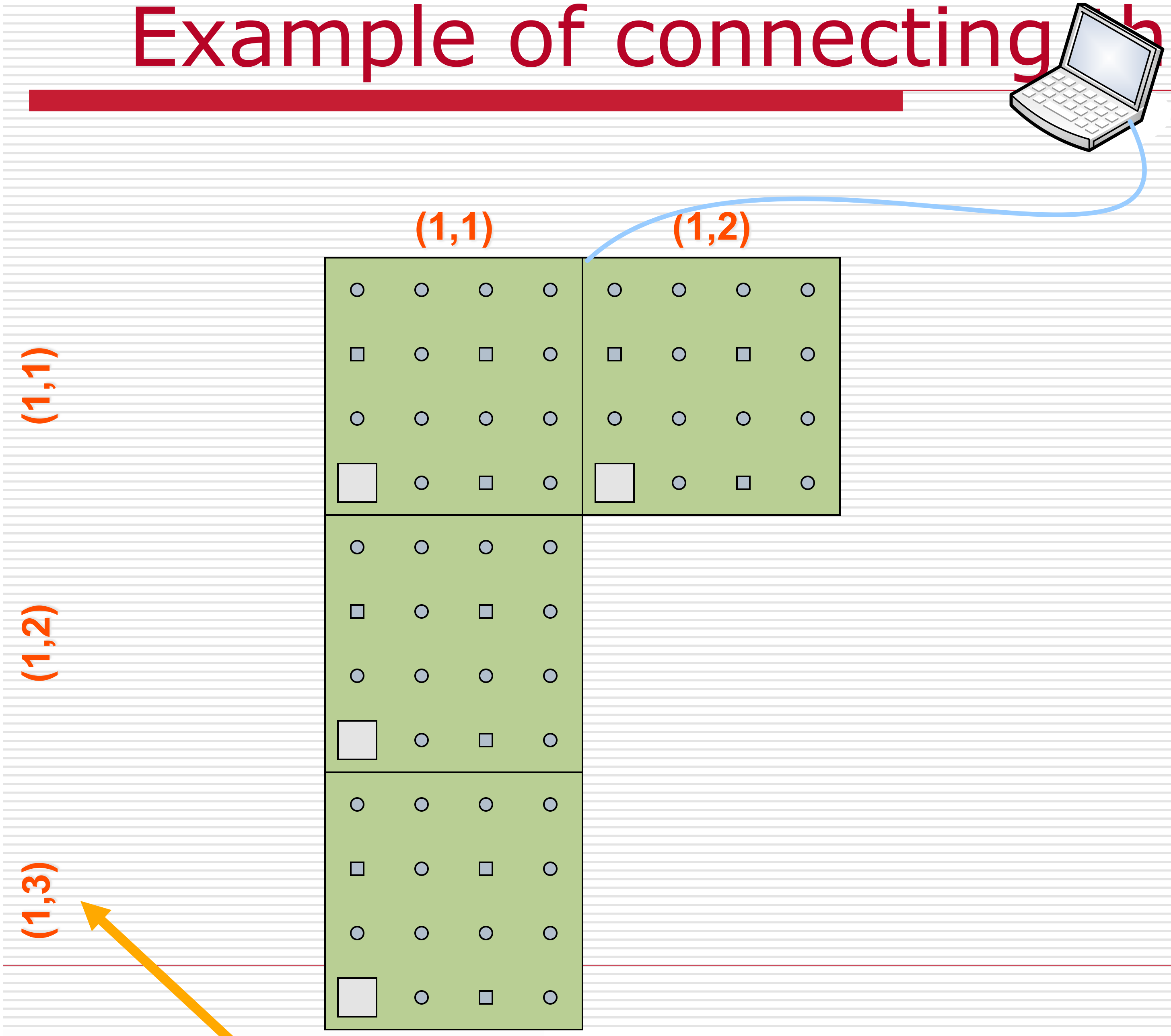
Example of connecting the cells



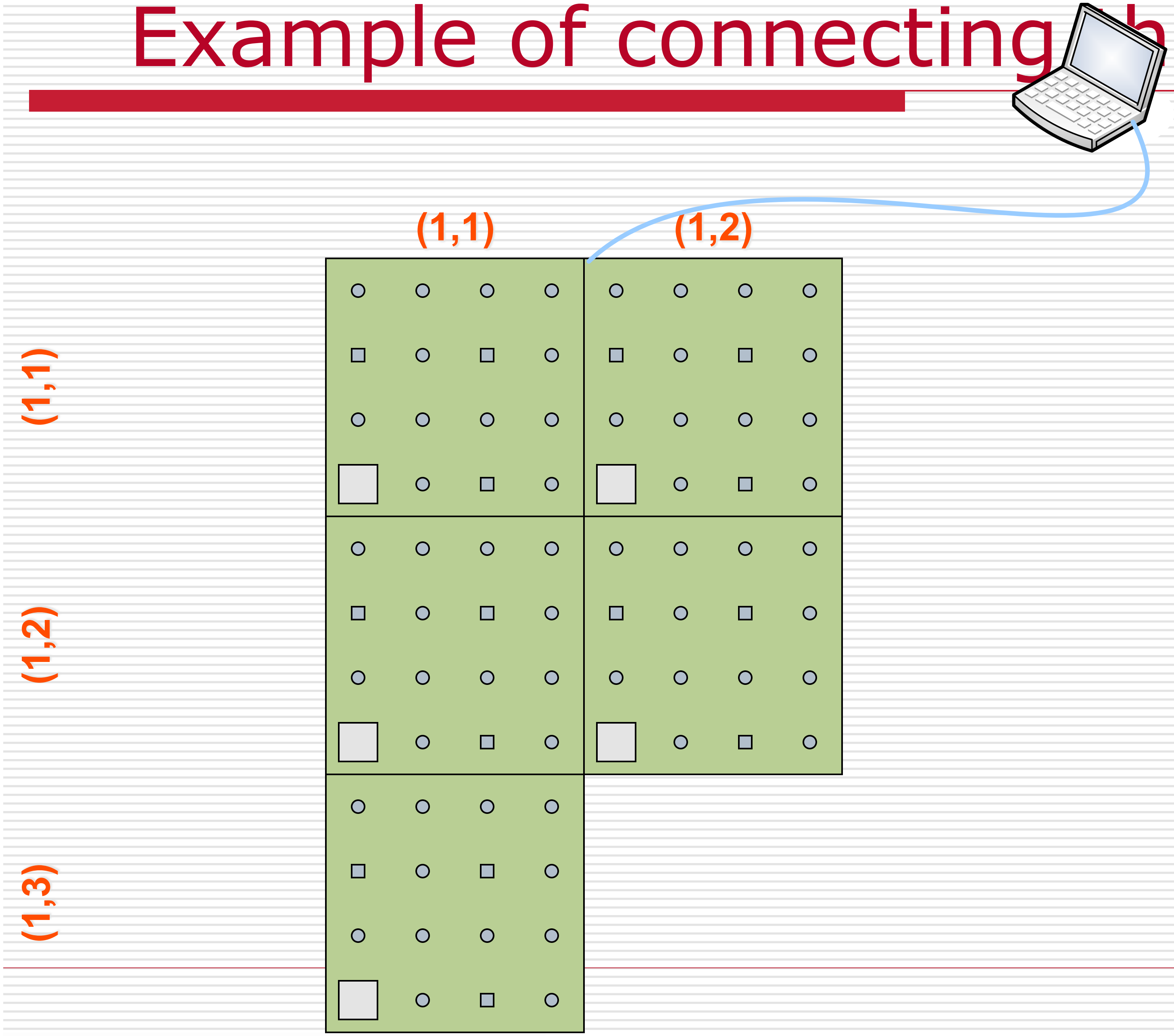
AWP: 3 cells

Example of connecting the cells

AWP: 4 cells

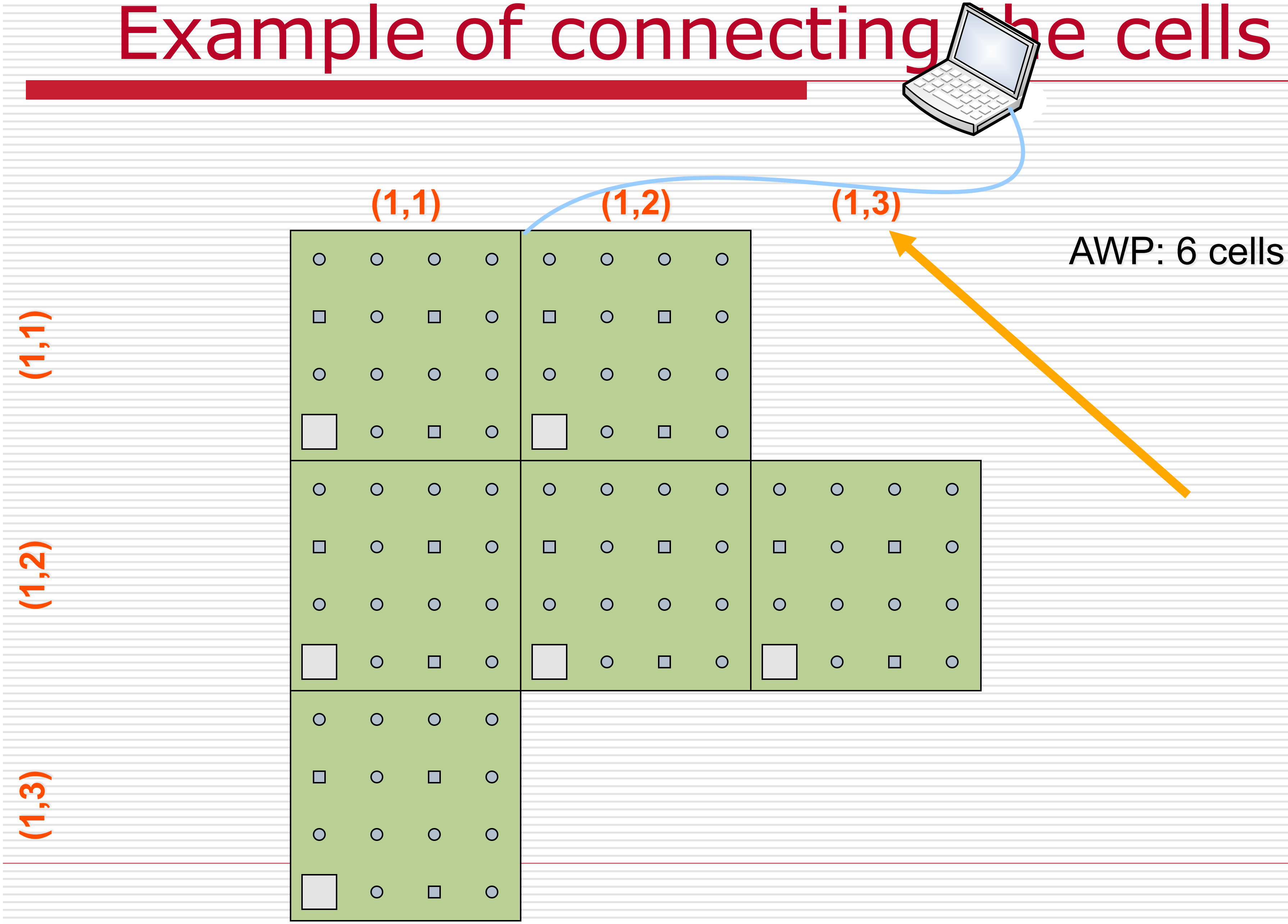


Example of connecting the cells

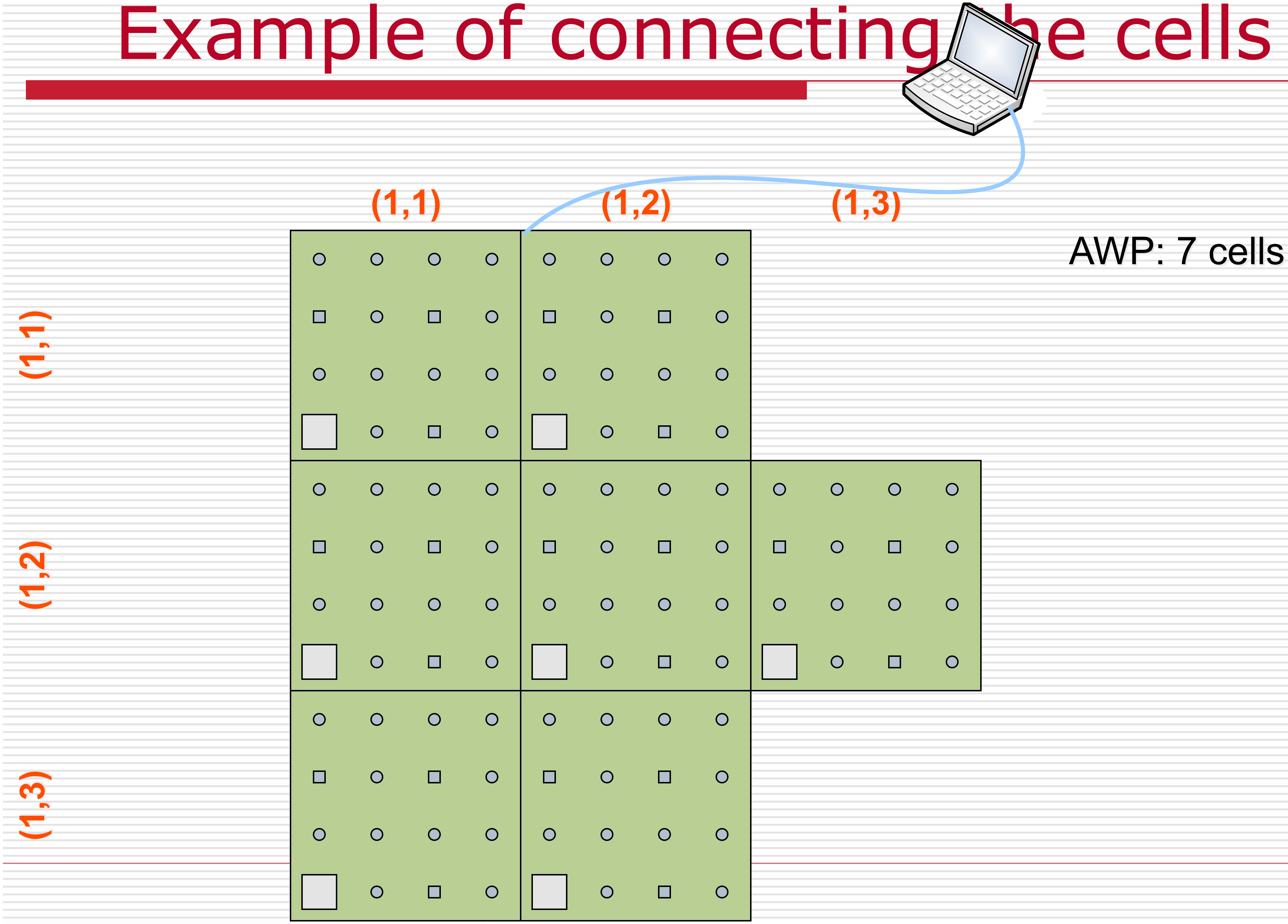


AWP: 5 cells

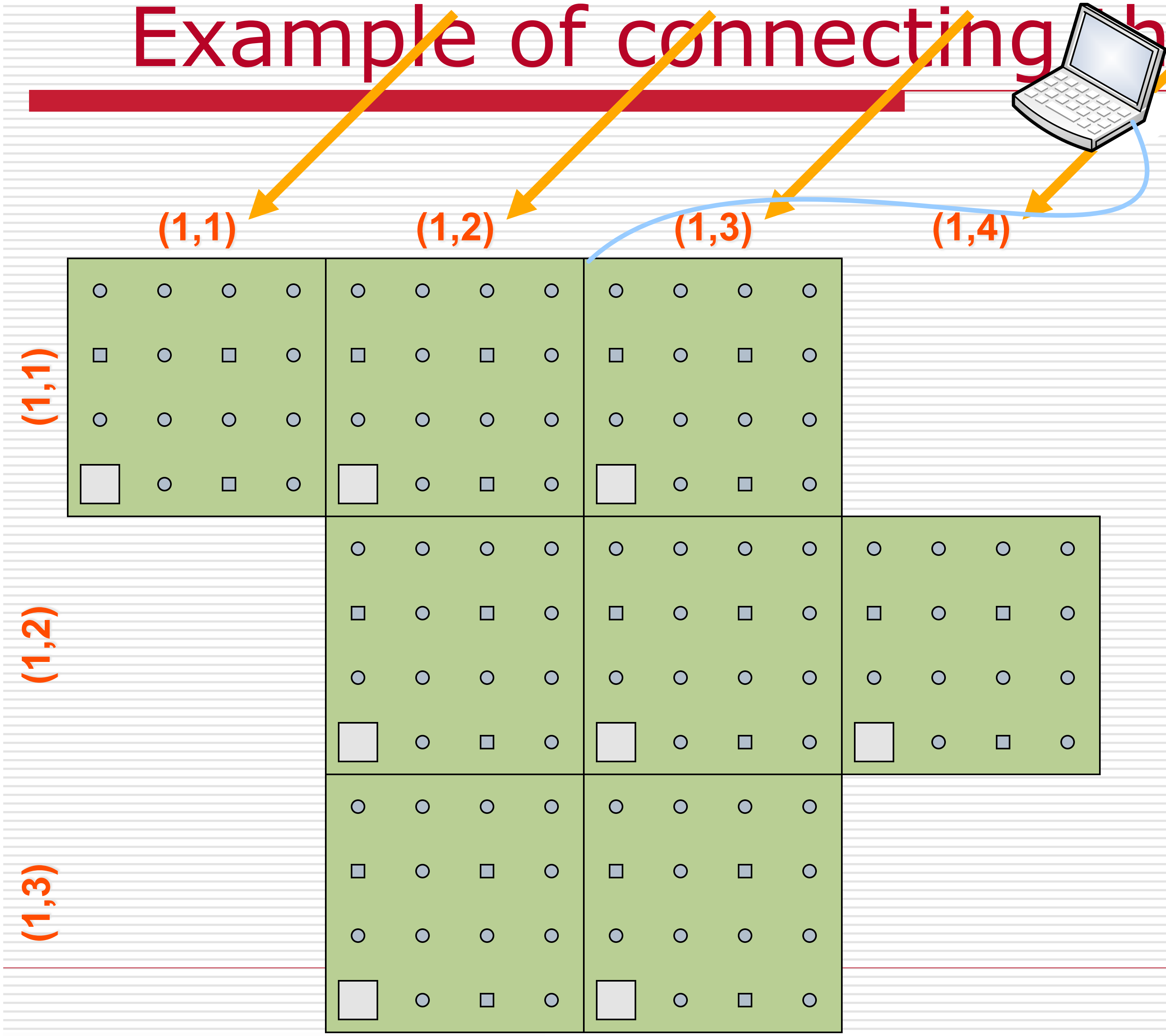
Example of connecting the cells



Example of connecting the cells

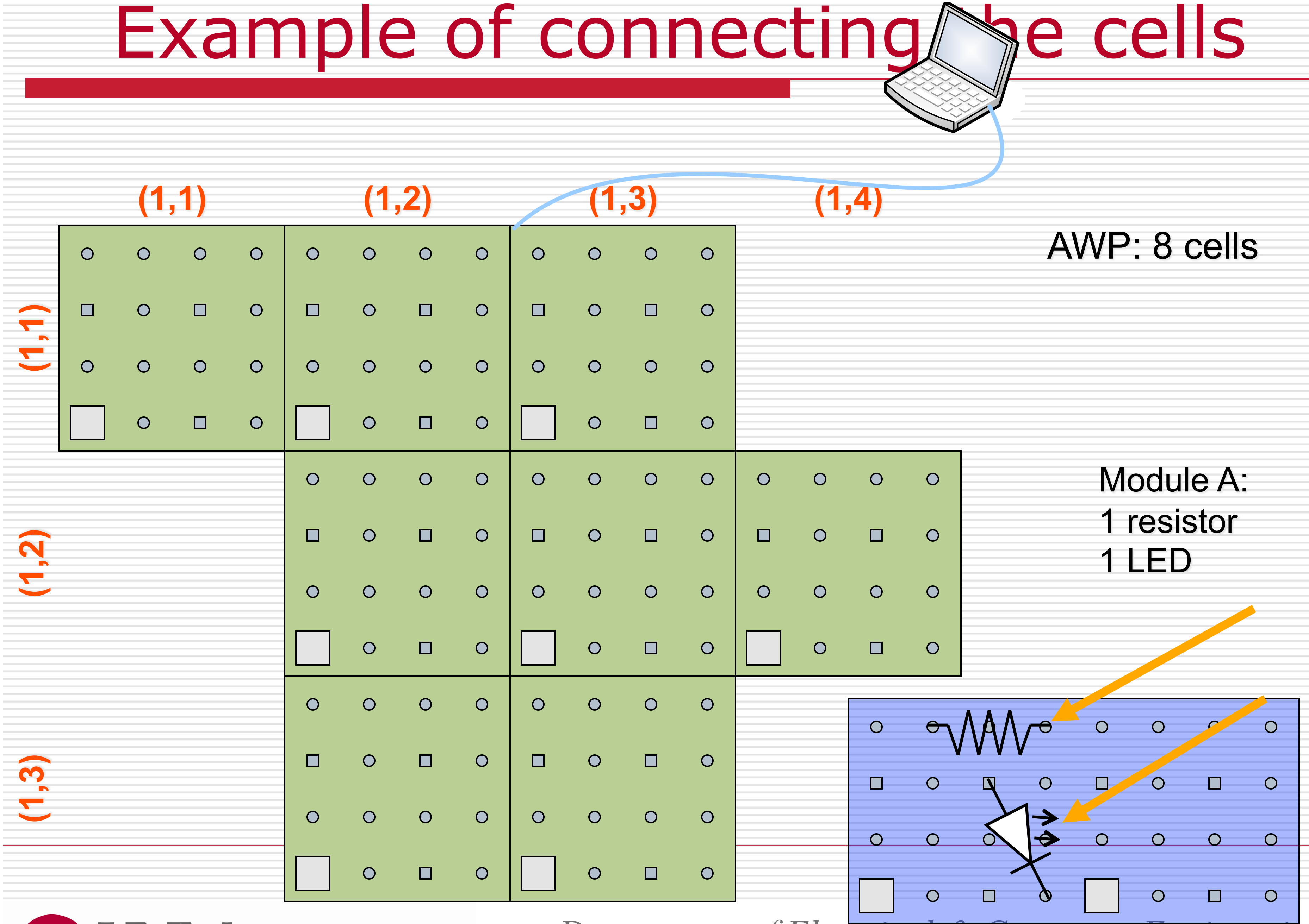


Example of connecting the cells



AWP: 8 cells

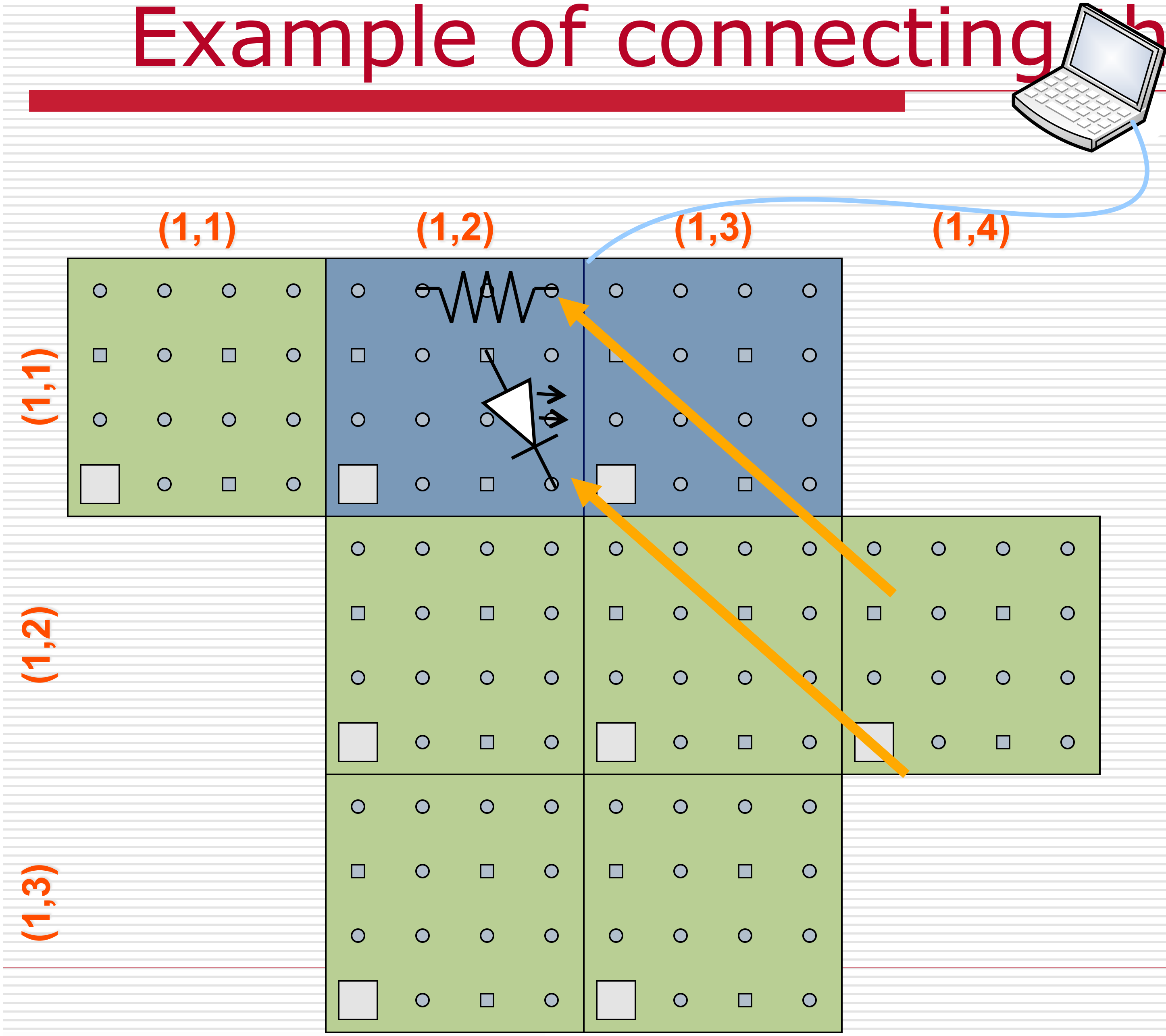
Example of connecting the cells



AWP: 8 cells

Module A:
1 resistor
1 LED

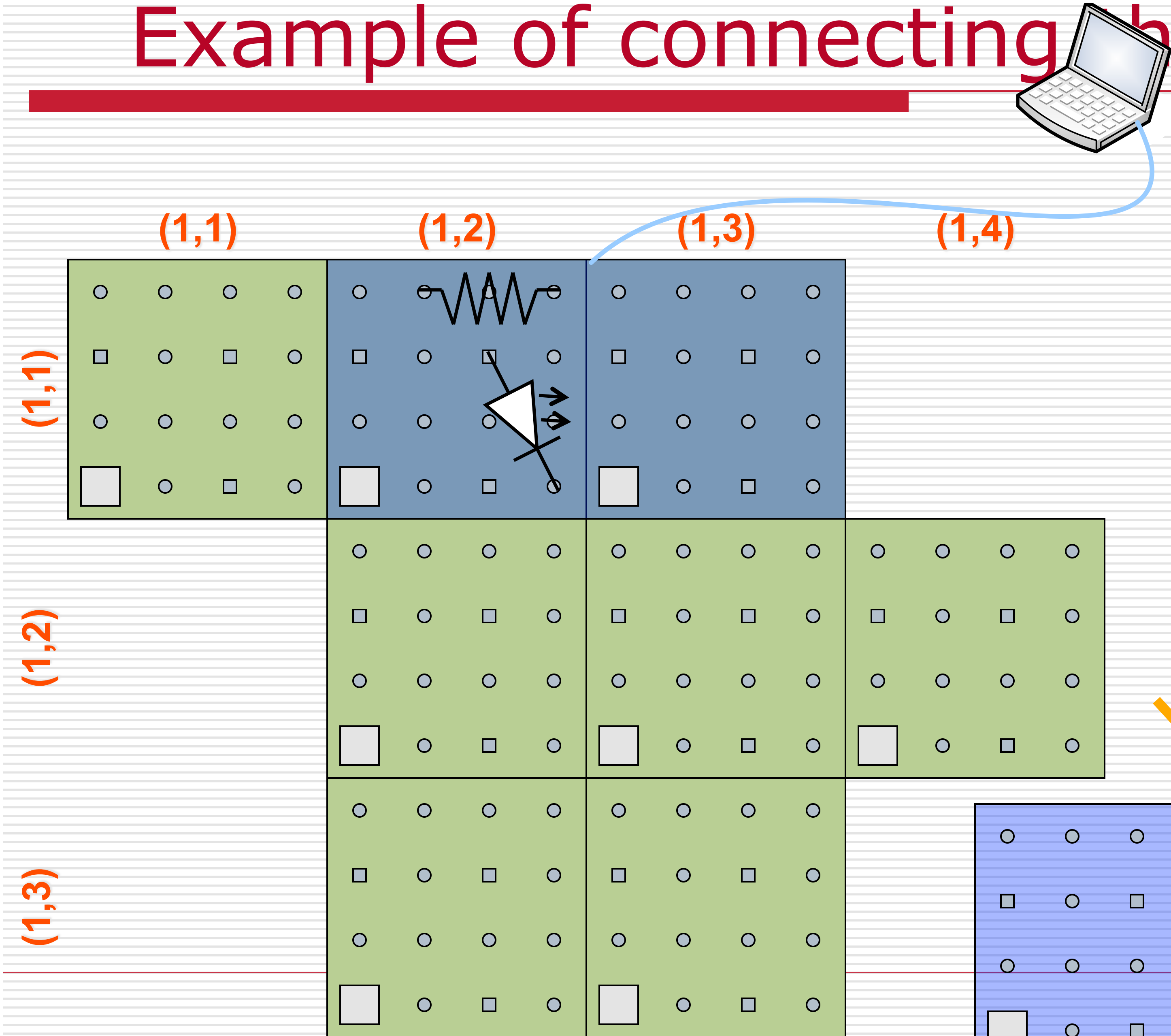
Example of connecting the cells



AWP: 8 cells

Module A:
1 resistor
1 LED

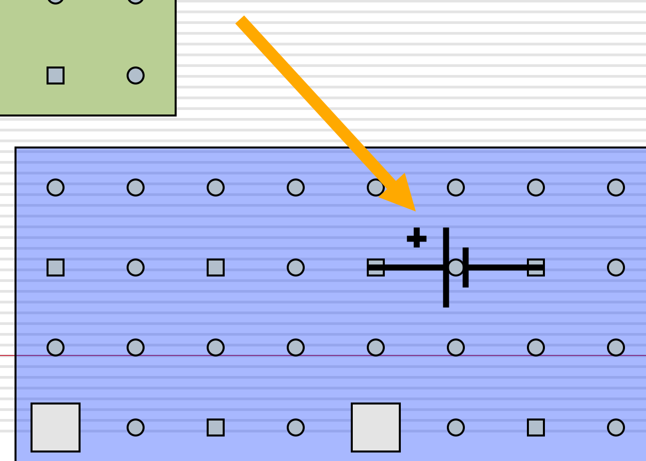
Example of connecting the cells



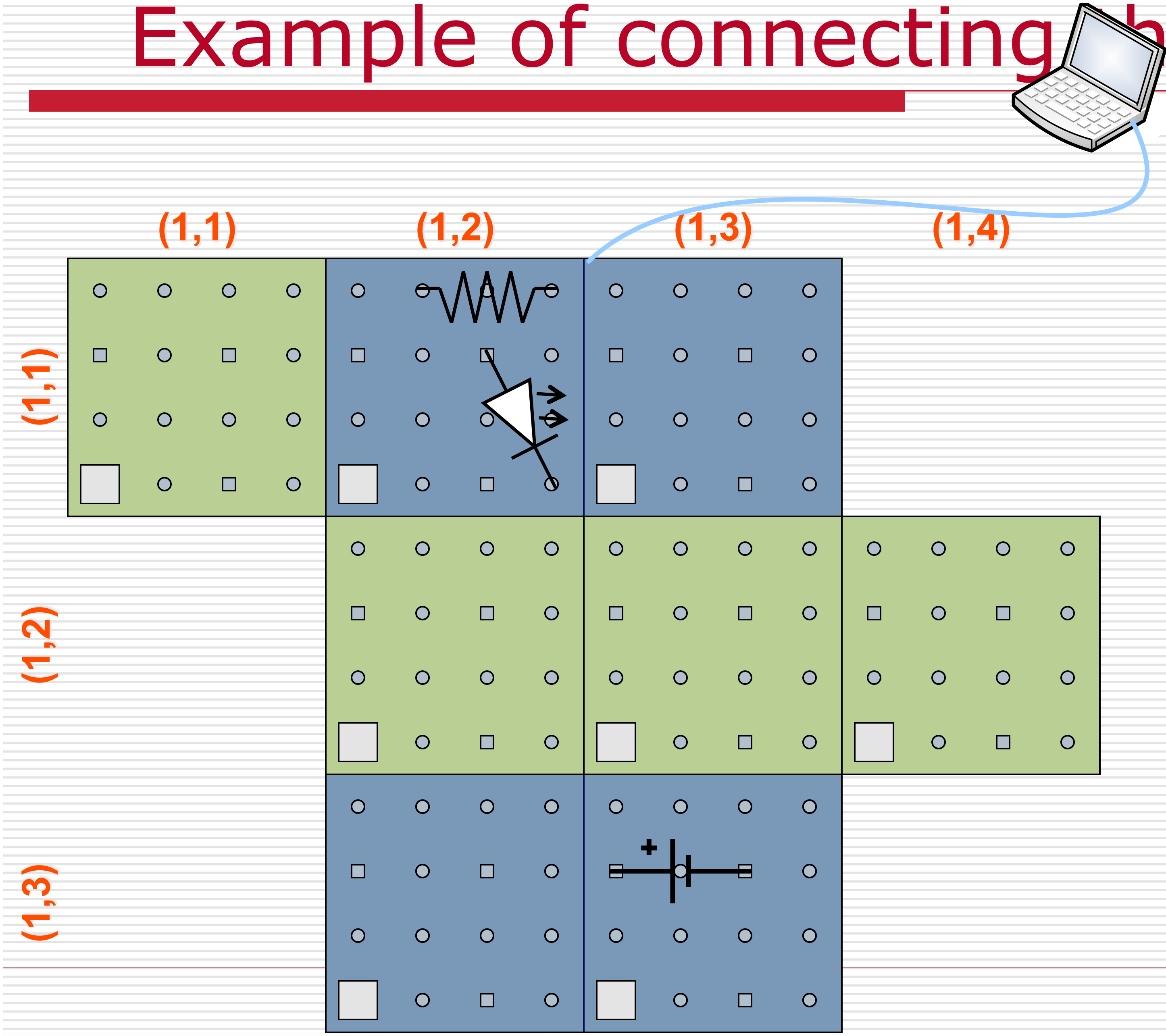
AWP: 8 cells

Module A:
1 resistor
1 LED

Module B:
1 battery



Example of connecting the cells

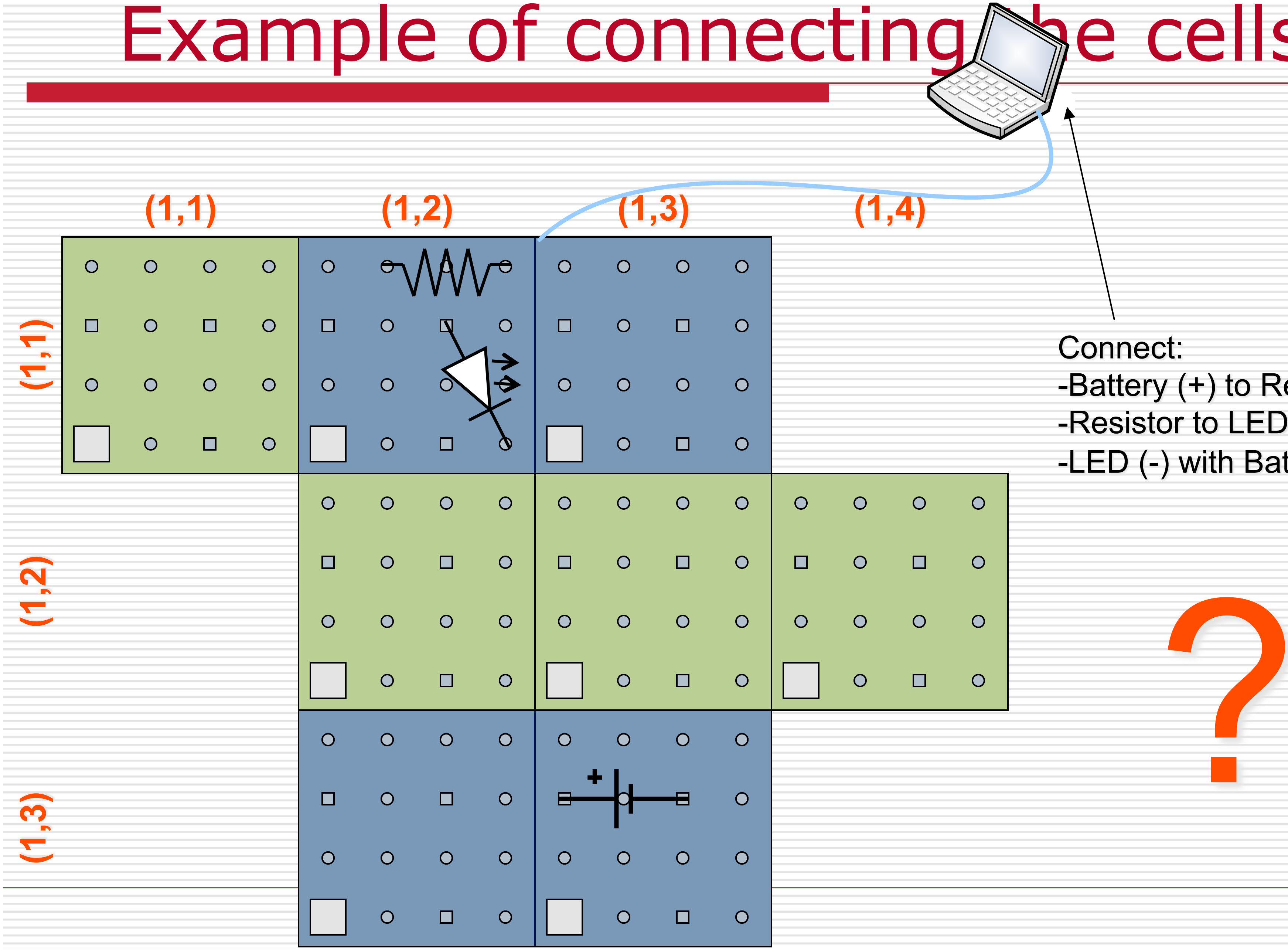


AWP: 8 cells

Module A:
1 resistor
1 LED

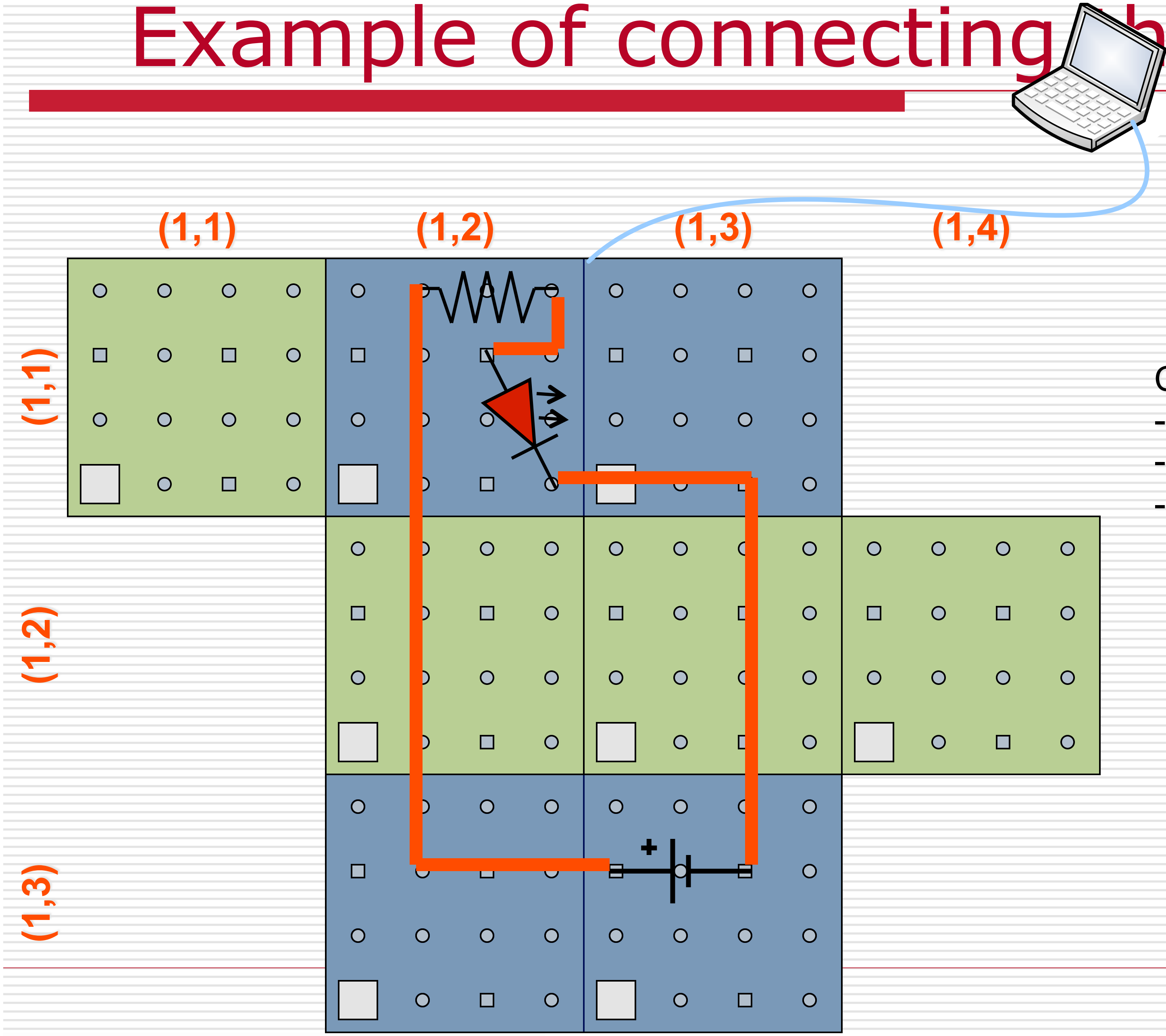
Module B:
1 battery

Example of connecting the cells



Connect:
-Battery (+) to Resistor.
-Resistor to LED (+).
-LED (-) with Battery (-).

Example of connecting the cells



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-Resistor to LED (+).
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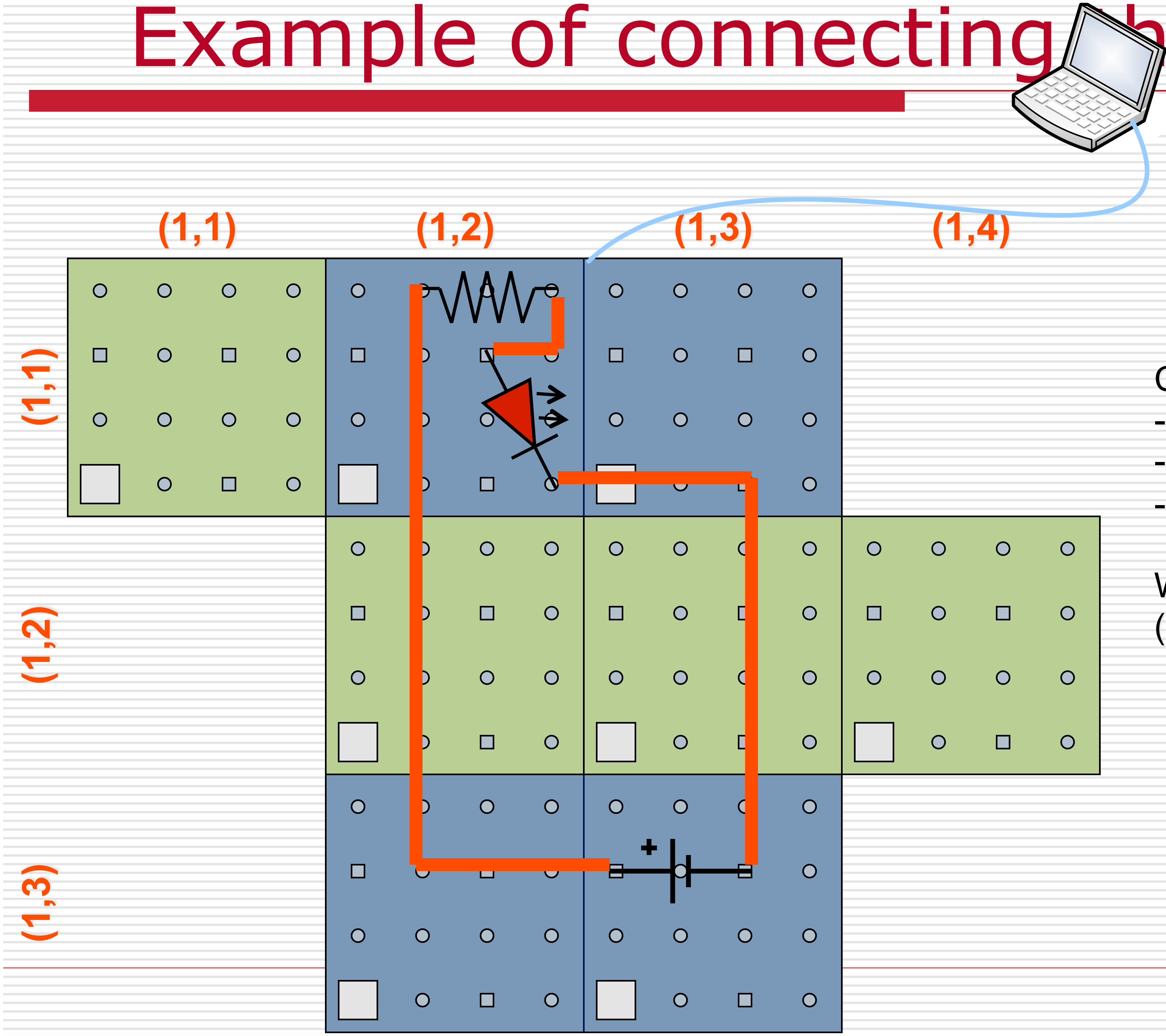


Connect:

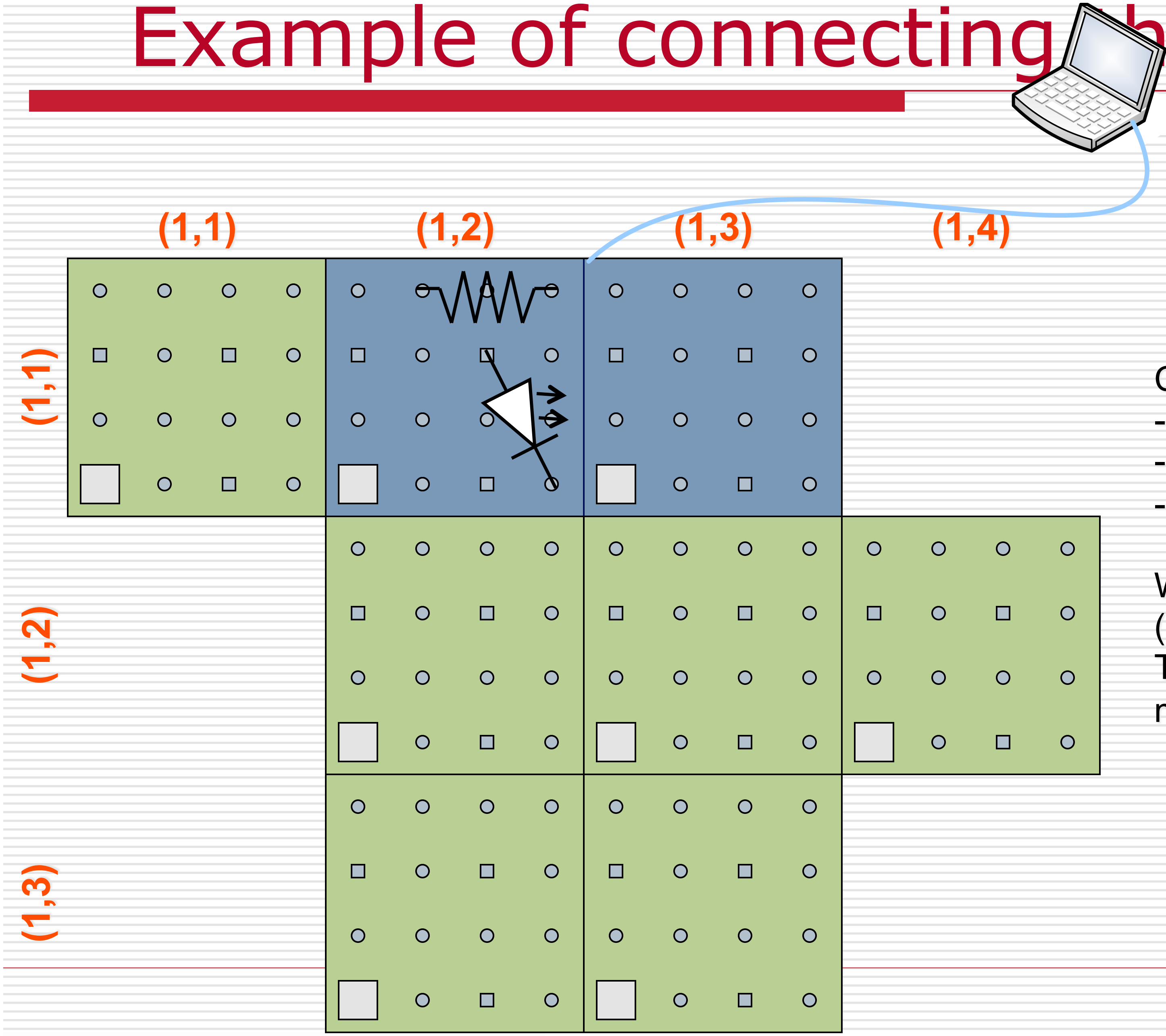
-Battery (+) to Resistor.

-Resistor to LED (+).

-LED (-) with Battery (-).

What if the module B (battery) is removed?

Example of connecting the cells

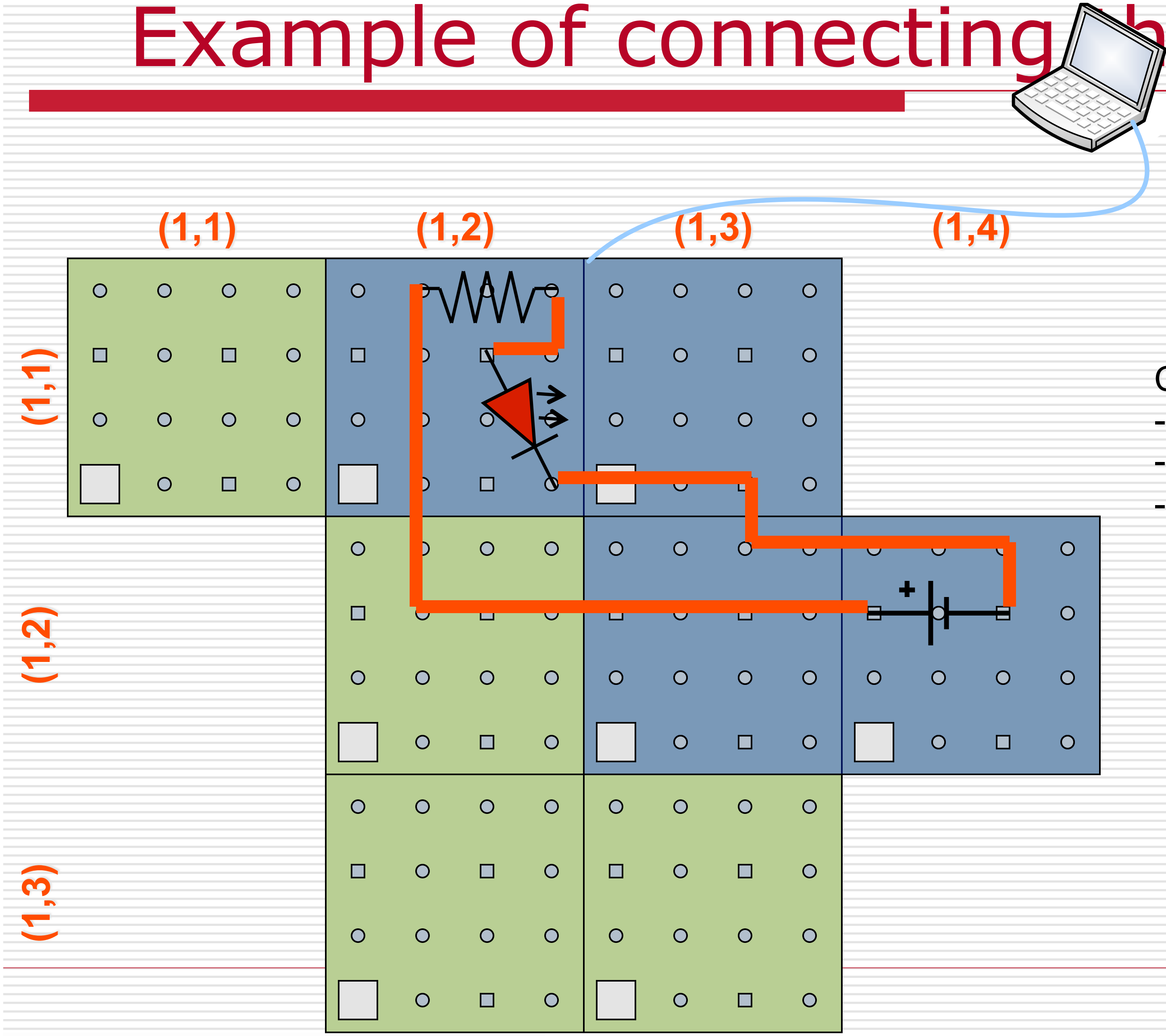


Connect:
-Battery (+) to Resistor.
-Resistor to LED (+).
-LED (-) with Battery (-).

What if the module B (battery) is removed? The AWP looks for the module until it finds it.

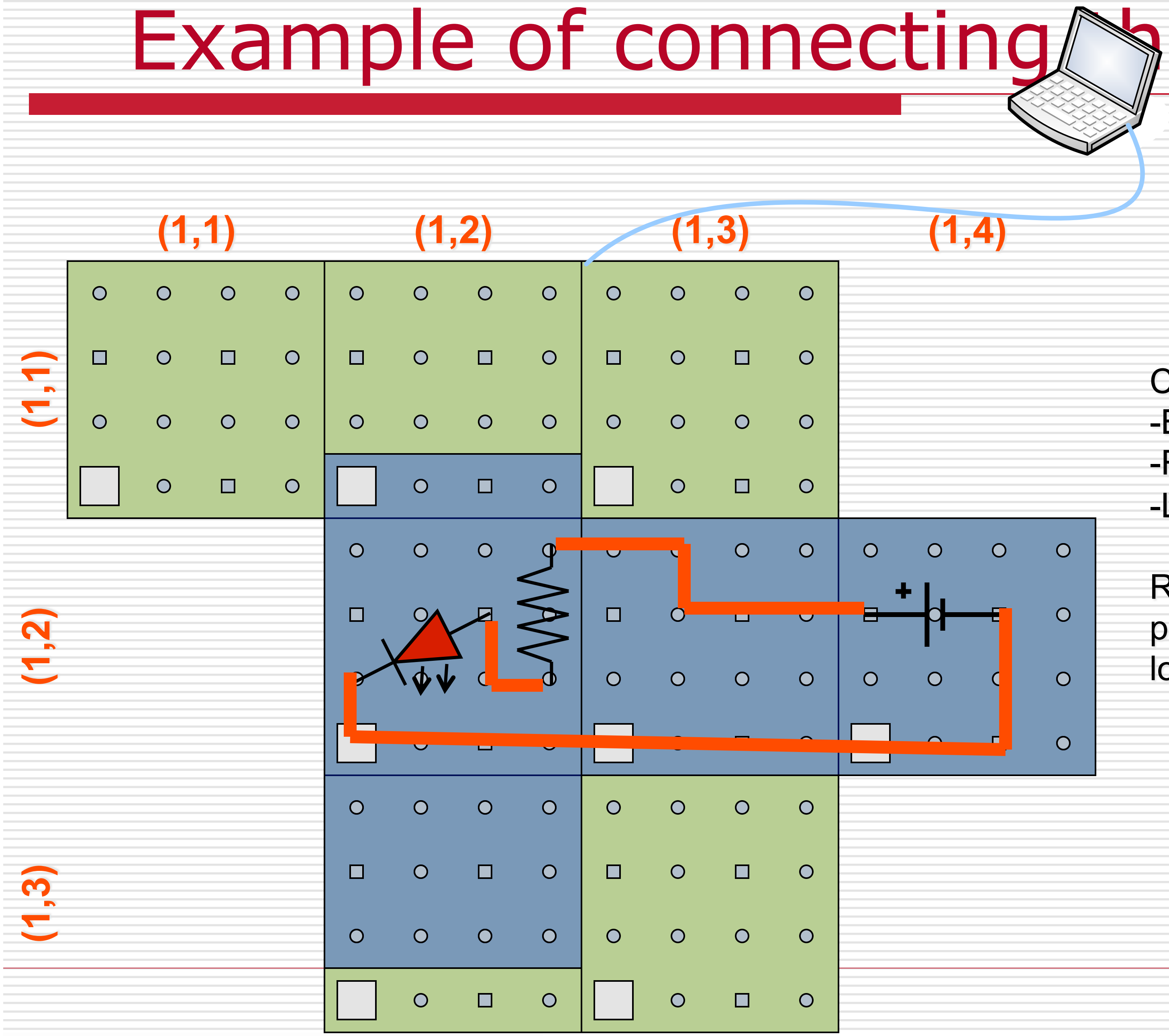
?

Example of connecting the cells



Connect:
- Battery (+) to Resistor.
- Resistor to LED (+).
- LED (-) with Battery (-).

Example of connecting the cells

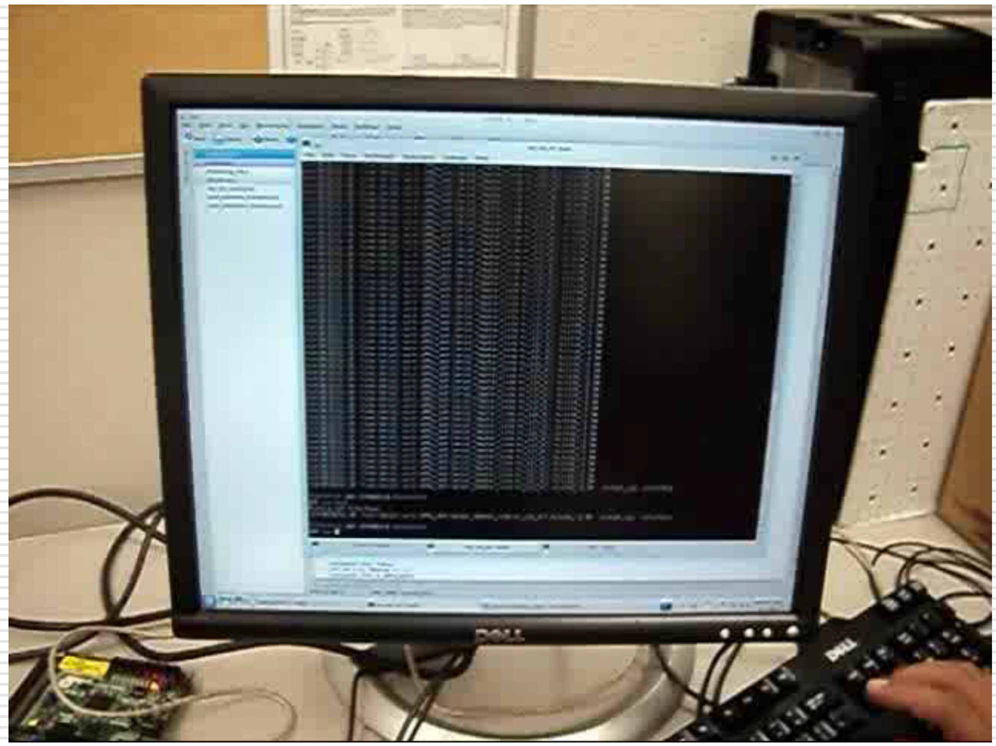


Connect:
-Battery (+) to Resistor.
-Resistor to LED (+).
-LED (-) with Battery (-).

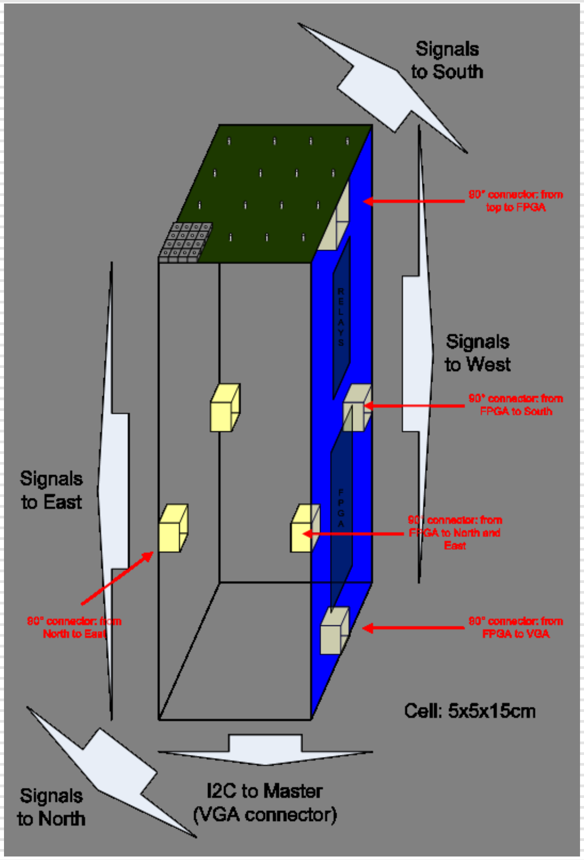
Remove module A and place it in another location.

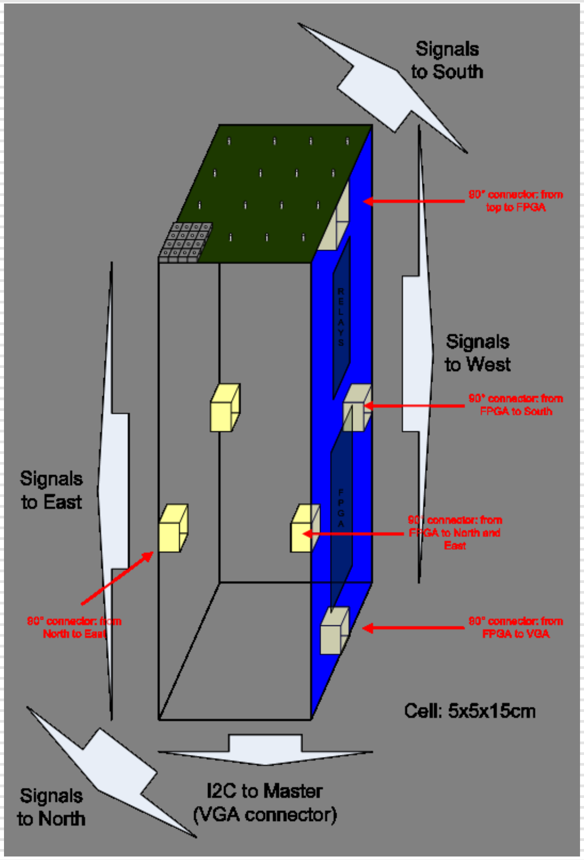
Prototype 1: alpha version

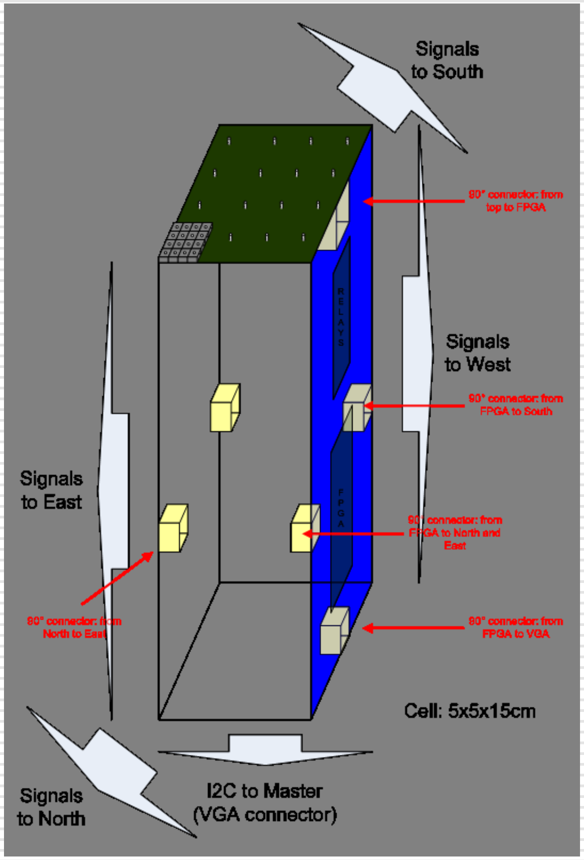
Prototype 1: alpha version (cont'd)



Conclusions and Future Work

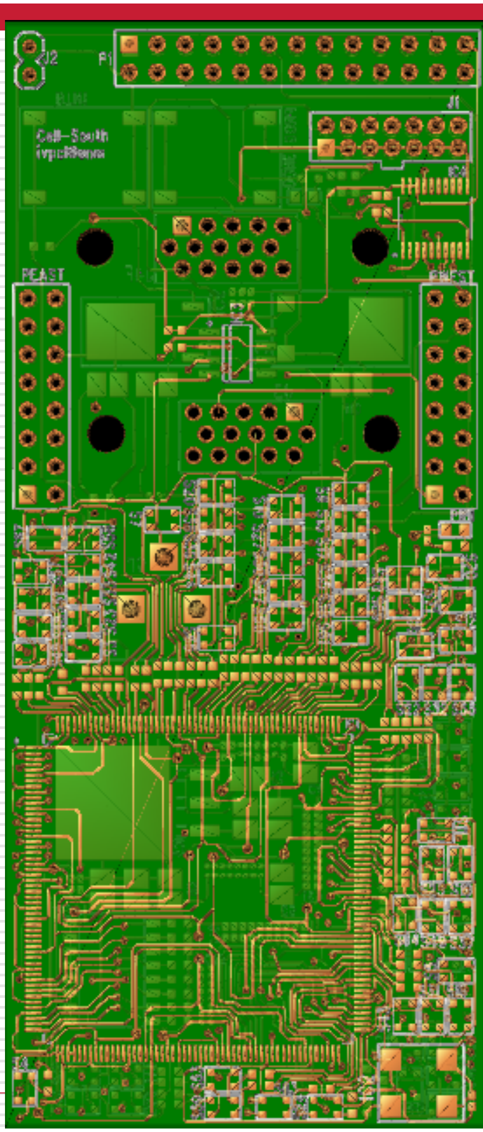


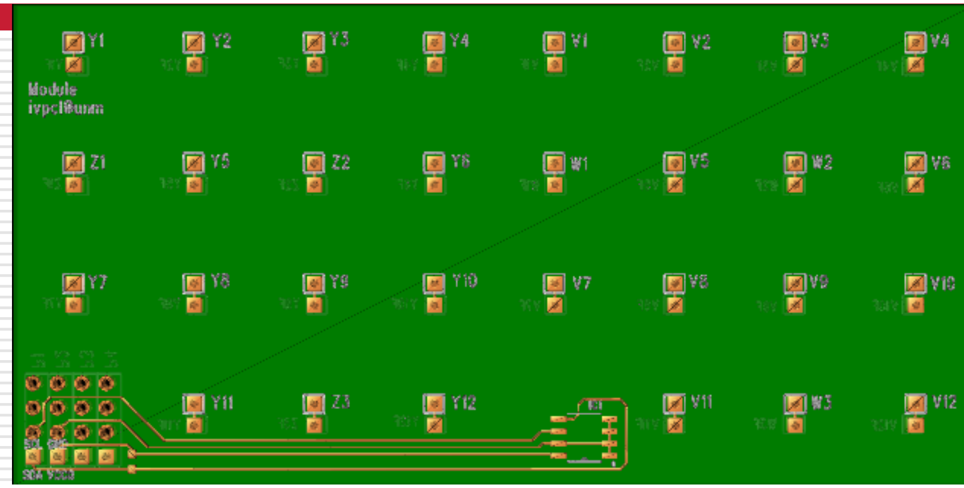




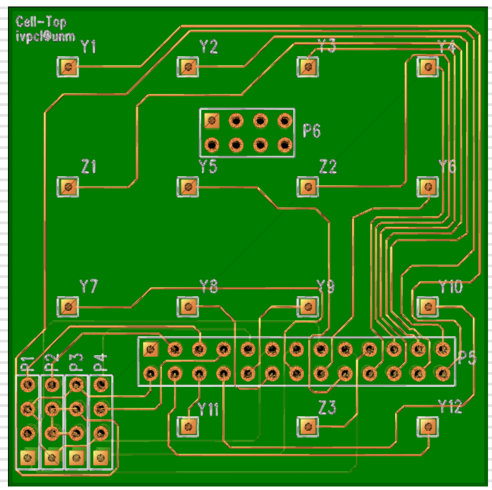
Conclusions and Future Work

FPGA + relays

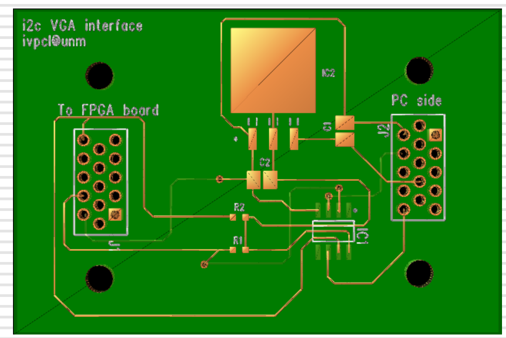




Module



Top



I2C Expander

Conclusions and Future Work

- We have successfully implemented a first (and big) version of the AWP using Spartan3 boards, PhotoMOS relays, and a C based software.
- Reduce scale of cells to 5x5 cm.
- No cables, no wires.
- I2C expander.
- Exploit subgraph capabilities to route different signals.
- GUI implementation.
- RF signals.
- Fully Implement Self-Healing Algorithm.
- Greater decision making at the cellular level.