Small Microprocessor (SM) Design Using AXI4 Full of ARM Cortex-A9

By

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Outlines:

- Overview
- Methodology & Block Diagram
- Result & discussions
- Conclusions & Future work
- Demo

Overview

- We implement a simple microprocessor where instructions are processed in one clock cycle.
- We design an AXI4_Full interface for a small microprocessor (SM) peripheral.
- We integrate this custom peripheral into an embedded system in Vivado.
- We also create a software application in the SDK tool that can communicate with the peripheral.
- The output is mapped to external outputs on the development board LEDs.

Methodology & Block Diagram

VBC_Architecture





VBC_MultiRound

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AXI4_Full_SM_LEDs















Result & discussions

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mySM_ip_OneRound3

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mySMfull_v1_0_OneRound

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tb_mySMAXI4Full_behav.wcfg* _ 0 7 X Q 📓 🔍 Q 🔀 📲 🔀 M 💌 🐭 🕂 🕼 🖬 ¢ 35.000 ns Value Name 400 ns 450 ns 500 ns 550 ns 600 ns 650 ns 700 ns 750 ns 800 ns 850 ns 900 ns 950 ns 1,000 ns 1,050 ns 1,100 ns soo_axi_aclk 1 **b** s00_axi_aresetn 0 le rst > V s00_axi_wdata[31:0] 00000000 00000000 00000000 00000004 00000005 00000007 00000008 00000009 0000000a 0000000b V s00_axi_rdata[31:0] 00000000 00000006 Ъy **S**8 **S4** s5 🚺 **S7 S7 S7 S7 S7** YO) **S7 S7 s**2 le orden 0 1 🟭 owren \1\2\3\4\5\6\7\8\9\d\D\D\D\D\d\D\d\D\D\D\D\D\D\D\D\ 10 D D 0 1 2 0 1 2 300 16 C 0 0 P P 0 Π 2 3 4 5 6 0 1 L in 0 0 le start step. 0 0 s00_axi_rvalid 0 > V s00_axi_awid[0:0] 0 00 > V s00_axi_awaddr[5:0] 00 00 V s00_axi_awlen[7:0] 00 2 s00_axi_awsize[2:0] 2 0 8 s00_axi_awburst[1:0] 0 s00_axi_awlock 0 s00_axi_awcache[3:0 0 0 0 Solution 0 0 > V s00_axi_awqos[3:0] 0 0 > 😼 s00_axi_awregion[3:0_0 > W s00_axi_awuser[-1:0] soo_axi_awvalid 0 > V s00_axi_wstrb[3:0] £



mySMfull IP Design



mySMfull_v1_0 _LEDs_OneRound

tb_mySMAXI4Full_LEDS_behav.wcfg* _ 0 7 X Q X 📲 M M 🛨 🏝 🕂 🕼 ୶ 🔤 Q. Ð, ÷. 639.920 ns Name Value 1,000 ns 400 ns 450 ns 500 ns 550 ns 600 ns 650 ns 700 ns 750 ns 800 ns 850 ns 900 ns 950 ns 1,050 ns 1,100 soo axi aclk soo_axi_aresetn 1 le rst 0 s00_axi_wdata[31:0] 00000000 00000000 0 4 8 b LEDS[3:0] 6 7 9 5 а 00000004 00000000 00000004 00000009 0000000a 0000000b V s00_axi_rdata[31:0] 00000005 00000006 00000007 0000000 **S8 S4** s5 🚺 s7 s7 **S7 s7 s**2 Вy Xo **S7 S7 S7** orden 0 le owren 0 16 D 0 1 C 0 $1 \sqrt{2} 0 \sqrt{1} \sqrt{2} \sqrt{3}$ 0 0 P 0 2 4 5 6 0 0 1 з L in 0 16 start 0 0 step 0 0 > V s00_axi_awid[0:0] 00 00 s00 axi awaddr[5:0] s00_axi_awlen[7:0] 00 00 2 Interpretation with a state with a solution with a solutio 2 0 ♥ s00_axi_awburst[1:0] 0 0 s00 axi awlock 0 s00_axi_awcache[3:0] 0 0 0 > V s00 axi awprot[2:0] > V s00_axi_awgos[3:0] 0 0 0 0 s00_axi_awregion[3:0] s00_axi_awuser[-1:0] 0 soo axi awvalid > V s00_axi_wstrb[3:0] f > < -1



mySMfull_v1_0_LEDs_Delay_OneRound

tb_mySMAXI4Full_LEDS_behav.wcfg _ D 7 X Q 55 📲 🖌 射 🛫 🖅 👎 👘 🖂 0 Q. -735.000 ns Name Value 400 ns 500 ns 600 ns 700 800 ns 900 ns 1,000 ns 1,100 ns 1,200 ns 1,300 ns 1,400 ns 1,500 ns 1,600 ns 1,700 ns 1,800 ns s00 axi aclk 300_axi_aresetn le rst 0 > V s00_axi_wdata[31:0] 00000000 00000000 4 8 LEDS[3:0] 0 5 6 7 . a h 00000000 0000000 00000005 00000007 00000009 0000000a 0000000b 00000004 00000006 00000008 😼 s00_axi_rdata[31:0] **s**2 **S**4 S5 S7 s7b S7b **s**2 18 y **S8** S7b S7 s7b **S7** S7b **S7** s7b **S7** S7b **S7** \$7 Q Π 0 0 0 0 0 0 0 0 orden 0 owren _____ 0 0 D 0 0 XXX 0 L C 0 XX) 0 0 0 0 0 2 0 P 1 3 4 5 6 L in start step s00_axi_rready b s00 axi rlast s00 axi rvalid 00 Image: Solo axi awaddr[5:0] 00 00 00 s00_axi_awlen[7:0] 2 s00_axi_awsize[2:0] 2 n ₩ s00_axi_awburst[1:0] 0 soo_axi_awvalid 0 s00 axi awreadv 0 s00_axi_wlast 0 s00_axi_wvalid soo_axi_wready 0 > < -1

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tb_mySMAXI4Full_LEDS_behav.wcfg - 8 7 X Q 🖬 @ Q 💥 📲 🖊 M 🔁 💇 🕂 🕼 ÷. Name Value 620 ns 640 ns 660 ns 720 ns 740 ns ,500 ns 520 ns 540 ns 560 ns 580 ns 600 ns 680 ns 700 ns 760 ns 780 ns s00_axi_aclk 3 s00_axi_aresetn 1 le rst 0 ¹⁰ s00 axi wdata[31:0] 00000000 00000000 0 LEDS[3:0] 0 4 5 6 00000000 00000004 0000 > V s00_axi_rdata[31:0] 00000000 **S4 S**7 s7b s7b le y **S**2 **S**5 **S6 S**8 \$7 100 0 1 3 χ 4 / 5 6 7 8 ¥ 9 0 0 0 orden owren 0 $\square \ 14 \ 15 \ 16 \ 17 \ 18 \ 19 \ 20$ D 0 0 2 3 0 0 1 2 C 0 2 3 0 P 0 0 Lin 0 start 0 step 0 16 s00_axi_rready 0 [™] s00 axi rlast 0 s00 axi rvalid 0 00 00 s00_axi_awaddr[5:0] 00 00 s00_axi_awlen[7:0] 2 s00_axi_awsize[2:0] 2 0 s00_axi_awburst[1:0] 0 s00 axi awvalid 0 s00_axi_awready 0 0 s00 axi wlast s00_axi_wvalid 0 s00_axi_wready 0

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Conclusions & Future work

- The control signal input data **0xAA55FFFF** is provided to the designed.
- The CPU operation is triggered by the **FSM** and start counting provided counter sequences.
- The counter will count value from **0x04 to 0x0B** and repeats the same counter if the state machine is triggered again.
- The **LEDs** are used as external outputs of the Zybo board.
- All over, this project was great learning from the class materials and also provides the **platform** to grow our skills in related filed within industries.
- We believe that this project work was very didactic to learn about real-world technology.
- This design could be **expanded** into a more complex processor with a stack to allow for less reading and writing between the software and hardware.
- The instruction set could be expanded from a 3-bit to a 4-bit or higher set depending on the required project complexity.
- The **software** can be used with more than two processors.
- The **reconfigurable partition** can be designed to allow multiple configuration switches at run time.

Demo

- <u>Project Demo Final.mp4 Google Drive</u>
 - (Also provided with submission folder)

Thank you !!

Any Question?