## DFX Calculator [16 8 4] (Adder, Subtractor, Multiplier)

ECE 5736 – Reconfigurable Computing

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## **Dual Fixed Point Background**

**Standard Numerical Representations:** 

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  - Fixed and Floating Point:
     Floating point features a large dynamic range at the expense of a large resource usage on the other hand fixed point requires fewer resources, but it delivers low dynamic range.
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  - Dual Fixed point (DFX):
     This numerical representation is a compromise between Fixed and Floating point number system, it overcomes the limitations of Fixed and Float point humbers
- For applications such as Digital Signal Processing where a large dynamic range is required using the floating point data representation
- The DFX has Exponent and Significand, depends on the exponent value DFX can have two types of scaling: num0 and num1
- For the project DFX calculator we are using the DFX number system

### DFX Process & Formulas

- As part of the pre scaling convert the DFX to FX
- Process the data for Fixed point Addition/Subtraction/Multiplication
- As part of the post scaling convert FX to DFX



- Range for num0:  $[-2^{n-p_0-2}, 2^{n-p_0-2} 2^{-p_0}]$
- Range for num1:  $[-2^{n-p_1-2}, -2^{n-p_0-2} 2^{-p_1}] \cup [2^{n-p_0-2}, 2^{n-p_1-2} 2^{-p_1}]$

✓ Unsigned numbers with $n$ bits:	$\frac{ 2^n - 1 }{ 1 } = 2^n - 1 \rightarrow Dynamic \ Range = 20 \log_{10}(2^n - 1) \ dB$
✓ Signed numbers (2's complement): [n p]	$\frac{ -2^{n-1-p} }{ 2^{-p} } = 2^{n-1} \to Dynamic \ Range = 20 \log_{10}(2^{n-1}) \ dB$
✓ Dual fixed point (DFX) numbers: n_p0_p1	$\frac{ -2^{n-2-p_1} }{ 2^{-p_0} } = 2^{n-2-p_1+p_0} \to Dynamic \ Range = 20 \log_{10}(2^{n-2-p_1+p_0}) \ dB$

Dynamic range=20log10(2n+p0-p1-2) dB

## Benefit of using DFX over Fixed & Floating Point

By choosing the right scaling, DFX can have similar performance to fixed-point and also having the capability of handling a wider dynamic range of the Floating point.

Number System	DFX	Fixed-Point	Floating-Point
Format	32-bit	32-bit	32-bit IEEE
Dynamic Range	2*46 ~276dB	2 <sup>+46</sup> ~187dB	2 <sup>+254</sup> ~1529dB

Table 1. Dynamic Range Comparison. The DFX is 32 bits wide, P0 =16 and p1=4

Ref: IEEE document/1515822



### **File Hierarchy**



## FSM



#### **State Description**

**S1**: If there is data to be read, it will start execution

**S2**: Input data is written into memory

**S3**: Read the first byte of multiplexor

**S4**: Read second byte of multiplexor

# Hardware/ Software Tasks

#### Hardware

Input data is read from axi\_wdata.

Digital Systems perform processes. (DFX Multiplier/ DFX Adder).

Output data of Digital Systems is sent to Multiplexer (2 to 1).

FSM will trigger output FIFO to read first set of data and then the next set.

Data is output on axi\_rdata.

#### Software

Will take User input.

Provide input into AXI Interface.

Read output from AXI Interface.

Parse the data according to operation.

Determine if there is overflow.

Print results to User.

#### **DFX Adder/ Subtractor**



### **DFX Multiplier**



#### **DFX Multiplier Range Detector+ Bit slicing**



A(N-1)	B(N-1)	ERD	SCTRL	ECTR L
0	0	0	01 (B)	0
0	0	1	11 (D)	1
0	1	0	00 (A)	0
0	1	1	01 (B)	1
1	0	0	00 (A)	0
1	0	1	01 (B)	1
1	1	0	10 (C)	0
1	1	1	00 (A)	1

## Test bench Simulation : Input A = FA2A ; Input B = OA0E

											381.883	ns			
	Name	Value			340 ns .		350 n	s	360 ns	l <sup>370 ns</sup> , l <sup>3</sup>	80 ns		1 <sup>390 ns</sup> .	400 ns .	$ ^{410 ns}$
	I C_SUU_AXIER_WIDTH	1										ننظ		1	
	Ът	10000 ps							10000 ps					X	
	<sup>™</sup> MAX_B	100							100						
Input A —	→ ₩ A[15:0]	fa2a							fa2a						
Input B—	▶ ₩ B[15:0]	0a0e							0a0e						
Sum	▶ 😽 R[15:0]	faca							faca					2	
Difference	🛶 😻 Sub[15:0]	f98a							f98a					2	
Product	🛶 😻 P[15:0]	c552							c552					2	
MUX 1st input	→ 😽 I_in[31:0]	facaf98a							facaf98a						
IVIUX 2nd input-	N_next[31:0]	c5520000							c5520000						
	> 👹 DO[31:0]	facaf98a	fa	af98a	•X	c552	0000	χ		facaf98a					
	> 👹 DI[31:0]	fa2a0a0e							fa2a0a0e						
	<b>1₿</b> γ	S2	S2 🗸	S:	з Х	s	4	χ		52					
	> 👹 S_AXI_RDATA[31:0]	00000000						0000000	0				facaf98a		
	> 😽 s00_axi_wdata[31:0]	00000000							00000000						
	> 😽 Az[14:0]	7a2a		Q					7a2a						
	> 😻 Bz[14:0]	0a0e					K		0a0e						
	> 😻 F[29:0]	3fc5524c							3fc5524c						
	🐻 Erd	1													
	16 E_rdet1	0													
	16 E_rdet2	1													
	16 E_rdet3	1													

## Test bench Simulation : Input A = A004 ; Input B = B1C3

					384.600 ns		
Name	Value	280 ns 300 ns 3	320 ns   340 ns	l <sup>360 ns</sup> . l <sup>380</sup>	ns	1 <sup>400 ns</sup> .	1 <sup>420</sup> 1
C_SUU_AXIER_WIDTH	1						┼┷┙
Ът	10000 ps		10000 ps				
₩ MAX_B	100		100				
> 😽 A[15:0]	a004	0000		a004			
> 😽 B[15:0]	b1c3	0000	_X	blc3			
> 😽 R[15:0]	d1c7	0000	_X	dlc7			
> 😽 Sub[15:0]	ee41	0000	_X	ee41			
> 😻 P[15:0]	9270	0000	_X	9270			
> 😻 l_in[31:0]	d1c7ee41	0000000	LP L	Lc7ee41			
> 😻 N_next[31:0]	92708000	0000000	92	2708000			
> 👹 DO[31:0]	d1c7ee41	0000000	dlc7ee41 / 9270 /	dlc7ee41			
> 👹 DI[31:0]	a004b1c3	0000000		04b1c3			
ן א אין אין אין אין אין אין אין אין אין	S2	52	X 53 X 54 X	\$2			
> 👹 S_AXI_RDATA[31:0]	00000000		0000000		dlc7ee41		
> 😽 s00_axi_wdata[31:0]	00000000	0000 a004b1c3	0000000				
> 😽 Az[14:0]	2004	0000	_X	2004			
> 😼 Bz[14:0]	31c3	0000	_X	31c3			
> 😽 F[29:0]	0639270c	0000000		539270c			
1⊌ Erd	1						
l⊌ E_rdet1	1						
li E_rdet2	1						
li E_rdet3	1						

### Test bench Simulation : Input A = BEEF ; Input B = FADE

\*\*Calculation of Multiplication on next slide

## Multiplication Verification (Manual and Matlab)



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🗋 Name 🔺		Ē	my_fx2dec.m × my_dec2fx.m × my_bitcmp.m × test.m × Test2.m × +
<ul> <li>my_bitcmp.m</li> <li>my_dec2fx.m</li> <li>my_fx2dec.m</li> <li>test.m</li> <li>Test2.asv</li> <li>Test2.m</li> </ul>		1 2 3 4 5 6	<pre>- A = my_fx2dec('01111011101111',15,4,'s'); %3EEF - B = my_fx2dec('111101011011110',15,4,'s'); %FADE - F = A*B - C = my_dec2fx(F,30,8,'s')</pre>
Details	^		
Workspace			
Name 🔺	Value	C	ommand Window
A B abc C F	1.0069e+03 -82.1250 '11111010111100111110010 -8.2695e+04	fx	<pre>&gt;&gt; Test2 F =     -8.2695e+04 C =     11111010111100101000010 &gt;&gt;</pre>
		14	

## Softwar



### **SDK TERMINAL**

Condition	SDK Terminal
Calculations with no Overflow	AXI4-Full DFX Calculator Peripheral: Test
	Peripheral: Base address is 0x7AA00000
	Input A = FA2A, Input B = 0A0E Sum = FACA, Difference = F98A, Product = C552
Calculations with Overflow in Addition	AXI4-Full DFX Calculator Peripheral: Test
	Peripheral: Base address is 0x7AA00000
	Input A = A004, Input B = B1C3
	Sum = Overriow Difference = EE41, Product = 9270
Calculations with Overflow in Subtraction	AXI4-Full DFX Calculator Peripheral: Test
	Peripheral: Base address is 0x7AA00000
	Input A = BEEF, Input B = FADE
	Sum = B9CD Difference = Overflow Product = CF94

## Project Responsibilities

Oshin Gupta	-Creation of DFX Multiplier & Testbench (Digital System) -Assistance in Bus Interface -Circuit Block Diagrams & Test Bench runs in presentation
Chandra Kasimkota	<ul> <li>-Research of background for using User inputs in SDK Terminal</li> <li>-High level diagrams in HW/report</li> <li>-Background of DFX slides of presentation</li> </ul>
Tahmid Uddin	-Bus Interface between circuits & AXI Full Interface -Software Implementation -System Diagrams in presentation

## Conclusion

- Challenges
  - Multiplier
- Next steps
  - Adding the Divider Circuit
  - Adding User Inputs
  - Add on-the-fly reconfigurable portion to set P0 & P1