8-Bit Calculator With Keyboard Input

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Description

- Constructing a calculator which performs the four basic mathematical operations
 - \circ Addition, subtraction, division (modulus), multiplication
- USB (PS/2 supported) keyboard
- Nexys4 FPGA board will manage the computation
- Nexys4 7 segment display

Keyboard - ASCII - Binary

- USB(PS/2) Keyboard
- Keyboard input takes ASCII code using decoder will pass values into registers
 A[0-2], B[0-2], OP
- Each register sends to appropriate ASCII to binary conversion register
- Converted bits sent to register that holds binary value
- Binary 8 bit numbers are send to ALU as A and B inputs
 OP: a 2 bit input



Top-Level



ASCII to Binary Simulation

								308.5	583 ns					
Name	Value		50 ns	100 ns	150 ns	200 ns	250 ns	30 <mark>0</mark> ns		350 ns	400 ns	450 ns	500 ns	550 ns
▶ 🛃 ascii1[7:0]	31	30	31	33	35	32	30		31	33	35	32	30	31
▶ 🔩 ascii2[7:0]	31	30	3	1	33	32	30		3	1	33	32	30	31
▶ 🔩 ascii3[7:0]	30	31	30	31	36	34	31		30	31	36	34	31	30
lle e	1													
🕨 式 bin[7:0]	110	1	110			224	1		110			224		110

Control Circuit

- Calc_btn triggers whether the values are ready to be put into registers.
- Control Circuit waits for the first keys to be pressed which will indicate it's A value and enable the A ascii to binary register.
- Second calc button press will enable the operator ascii to binary register.
- The third will enable the B value for ascii to binary register.



Calculations

- Using VHDL provided libraries
 - use IEEE.STD_LOGIC_1164.ALL
 - use IEEE.STD_LOGIC_ARITH.ALL
 - use IEEE.STD_LOGIC_UNSIGNED.ALL
- 8 bit inputs and outputs with a 2 bit selector for operation
- Division
 - o 8 bit by 8 bit divider with 8 bit quotient and remainder
- Remainder set to 0 for all but division
- Sends to assigned register to hold value

ALU Simulation

				27.613 ns										
lame	Value	0 ns	20 ns		40 ns	<u></u>	60 ns	80 ns	100 ns	120 ns	140 ns		160 ns	180 ns 200
en_alu	1													
📲 a[7:0]	00001000		000010	00		X	00000100			00001000			0000110	0
📑 b[7:0]	00000100		000001	00		Χ		0000	0010			<	0000010	0
📑 op_sel[1:0]	00		00				01			10			11	
📲 result[7:0]	00001100		000011	00		X	00000010			00010000		<	0000001	1
📲 re[7:0]	0000000							000	00000					

7 Segment

- Using a serializer to display results
- The result of the calculation is displayed as the Hexadecimal value on the two leftmost displays
- The remainder is displayed on the two rightmost displays as the remainder's Hexadecimal representation