

Digital Security Alarm System

ECE2700 Final Project Report

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Abstract— In this project, students use skills taught in ECE 2700 Digital Logic Design and preceding classes to create a digital system utilizing FPGA and Vivado to code VHDL. The students decided to create a digital alarm system that will sound when a motion sensor is triggered and can be disarmed using a four-switch combinational code. The primary goal of this project is to dissuade intruders. The creation of this digital system led to several findings and additional suggestions.

I. INTRODUCTION

This digital motion alarm system will necessitate several electrical components in addition to software programming. This project will make use of a Nexys A7 100T FPGA, and buzzer amplifier, an HC-SR501 PIR (Passive Infrared) motion sensor module to detect motion within an area, an LED, an active buzzer, a micro breadboard, and jumper wires. The code will be written in Vivado VHDL 2019.1. The goal of this study is to better understand and duplicate the operation of alarm systems. Another incentive is knowing whether there is an intruder, or someone present within a room for security concerns, with the intention that a buzzer will stop them before they steal anything.

This project can help to improve security and safety by sounding an alarm whenever there is movement in an area where intruders are not welcome. This project incorporates many of the concepts covered in this semester thus far. To be capable of putting specific components into code, one must first understand how they work. It is critical essential students not only grasp how to code components in VHDL using Vivado, but additionally how to connect these parts using a top file and construct a comprehensive testbench to mimic his or her code.

The abilities required for performing these tasks were thoroughly covered in the course and were heavily applied during this project. Counters, decoders, and deterministic finite systems are examples of important Vivado coded components that were taught in class. To complete this project, the students needed to study a few things on their own. Students required to read the Nexys FPGA

documentation to figure out what the I/O pins on the FPGA were called to discover them in the xdc restrictions file. Understanding how to use a PIR sensor, how to properly feed voltage to the FPGA without destroying the board, and how to properly feed voltage to the FPGA are all challenges of this project. Voltage should be fed from the FPGA board to a buzzer. It is also critical that students understand how to wire simple circuits. This project's uses are applicable in any case where a motion sensor alarm is required.

II. METHODOLOGY

A. System's Goal

This project is supposed to replicate a home security digital alarm system in order to prevent any intruders from breaking in. The alarm is activated only in the case of motion detection by a Passive Infrared sensor (PIR sensor). The way it works is that the user has three attempts in order to get the code right. The code has five bits and is controlled by four switches (SW[3]-SW[0]) and also a button (CNT BTN) that needs to be held at the same time. So, the button acts as our enter key in a security alarm while the four switches act as the code to be inserted. The correct code is 11001. After every attempt, the user has 8 seconds in between in order to put in another code. If the user guesses the right code in any of the attempts, the normal state is restored, and everything goes back to normality. If the user runs out of attempts, then the buzzer is activated and will make a sound until the right code is inserted again. The setup and the wiring of the Nexys-A7 board is shown in Figure 1 below.

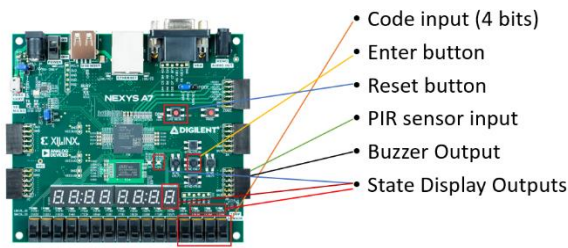


Figure 1: Nexys A7 100T board layout

B. Implementation

In order to implement this system, our group started picking out some components like counters, a decoder, a finite state machine and a BCD counter in order to use them. We had some different ideas how we were going to do this process but ultimately the goal was the same, which was a digital security alarm. We tried doing this project with a comparator where the code inserted is compared to the actual code saved in a state machine but decided to go for this design better as it was less complex and had the same function. All of the components had a specific task that needed to be done in order for this system to work. Figure 2 shows how the circuit was designed and implemented.

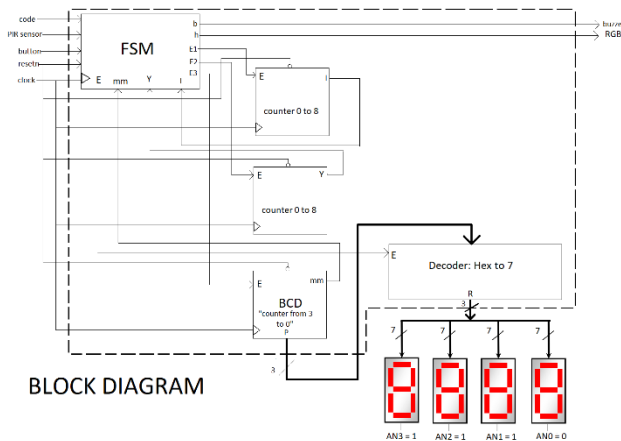


Figure 2: Block Diagram of the System

C. PIR Sensor/Buzzer

The main components that represent this digital alarm system are the PIR sensor and the buzzer. A Passive Infrared sensor (PIR sensor) is a type of sensor that uses infrared temperature to detect any kind of motion and transmit that motion to the FPGA board in this case. So, this sensor only picks up radiation which is released by the human body. It has a wide lens and a wide beam, which makes it able to pick up radiation in a range of 180 degrees. The motion pickup marks the start of the digital alarm system. Before

using this type of sensor, its output was measured using a voltmeter to make sure it doesn't damage the Nexys A7 board. The board only supports a maximum input of 3.8V, so the output of the PIR sensor which acts as the input for the board was measured. After successful measurements, it came out to be around 3.31V, which meant that it was safe for the board to use this sensor. Figure 3 represents the motion sensor that was used to successfully complete this project. On the other hand, an active buzzer is also being utilized. The buzzer releases a sound and acts as a way to alarm everyone that someone is intruding into a house. Since the buzzer is active, it needs a high input from the FPGA Nexys-A7 board in order to get activated.



Figure 3: PIR Sensor Used in the Project

D. Finite State Machine (FSM)

Our project was mainly based on the state machine, where everything is based on the state that we are in. Figure 2 represents the Moore state machine, where each output is dependent solely on the present state and not the inputs. This state machine mainly relies on the code input from the switches and the button and the outputs from the counters. The output goes in the 7-segment screen and in the RGB LED of the FPGA board. The state machine has 8 different states, and each state signifies what is going on with our circuit. The first state is the normal state or the state that there are still three attempts left for the user to insert. In order to go from the first state to the second, the code must be wrong (not 11001) and motion must be detected. If the code is correct or no motion is detected, then the system will stay in the normal state. Once in the second state, then a counter is activated and when the output is high then the code will get checked again. So, in simpler terms, there is a

```

graph TD
    S4[S4  
E3 ← 1, sclr3 ← 1  
rgb ← 100, p ← 0011] -- 0 --> S5[S5  
E4 ← 1, sclr4 ← 0  
rgb ← 101, p ← 0010]
    S4 -- 1 --> S6[S6  
E5 ← 1, sclr5 ← 0  
rgb ← 101, p ← 0001]
    S5 -- 0 --> S6
    S5 -- 1 --> S7[S7  
E6 ← 1, sclr6 ← 0  
rgb ← 101, p ← 0000]
    S6 -- 0 --> S7
    S6 -- 1 --> S8[S8  
b ← 1, rgb ← 100  
p ← 0000]
    S7 -- 0 --> S8
    S7 -- 1 --> S8
    S8 -- 11001 --> S4
    S8 -- ≠ 11001 --> E+C{E+C}
    E+C -- 11001 --> S4
    E+C -- ≠ 11001 --> Exit(( ))
  
```

```

graph TD
    Restn0[Restn=0] --> S1[S1]
    S1 --> E1C[E←C]
    E1C -- 11001 --> NE11001{≠ 11001}
    NE11001 -- 0 --> M[M]
    M -- 1 --> S2[S2]
    S2 --> E2C1[E1 ← -1, scr1 ← 0  
rgb ← 001, p ← 0010]
    E2C1 --> I[I]
    I -- 0 --> E2C1
    I -- 1 --> E2C2[E←C]
    E2C2 -- 11001 --> NE211001{≠ 11001}
    NE211001 --> S3[S3]
    S3 --> E2C2_2[E2 ← -1, scr2 ← 0  
rgb ← 110, p ← 0001]
    E2C2_2 --> Y[Y]
    Y -- 0 --> E2C2_2
    Y -- 11001 --> E2C3[E←C]
    E2C3 --> S1
    E1C -- First TRY --> TRY1[First TRY]
    E2C1 -- Second TRY --> TRY2[Second TRY]
    E2C2_2 -- Last TRY --> TRY3[Last TRY]
    TRY1 --> S1
    TRY2 --> S2
    TRY3 --> S3
  
```

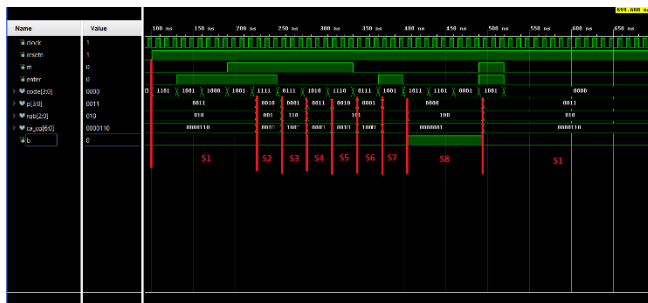
The flowchart illustrates the Dining Philosopher Problem solution using three semaphores (S1, S2, S3) and a 'TRY' state. The initial state is Restn=0. The process starts with S1, followed by E←C (First TRY). If the state is not 11001, it proceeds to M (Second TRY) and then S2. At S2, E1 ← -1, scr1 ← 0, rgb ← 001, p ← 0010. If the state is 0, it loops back to E1 ← -1. If the state is 1, it proceeds to E←C (Last TRY). If the state is not 11001, it proceeds to S3. At S3, E2 ← -1, scr2 ← 0, rgb ← 110, p ← 0001. If the state is 0, it loops back to E2 ← -1. If the state is 11001, it proceeds to E←C, which then loops back to S1.

Two counters and a BCD counter were used in this project. It was decided for the two counters to be 8-second counters in order to prevent debouncing from happening and also create a realistic situation that would be found in the real world. As explained in the finite state machine diagram, these counters acted mainly as components to move from one state to another in the FSM. The BCD counter was also implemented inside the FSM, where a countdown from three to zero appears on the 7-segment LED screen to let the user know that the buzzer is getting activated. As for the decoder, it is also connected to the FSM and its input is the output of the FSM. The decoder converts the output of the FSM into 7-bit data that is shown in the 7-segment LED screen. This input of the decoder is also shown in the FPGA LED's.

For this experiment setup, the hardware that was used was the Nexys A7-100T board, Breadboard, PIR sensor, Active Buzzer, LED's and Wires. The breadboard was used to show the LEDs lighting up during the correct states. On the breadboard was the buzzer, LEDs. When the last attempt is wrong, the buzzer would sound off. The PIR Sensor is used to activate the actual alarm. The PIR Sensor picks up motion and starts looking for 4-bit code inputs from the Nexys A7 board. The wires are used to connect the buzzer on the

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We tried it on the whole project with the buzzer and Nexys A7 100T board. Simply if the simulation worked well and counted exactly as we expected, the sensor caught up with the motion and it started to count. We tried every single case as stated on the FSM. The counter started to count, and the buzzer went off if there is no code or the wrong code is entered. Every number is displayed on the 7-segment display. The link below is the demonstration of the alarm clock showing the result of every case of the FSM and the buzzer goes off:

This final project is a perfect wrap-up for a semester of learning about digital logic design. Making one real alarm clock system develops our skills in VHDL designing and coding. It's a step that lays important groundwork for stepping out in real life. We can make a sensor digital security alarm, and based on that we can also make so many things with sensors such as an automatic door, an automatic light system when it turns off all the lights while detecting no heat motion, and even auto driving for automotive. Most importantly, we want to improve and develop our digital security alarm system. The downside of our system is when the sensor detects motion, we need to hold the button in order to enter the code and reset it. We can switch from holding the button to turning on/off the switch and making it an input. The first four switches are input codes and the fifth switch acts like an enter button. We want to develop more on the alarm in order to use the full capacity if we have more time and the right equipment. The first thing is an on/off button that we want to add. The second thing is a door that acts like a trigger to turn on the alarm. The idea is to use two

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