# **Banner on Seven Segment Displays**

With Scrolling Messages at Different Speeds

Jessica Odish, Alain Sfeir, Randa Odeesh, Victoria Poirier Electrical and Computer Engineering Department School of Engineering and Computer Science Oakland University, Rochester, MI

e-mails: jessicaodish@oakland.edu, alainsfeir@oakland.edu, randaodeesh@oakland.edu, vpoirier@oakland.edu

**Abstract**—The purpose of this project is to construct and design a circuit that will primarily interface all eight seven segment displays on the Basys 3. Using the switches will allow for the banner being shown to display scrolling messages at a constant speed. The user can activate the stop switch to pause on the current pattern being shown across the seven segment displays. The major findings are that the banner on the seven segment displays is accomplished with the use of several hardware components controlled by:

Eight Registers( Chained together to make a shift RAM module),Scroll speed module ,and hex to seven segment decoder.

# I. INTRODUCTION

A circuit in Xilinx Vivado that has a message scroll across eight seven-segment displays should be built in this project. The key idea behind this project is that it uses a clock pulse with a certain light pattern in each of the seven parts. The human eye can be fooled into seeing a message scrolling across seven displays of segments. In the development of this project, the concepts of finite state machines and synchronous circuits taught during the course are extremely useful. Furthermore, it will be useful to create components for laboratory assignments.Because of its performance, this project is useful for all applications shown in seven segment displays, with only one display being turned on out of eight seven segment displays saving energy.

### II. METHODOLOGY

## A. Design

This circuit consists of two counters, a final state maker, eight three-bit shift registers and a 2-to-1 multiplexer, and an 8-to-1 multiplexer. The circuits are often fitted with a tweaked version of the show decoder hex to 7 segments, which is used in previous laboratories to decipher letters rather than integer.. This would give the customer the feeling that several screens are displayed simultaneously.

# B. Implementation

By following our flow chart outline and using assets available. We were able to design the components of our circuit and implement them in our design.

Implementations of early messages were halted by the limiting restrictions caused by using a 7 segment display, we were forced to think of an engaging message that would be readable using a 7 segment display.

### III. EXPERIMENTAL SETUP

Using Vivado, we checked our project behavioral simulation. By building a relevant simulation test bench we could see how the signals were translated and how our design worked prior to writing to the Basys 3 hardware.

### IV. RESULTS

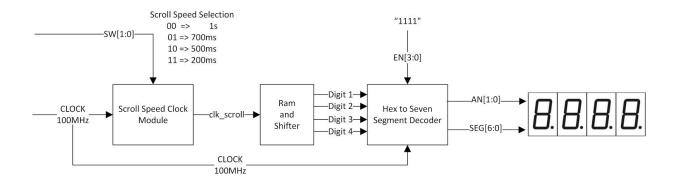
The expected output of the circuit was two messages ("HELLO" and "ECE2700") successfully scrolling across the set of seven-segment displays. These messages could be played at different speeds using switches to set the speed. Some additional features that could be added to this project include adding more registers to the circuit to allow longer messages to be stored.

#### CONCLUSIONS

This project resembled most of the laboratories we operated as a school, allowing us to be more familiarized with the concept as well as give us a better understanding of what it is we want to accomplish. This project enabled us to incorporate a variety of different components we have designed over the whole semester to build our own vision and solve problems before they worked properly.

# References

[1] Llamocca, Daniel. "DIGITAL SYSTEM DESIGN VHDL Coding for FPGAs]." RECRLab, Electrical and Computer Engineering Department, Oakland University, www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html.[2] "Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics." Xilinx.com, Xilinx, Inc., 13 Apr. 2017, www.xilinx.com/support/documentation/data\_sheets/ds181\_Artix\_7\_ Data\_Sheet.pdf



RAMshifter Module Diagram

