LED ASCII Matching Game

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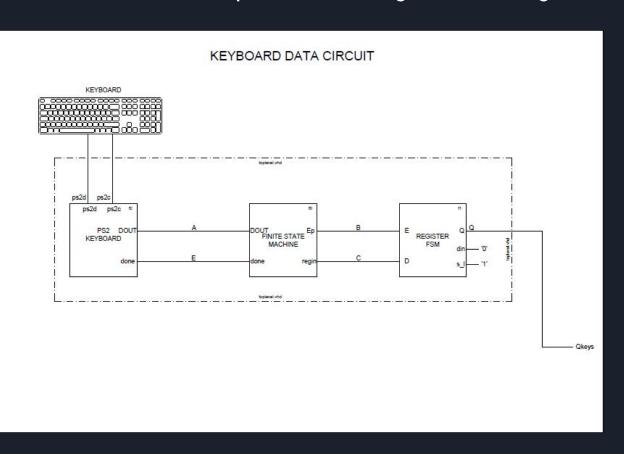
LED Matching Game How to Play

The LED Matching Game consist of an 8 bit random input that lights LEDs on the Nexys4 board. The user has to match the correct input by pressing the right key before the timer runs down.

To limit the options chosen by the 8 bit random number generator the keys that will be used are 0-9 on the keyboard.

If the user presses the correct key the output will be added to a score and displayed on the seven segment display. Then the value will be changed for the user to press another key.

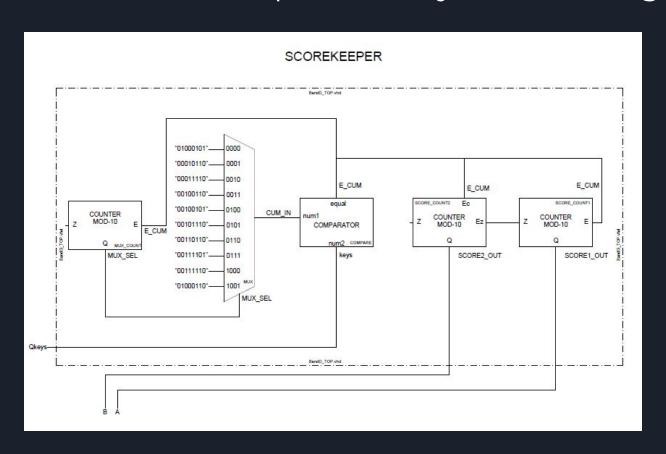
Schematic / Component Layout - Key Data



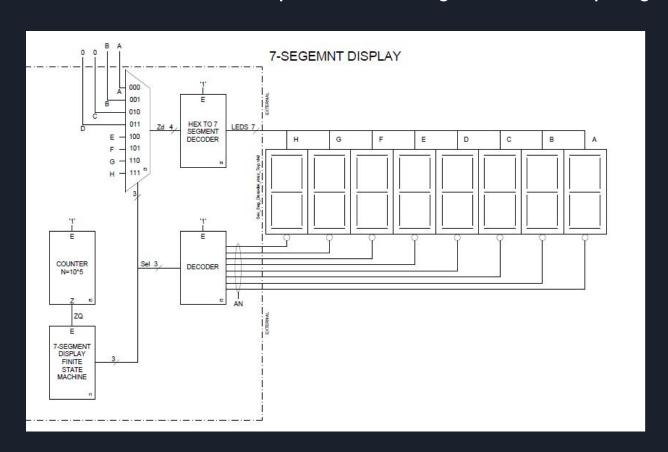
Key Data FSM Code

```
type state is (S1, S2);
    signal y: state;
    signal FCD : std logic vector (7 downto 0);
    begin
    regin <= FCD;
    FCD <= DOUT (7 downto 0);
    transitions: process (resetn, clock, DOUT, done)
    begin
23 Gif resetn = '0' then y <= sl;
            elsif (clock'event and clock = '1') then
25
                case y is
                    when S1 =>
                        if done = '1' and FCD = x"FO" then y <= S2; --FO
                             else y <= S1;
29
                        end if:
30
                    when S2 =>
31
                            if done = '1' then y <= S1;
                                else y <= S2;
33
                        end if:
34
                    end case;
35
            end if:
36
        end process;
37
38
     Outputs: process (y, done)
      begin
      Ep <= '0';
      case y is
        when S1 =>
        when S2 => if done = '1' then Ep <= '1'; end if;
        end case:
     end process;
    end Behavioral;
```

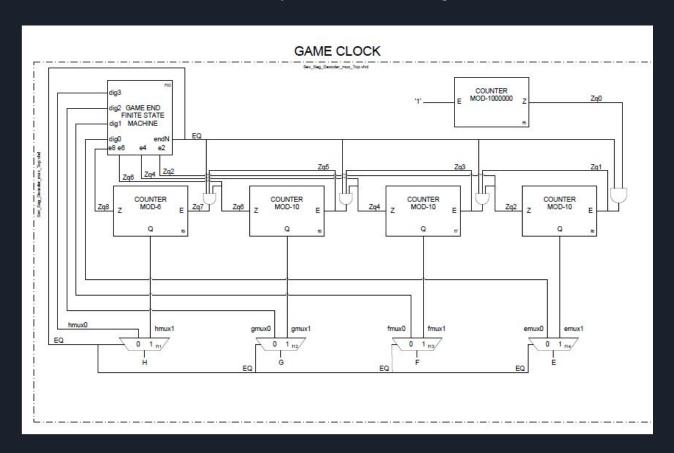
Schematic / Component Layout - Scoring



Schematic / Component Layout - Displays



Schematic / Component Layout - Clock



Code

The code consisted of many digital logic operations that we have learned throughout the semester, including a multiplexer, seven segment display, comparator, and a full 4 bit adder for example. A snippet of the code can be seen below for the comparator:

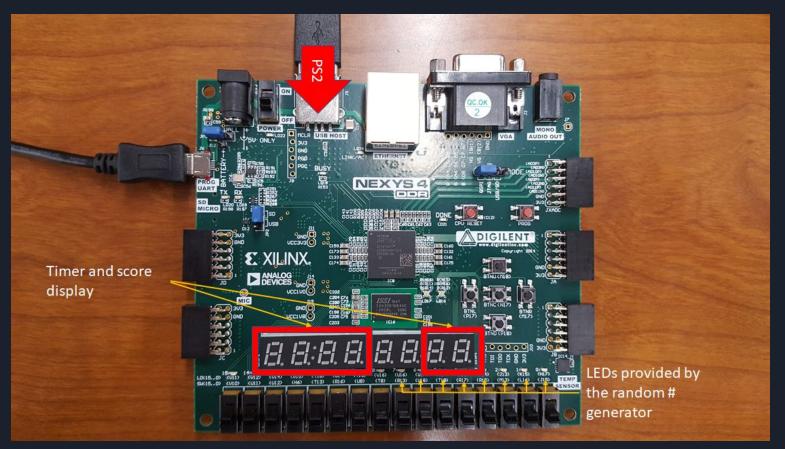
```
architecture Behavioral of COMPARATOR is
    signal clk: std_logic;
    begin
    process(num1,num2)
    begin
        if ( num1 > num2) then
        elsif(num1 < num2) then
        else
        equal <= '1';
        end if;</pre>
```

Code

Here is the code for the game end finite state machine. Once you reach state 5, you can't exit unless the game is reset using the CPU reset button.

```
Transitions: process (resetn, clk, e8, e6, e4, e2, y) -- Definition of State Transitions
20
        begin
21
            if resetn = '0' then --asynchronous clear
                y <= S1; -- Initial State
            elsif (clk'event and clk ='1') then
                case y is
                        if e8 = '1' then v <= S2; else v <= S1; end if; --and e6 = '1' and e4 = '1' and e2 = '1'
                    when S2 =>
                        if e6 = '1' then y <= S3; else y <= S2; end if;
                    when S3 =>
                        if e4 = '1' then y <= S4; else y <= S3; end if;
                    when S4 \Rightarrow
                        if e2 = '1' then y <= S5; else y <= S4; end if;
                    when S5 =>
35
                        --no escape except resetn
                end case;
37
             end if;
39
       end process;
        Outputs: process (y) -- Definition of Outputs Based on State
        begin
43
            endN <= '1':
            case v is
45
                when S1 => endN <= '1':
                when S2 => endN <= '1';
                when S3 => endN <= '1':
                when S4 => endN <= '1';
49
                when S5 => endN <= '0'; dig3 <= "0110"; dig2 <= "0000"; dig1 <= "0000"; dig0 <= "0000";
50
            end case;
        end process;
```

Board layout



Design Difficulties

One design difficulty that was faced was the creation of the random number generator. We first intended to have the numbers randomly generated after each successful button input, but found that it would be quite difficult to implement this into VHDL.

So it was decided to have a random order MUX to the LEDs lighting up, whereas a segment of 10 different numbers would light up in a certain order. This order would then be repeated every time the cycle was completed.

Conclusion

As expected, we made many changes when working throughout the project. Although there were some disagreements, we found a happy medium for the final game. We learned how to communicate with one another and create a project that every member was satisfied with.

Working together as a group allowed us to further our understanding of VHDL and its applications to the real world. The team problem solved through various issues in the project and came out with an entertaining game.

Thank You

Questions and Demonstration

Nexys4 DDR Keyboard:

ESC F1 05	F2 F3 F4 0C	F5 F6 F7 F8 0A	F9 F10 F11 F12 07
TAB Q 0D 15		6 ^ 7 & 8 * 9 (3E 46) Y U I O 44 44	0)
Caps Lock A 58 1C	S D F 28 2B	G H J K 42	L ;: '" Enter 4B 4C 52 ← 5A
	Z X C V 2A	B N M , < 41	>. 49 /? 4A \(\rightarrow \) Shift 59
Ctrl 14	Alt 11	Space 29	Alt Ctrl E0 11

ASCII to binary conversion table:

ASCII Code	Binary Value
0	01000101
1	00010110
2	00011110
3	00100110
4	00100101
5	00101110
6	00110110
7	00111101
8	00111110
9	01000110