RECRLab
Reconfigurable Computing Research Laboratory

IREECE REU Summer Project: High-Performance Architectures for Real-Time Cylinder Pressure Estimation

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Outline

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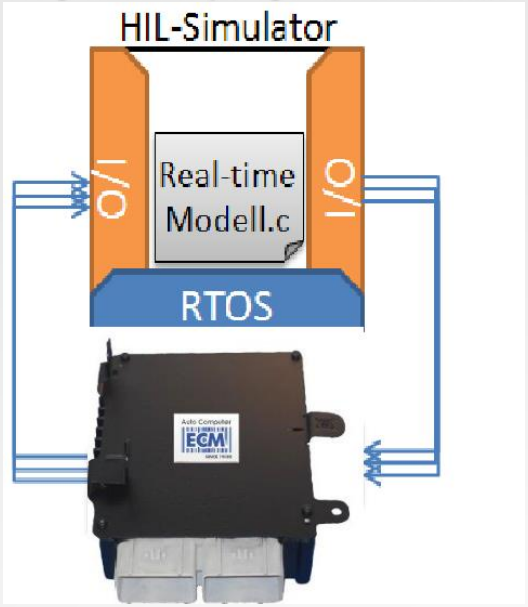
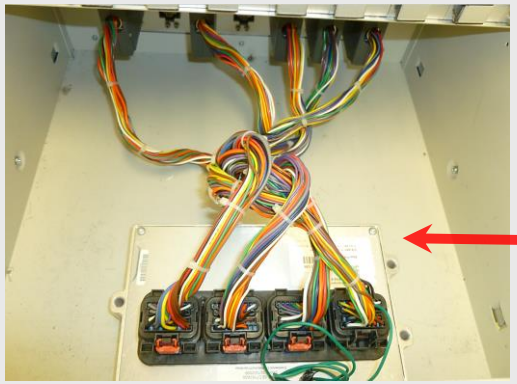
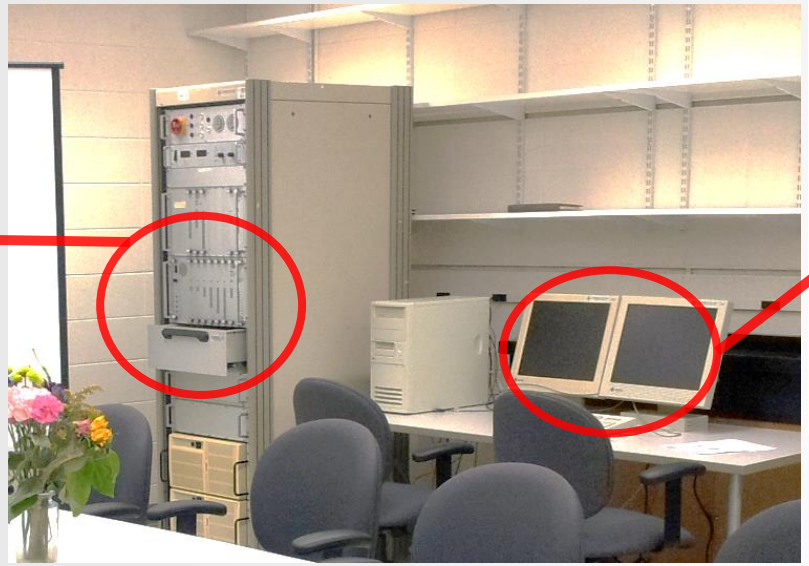
Motivation

- ***Cylinder pressure modeling for Hardware-in-the-loop (HIL) testing.***
  - *Hardware-in-the-loop (HIL) testing is standard practice in automotive industry.*
  - *HIL = Testing of **complex real-time embedded controller** using a mathematical representation (i.e., software model) of the **plant**.*

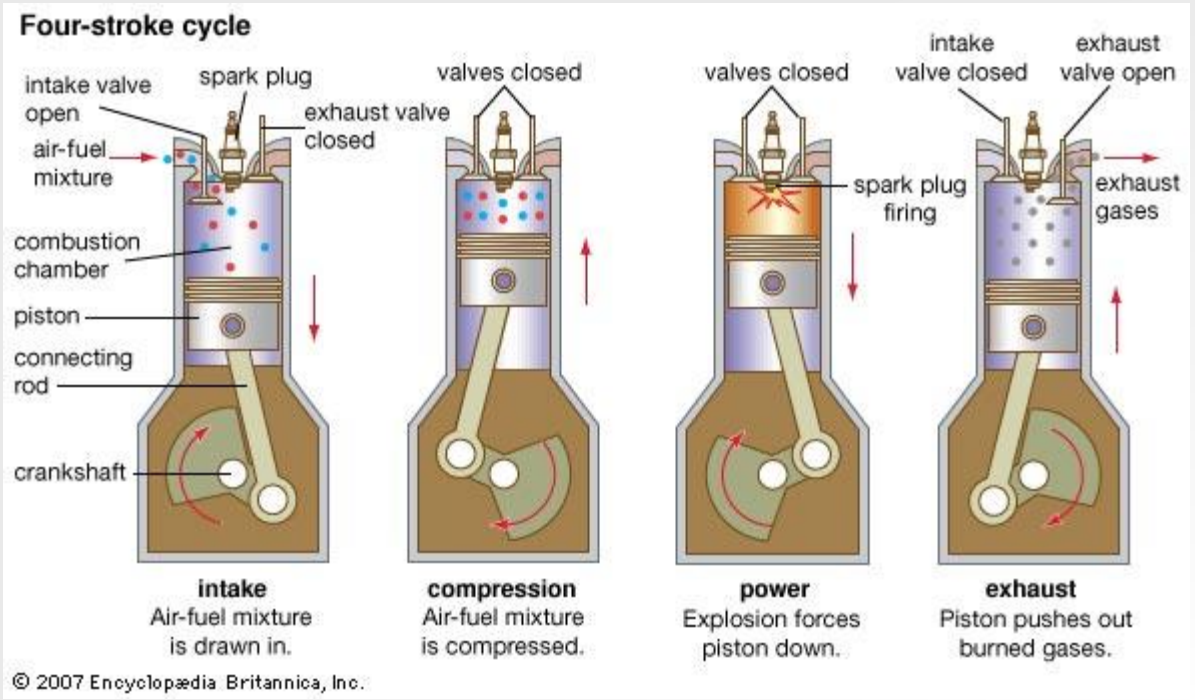






Motivation

- ***Cylinder pressure modeling. Challenges:***
- *Physical models of the combustion event are complex*
- *Current HIL cylinder pressure models are simplistic.*
- *More accurate models (to be developed by ME faculty) need to computed in real-time to work in a HIL setup.*



- ***Problem:*** *Compute accurate pressure estimation every 0.5 degrees.*
  - *RPM range: 500 -9000 rpm. Each crank-angle revolution is 360º.*
  - *For 500-9000 rpm, this means computing every 10 us to 167 us.*

Objectives

- ***Objective 1: Scalable Hardware Implementations of the cylinder pressure model suitable for HIL testing.***
  - *A set of fully-customizable architectures will be implemented. This will allow users to quickly modify design parameters (e.g.: # of input bits, # of iterations, # of processing units).*
  - *High-performance hardware architectures will be achieved by employing techniques that exploit parallelism and pipelining.*
- ***Objective 2: Characterization of the Hardware Architectures***
  - *The fully-customized nature of the architectures will allow us to carry design space exploration, i.e., the creation of a set of different hardware profiles by varying the design parameters. This will help us explore trade-offs among design parameters, accuracy, resources, and execution time.*
- ***Objective 3: Documentation and conference submission***
  - *A conference paper will be submitted based on the implementation aspects of the scalable hardware architectures.*
  - *The documentation and the HDL code of the open-source architectures will be posted in the RECRLab website (hosted by SECS-OU).*

Methodology

- ***Equation – Cylinder Pressure Model:***
  - $h = k \times B^{-0.2} \times p^{0.8} \times T_g^{-0.53} \times v_c^{0.8}$, k: *constant*
  - h: *Instantaneous heat transfer coefficient*
  - B: *cylinder bore diameter* p: *cylinder pressure*
  - T_g: *Gas Temp* v_c: *characteristic velocity*
  - *The equation needs to be executed in real-time (~every 10 us)*
  - *The exponentiation* x^y *takes significant time when executed on traditional embedded microcontrollers.*

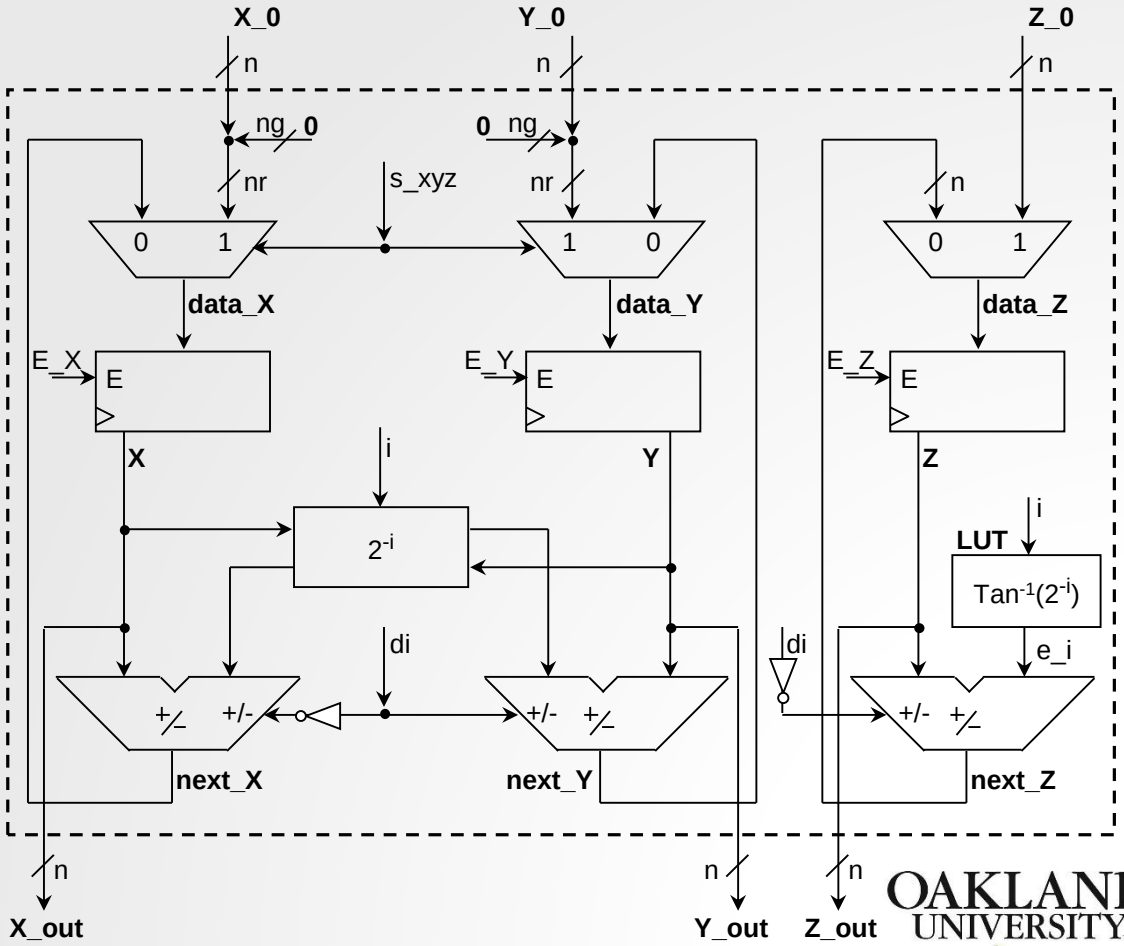
- ***Selection of custom hardware architecture:***
  - *We need to implement the function:* $x^y = e^{y \ln x}$, y: *constant*
  - *Several approaches: Look-up table method, Taylor series, etc.*
  - *The hyperbolic CORDIC (Coordinate Rotation Digital Computer) algorithm is selected to implement the exponentiation and natural logarithm. CORDIC is a shift-and-add algorithm best suited for FPGA/VLSI implementations.*
  - *We will develop a fully parallel and an iterative version.*

Methodology

- *Hyperbolic CORDIC algorithm: i: iteration index (1,2,3,…N)*

$$x_{i+1} = x_i + \delta_i y_i 2^{-i}$$
$$y_{i+1} = y_i + \delta_i x_i 2^{-i}$$
$$z_{i+1} = z_i - \delta_i \theta_i, \theta_i = Tanh^{-1}(2^{-i})$$

- *δ_i=-1,+1 depends on the operation mode (rotation, vectoring) and x_i, y_i, z_i.*
- *By selecting x_0, y_0, z_0 and the oper. mode (rotation, vectoring), we can get various hyperbolic functions (cosh, sinh, exp, ln).*
- *The figure shows an iterative architecture.*
- **Algorithm requires changes to handle larger input domain.*

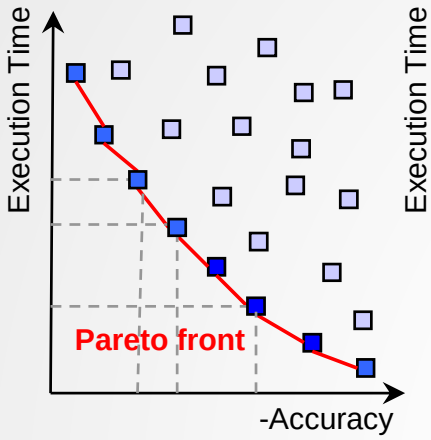


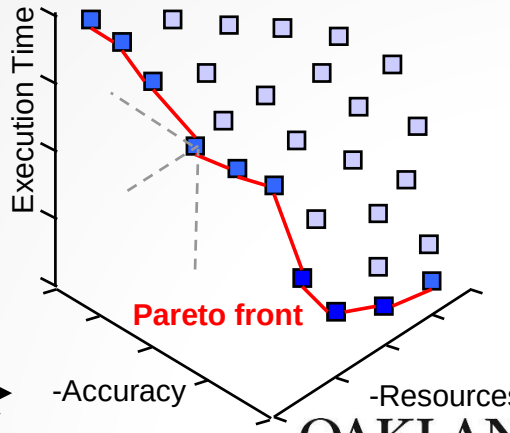
Methodology

- ***Hardware Modeling in MATLAB:***
  - *A model will be developed for both fixed-point arithmetic and single floating-point arithmetic.*

- ***Hardware implementation:***
  - *Parametric VHDL coding of both fully parallel an iterative versions for x^y computation. Definition of design parameters.*
  - *Final multiplication: $h = k \times B^{-0.2} \times p^{0.8} \times T_g^{-0.53} \times v_c^{0.8}$*
  - *Time-accurate hardware simulation.*

- ***Design Space Exploration:***
  - *Example: 2-variable and 3-variable space. Each point is a particular hardware configuration (obtained by a particular set of design parameters)*





Methodology

- ***Hardware verification***
  - *Students will include an external interface (e.g.: UART, USB, Ethernet) in order to feed in and retrieve data from the FPGA.*

- ***Schedule:***
  - *05/26: student describe their projects*
  - *06/01: weekly meeting. 12-1:30 pm at EC-347*
  - *06/08: weekly meeting. 12-1:30 pm at EC-347*
  - *06/15: Midterm presentation (20 min). 12-1:30 pm at EC-347*
  - *06/22: weekly meeting. 12-1:30 pm at EC-347*
  - *06/29: weekly meeting. 12-1:30 pm at EC-347*
  - *07/06: weekly meeting. 12-1:30 pm at EC-347*
  - *07/13: weekly meeting. 12-1:30 pm at EC-347*
  - *07/20: weekly meeting. 12-1:30 pm at EC-347*
  - *07/21: Final poster presentation*

Student Involvement

- ***Student Involvement:***
  - *MATLAB® modeling of the hardware architectures using fixed-point and floating point arithmetic.*
  - *Development of custom hardware for hyperbolic CORDIC. Students will write parametric VHDL code for the scalable hardware architectures.*
  - *Time-accurate simulation.*
  - *Hardware verification using an external interface.*
  - *Design-space exploration. By varying design parameters, students will generate a collection of hardware profiles based on resources, accuracy, and execution time.*
  - *Conference paper preparation and documentation.*

- ***Tools:***
  - *Software: Vivado™ Design Suite – Webpack Edition, MATLAB®*
  - *Hardware: Nexys-4 Development Board.*

Conclusions

- *This is an exciting project that will allow students to apply digital logic concepts on a real-life automotive application.*

- *By the end of this project, students will have learnt: advanced topics in computer arithmetic, development of custom hardware for hyperbolic CORDIC, parametric VHDL coding, synthesis/simulation with Vivado™ software, and communicate the results in a written research paper.*

- *The completed work will open up many new exciting research opportunities: embedded system integration of the developed architectures, analysis of other nonstandard numerical representations (dual fixed point arithmetic), run-time automatic adaptation of hardware resources, etc.*