Daniel Llamocca

RECONFIGURABLE COMPUTING RESEARCH LABORATORY (RECRLAB)
Electrical and Computer Engineering Department
School of Engineering and Computer Science (SECS)
Engineering Center, Room 438
Oakland University, Rochester, MI, 48309
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PRIMARY AREAS OF ACTIVE RESEARCH INTERESTS

- Reconfigurable Computing, High-Performance Embedded Systems.
- High-Performance Architectures for Computer Arithmetic, communications, embedded interfaces, automotive applications, digital video compression (H.264, HEVC), and digital signal/image/video processing.
- Dynamic multi-objective optimization and management of digital systems.
- Run-Time Partial Reconfiguration Techniques on FPGAs.
- Field Programmable Wiring Systems for power, analog, and digital signals.

EDUCATION

Ph.D., Computer Engineering, The University of New Mexico, Albuquerque, May 2012
Dissertation: "Dynamically Reconfigurable Management of Energy, Performance, and Accuracy applied to Digital Signal, Image, and Video Processing Applications"
Advisor: Prof. Marios Pattichis
M.S., Electrical Engineering, The University of New Mexico, Albuquerque, 2008
B.Sc., Electrical Engineering, Pontificia Universidad Católica del Perú, Lima, Peru, 2002

PROFESSIONAL EXPERIENCE

08/2020 – present	Associate Professor, Electrical and Computer Engineering Department Oakland University
08/2014 – 07/2020	Assistant Professor, Electrical and Computer Engineering Department Oakland University
08/2013 – 07/2014	Research Assistant Professor, Dept. of Electrical and Computer Engineering, The University of New Mexico
01/2012 - 07/2013	Post-Doctoral Fellow, Dept. of LLSS, The University of New Mexico.
01/2006 - 12/2011	Graduate Research Assistant, Dept. of Electrical and Computer Engineering, The University of New Mexico.
08/2010 - 12/2010	Internship, K&A Wireless, LLC, Albuquerque.
09/2009 - 10/2009	Internship, Los Alamos National Laboratory, Los Alamos, New Mexico
01/2003 - 12/2005	Teaching Assistant, Dept. of Electrical Engineering, PUCP

AWARDS

2020	Outstanding Teaching Award, School of Engineering and Computer Science (SECS), Oakland University.
2004	Best paper award, "Study of the implementation of speech processing algorithms on FPGAs", *X Workshop IBERCHIP*, Cartagena de Indias, Colombia*, March 2004.*
2000-2002	Undergraduate Scholarship Recipient of 'Fundación Educación' Organization (http://www.fundeducation.org), which supports students in Latin America.

PATENTS

- "System and Methods for Computing 2-D Convolutions and Cross-Correlations", Inventors: Marios S. Pattichis, Cesar Carranza, **Daniel Llamocca**. Int. App. No.: PCT/US2016/067102. Filed Dec. 16, 2016.

- "System and Methods for the computation of the Forward and Inverse Periodic Radon Transform on GPUs and CPUs", Inventors: Marios Pattichis, Cesar Carranza, **Daniel Llamocca**. Int. App. No.: PCT/US2016/067110. Filed Dec. 16, 2016.
- "System and Methods for computing Forward and Inverse Discrete Periodic Radon Transform", Inventors: Cesar Carranza, **Daniel Llamocca**, Marios S. Pattichis, U.S. Patent # 10,049,469. Issued August 14, 2018.
- "System and Methods for Dynamic Management of Hardware Resources", Inventors: Marios S. Pattichis, Yuebing Jiang, and **Daniel Llamocca**, US Patent # 9,111,059, Issued August 18, 2015.

TEACHING

INSTRUCTOR

Electrical and Computer Engineering Department, Oakland University

- Taught the following undergraduate/graduate courses:
  - ✓ High-Performance Embedded Programming. ECE4900/5900 (Fall 2020).
  - ✓ Digital Logic Design. ECE278 (Fall 2016), ECE2700 (Fall 2017, Winter 2018, Fall 2018, Winter 2019, Fall 2019, Winter 2020, Fall 2020).
  - ✓ Reconfigurable Computing. ECE495/595 (Fall 2015, Fall 2016). ECE4900/ECE5900 (Fall 2017, Fall 2018), ECE5736 (Summer 2020).
  - ✓ Computer Hardware Design. ECE378 (Winter 2016, Winter 2017), ECE3710 (Winter 2018, Winter 2019), ECE4710/5710 (Winter 2020).
  - ✓ Senior Design. ECE4999 (Summer 2019).
  - ✓ Design and Analysis of Electromechanical Systems. EGR280 (Winter 2017), EGR2800 (Summer 2018).
  - ✓ Digital Logic and Microprocessor Design. ECE378 (Winter 2015).
  - ✓ Microprocessor-Based System Design. ECE470/570 (Fall 2014).
- Taught the following Continuing Education courses:
  - ✓ Vehicle Networks and Testing (Summer 2019).

Department of Electrical and Computer Engineering, The University of New Mexico

- Taught the following undergraduate courses:
  - ✓ ECE238L, Computer Logic Design, Fall 2013.
  - ✓ ECE314, Signals and Systems, Summer 2013.
- Taught the following workshop:
  - ✓ Digital Circuit Design with VHDL, Fall 2013.

POST-DOCTORAL FELLOW

January 2012 – July 2013

College of Education, The University of New Mexico

- Collaborated in the development of a curriculum for middle-school students that used engineering problems (specifically digital signal, image, and video processing) to motivate and enhance students' understanding of mathematical concepts based on current research that integrates the fields of education and engineering (aolme.unm.edu).
- Developed the required software routines to aid in the teaching of image and video processing using i) MATLAB®, and ii) Python™ with the Raspberry Pi® computer.
- Worked on collaborative proposals to secure external funding.
- Participated in the implementation of the curriculum in an Out-of-School Summer Session (2012), an After-School Spring Session (2013), an Out-of-School Summer Session (2013), and an After-School Spring Session (2014).

TEACHING ASSISTANT, LABORATORY INSTRUCTOR

January 2003 – December 2005

Electrical Engineering Department, Pontificia Universidad Católica del Perú

- Taught the following undergraduate courses: Programming Languages, Digital Circuits, Introduction to Electrical Engineering, Analog Circuits, Electrical Circuits, and Computer Architecture.

BOOKS

- Dean, B.K., **Llamocca, D.**, *"Introduction to Analog & Digital Circuits"*, Dubuque, IA, USA: Kendall Hunt, 2019.

RESEARCH

SPONSORED RESEARCH

- *Oakland University: 2nd Year - Embedded Real Time Programming with the Intel Atom® Platform*. PI: **Daniel Llamocca**, $75,000, Intel Corporation, 09/2019 – 08/2020.
- *Oakland University: Embedded Real Time Programming with the Intel Atom® Platform*. PI: **Daniel Llamocca**, $50,000, Intel Corporation, 09/2018 – 08/2019.
- *Run-Time Reconfigurable Architecture for a SpaceWire Router*. PI: **Daniel Llamocca**, $10,000, Michigan Space Grant Consortium (MSGC), 05/2018 - 12/2018.
- *Self-Reconfigurable Architectures for the Next-Generation Video Compression Standard: HEVC (High Efficiency Video Coding)*. PI: **Daniel Llamocca**, $9,878, University Research Committee - Oakland University, 05/2015 - 07/2015.
- *Excellence in Teaching and Learning - Course Implementation: Reconfigurable Computing*. PI: **Daniel Llamocca**, $3,000, Center for Excellence in Teaching and Learning (CETL) – Oakland University, 05/2015 – 04/2016.
- *CSR: Small: Dynamically Reconfigurable Architectures for Time-varying Image Constraints (DRASTIC) Based on Local Modeling and User Constraint Prediction*. PI: Marios S. Pattichis, Co-PI: **Daniel Llamocca**, $459,870, **NSF** ($68,068 to Oakland University, subaward from the University of New Mexico), 10/2014 - 09/2017.

JOURNAL ARTICLES

1. Losh, M., Llamocca, D., "A Low-Power Spike-like Neural Network Design", *Electronics*, vol. 8, no. 12, Article 1479, December 2019.
2. Llamocca, D., Aloi, D., "Self-Reconfigurable implementation for a Switched Beam Smart Antenna", *Microprocessors and Microsystems,* vol. 60, pp. 1-14, July 2018.
3. Llamocca, D., "Self-Reconfigurable Architectures for HEVC Direct and Inverse Transform", *Journal of Parallel and Distributed Computing*, vol. 109, pp. 178-192, Nov. 2017.
4. Carranza, C., Llamocca, D., and Pattichis, M., "Fast 2D Convolutions and Cross-Correlations using Scalable Architectures", *IEEE Transactions on Image Processing,* vol. 26, no. 5, pp. 2230-2245, May 2017.
5. Carranza, C., Llamocca, D., and Pattichis, M., "Fast and Scalable Computation of the Forward and Inverse Discrete Periodic Radon Transform", *IEEE Transactions on Image Processing*, vol. 25, no. 1, pp. 119-133, January 2016.
6. Murray, V., Pattichis, M., Llamocca, D., and Lyke, J., "Field Programmable Wiring Systems", *Proceedings of the IEEE*, vol. 103, no. 7, pp. 1159-1180, July 2015.
7. Llamocca, D., Pattichis, M., "Dynamic Energy, Performance, and Accuracy Optimization and Management using automatically generated constraints for separable 2-D FIR filtering for digital video processing", *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 7, no. 4, Article 31, December 2014.
8. Llamocca, D., Murray, V., Jiang, Y., Pattichis, M., Lyke, J., and Avery, K., "Scalable Open-Source Architecture for Real-Time Monitoring of Adaptive Wiring Panels", *AIAA Journal of Aerospace Information Systems,* vol. 11, no. 6, pp. 344-358, June 2014.
9. Llamocca, D., Pattichis, M., "A Self-Reconfigurable Platform for the Implementation of 2D Filterbanks with Real and Complex-valued Inputs, Outputs, and Filter Coefficients", *VLSI Design*, vol. 2014, Article ID 651943, 24 pages, May 2014, doi: 10.1155/2014/651943.
10. Celedón-Pattichis, S., LópezLeiva, C.A., Pattichis, M.S., and Llamocca, D., "An interdisciplinary collaboration between computer engineering and mathematics/bilingual education to develop a curriculum for underrepresented middle school students", *Cultural Studies of Science Education*, vol. 8, no. 4, pp. 873-887, December 2013.
11. Murray, V., Llamocca, D., Lyke, J., Avery, K., Jiang, Y., and Pattichis, M., "Cell-based Architecture for Adaptive Wiring Panels: A First Prototype", *AIAA Journal of Aerospace Information Systems,* vol. 10, no. 4, pp. 187-208, April 2013.
12. Llamocca, D., Pattichis, M., "A Dynamically Reconfigurable Pixel Processor System based on Power/Energy-Performance-Accuracy Optimization", *IEEE Transactions on Circuits and Systems for Video Technology,* vol. 23, no. 3, pp. 488-502, March 2013.
13. Llamocca, D., Pattichis, M., and Vera A., "Partial Reconfigurable FIR Filtering system using Distributed Arithmetic", *International Journal of Reconfigurable Computing,* vol. 2010, Article ID 357978, 14 pages, Dec. 2010, doi: 10.1155/2010/367978.
14. Llamocca, D., Agurto, C., "A fixed point implementation of the expanded hyperbolic CORDIC algorithm", *Latin American Applied Research, Special Issue on Programmable Logic*, vol. 37 no.1, pp. 83-91, Bahía Blanca, Argentina, January-March 2007.

CONFERENCE PAPERS

1. Carranza, C., Llamocca, D., Pattichis, D., "Fast and Scalable 2D Convolutions and Cross-Correlations for Processing Image Databases and Videos on CPUs", in *Proceedings of the 2020 IEEE Southwest Symposium on Image Analysis and Interpretation (SSIAI'2020)*, Santa Fe, New Mexico, March 2020.
2. Alaswad, D., Llamocca, D., Gillespie, B., "Towards an Embedded Systems Curricula for the next-generation workforce", in *Proceedings of the 2019 ASEE North Central Section Conference*, Grand Rapids, Michigan, March 2019.
3. Carranza, C., Pattichis, M., Llamocca, D., "Fast and Parallel Computation of the Discrete Periodic Radon Transform on GPUs, multi-core CPUs and FPGAs", in *Proceedings of he 2018 IEEE International Conference on Image Processing (ICIP'2018)*, Athens, Greece, October 2018.
4. Oluwakemi, A., Llamocca, D., Dean, B. K., "Fly-inspired Edge Detection: Architecture and Reconfigurable Embedded Implementation", in *Proceedings of the 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2018)*, Windsor, Canada, August 2018.
5. Wu, J., Jacoby, A., Llamocca, D., Sangeorzan, B., "An Architecture for Real-Time Estimation of Crank-Angle-Resolved Engine Cylinder Pressure", in *Proceedings of the 17th Annual IEEE International Conference on Electro Information Technology (EIT'2018)*, Rochester, Michigan, May 2018.
6. Wu, J., Jacoby, A., Llamocca, D., Sangeorzan, B., "A Model for Crank-Angle-Resolved Engine Cylinder Pressure Estimation", in *Proceedings of the 2018 WCX World Congress Experience*, Detroit, Michigan, April 2018.
7. Jacoby, A., Llamocca, D., "Dynamic Dual Fixed-Point CORDIC Implementation", in *Proceedings of the 24th Reconfigurable Architectures Workshop (RAW'2017)*, Orlando, Florida, May 2017.
8. Jacoby, A., Llamocca, D., "Dual Fixed-Point CORDIC Processor: Architecture and FPGA Implementation", in *Proceedings of the 11th International Conference on Reconfigurable Computing and FPGAs (RECONFIG'2016)*, Cancun, Mexico, Dec. 2016.
9. Llamocca, D., and Aloi, D., "A Reconfigurable Fixed-Point Architecture for Adaptive Beamforming", in *Proceedings of the 23rd Reconfigurable Architectures Workshop (RAW'2016)*, Chicago, Illinois, May 2016.
10. Llamocca, D., "Design and Implementation of a Reconfigurable Computing Course for efficient Hardware/Software Co-Design in Reconfigurable Systems", in *Proceedings of the 2016 ASEE Northeast Section Conference*, Kingston, Rhode Island, April 2016.
11. Mack, J., Bellestri, S., Llamocca, D., "Floating Point CORDIC-based Architecture for Powering Computation", in *Proceedings of the 10th International Conference on Reconfigurable Computing and FPGAs (RECONFIG'2015)*, Mayan Riviera, Mexico, Dec. 2015.
12. Llamocca, D., and Dean, B.K., "A Scalable Pipelined Architecture for Biomimetic Vision Sensors", in *Proceedings of the 25th International Conference on Field Programmable Logic and Applications (FPL'2015)*, London, United Kingdom, Sep. 2015.
13. Carranza, C., Llamocca, D., and Pattichis, M., "A Scalable Architecture for Implementing the Fast Discrete Periodic Radon Transform for Prime Sized Images", *in Proceedings of the 2014 IEEE International Conference on Image Processing (ICIP'2014)*, Paris, France, October 2014.
14. Jiang, Y., Llamocca, D., Pattichis, M., and Esakki, G., "A Unified and Pipelined Hardware Architecture for Implementing Intra Prediction in HEVC", in *Proceedings of the 2014 IEEE Southwest Symposium on Image Analysis and Interpretation*, San Diego, CA, April 2014.
15. Carranza, C., Llamocca, D., and Pattichis, M., "The Fast Discrete Periodic Radon Transform for Prime Sized Images: Algorithm, Architecture, and VLSI/FPGA Implementation", in *Proceedings of the 2014 IEEE Southwest Symposium on Image Analysis and Interpretation*, San Diego, CA, April 2014.
16. Jacoby, A., Llamocca, D., Jordan, R., and Vera, G.A., "Proteus: An Open Source Dynamically Reconfigurable System-on-Chip with applications to Digital Signal Processing", in *Proceedings of the 9th International Caribbean Conference on Devices, Circuits and Systems,* Playa del Carmen, Mexico, April 2014.
17. LópezLeiva, C.A., Celedón-Pattichis, S., Pattichis, M.S., and Llamocca, D., "Image representation in a middle school afterschool program", in *Proceedings of the 4th International Realistic Mathematics Education Conference*, Boulder, Colorado, Sep. 2013.
18. LópezLeiva, C., Celedón-Pattichis, S., Pattichis, M.S., and Llamocca, D., "Successes and challenges of supporting interactive learning in a mathematics and engineering afterschool program for middle school students", in *Proceedings of the 2013 Annual meeting of the American Educational Research Association*, San Francisco, California, April 2013.
19. Llamocca, D., Carranza, C., Pattichis, M., "Dynamic Multiobjective Optimization Management of the Energy-Performance-Accuracy Space for Separable 2-D Complex filters", in *Proceedings of the 22nd International Conference on Field Programmable Logic and Applications* (*FPL'2012)*, Oslo, Norway, Aug. 2012.
20. Llamocca, D., Pattichis, M., Carranza, C., "A framework for self-reconfigurable DCTs based on Multiobjective Optimization of the Power-Performance-Accuracy space", in *Proceedings of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (RECOSOC'2012)*, York, United Kingdom, July 2012.

21. Llamocca, D., Carranza, C., Pattichis, M., "Separable FIR Filtering in FPGA and GPU implementations: Energy, Performance, and Accuracy Considerations", in *Proceedings of the 21st International Conference on Field Programmable Logic and Applications* (*FPL'2011)*, Chania, Greece, Sept. 2011.
22. Murray, V., Llamocca, D., Lyke, J.C., Avery, K., Jiang, Y., and Pattichis, "Cell-based Architecture For Adaptive Wiring Panels: A First Approach", in *Proceedings of the AIAA Reinventing Space Conference*, Los Angeles, CA, May 2011.
23. Steinwart, I., Theiler, J., Llamocca, D., "Using Support Vector Machines for Anomalous change detection", in *Proceedings of the 2010 IEEE International Geoscience and Remote Sensing Symposium,* Honolulu, Hawaii, July 2010.
24. Llamocca, D., Pattichis, M., "Real-time Dynamically Reconfigurable 2-D Filterbanks", *in Proceedings of the 2010 IEEE Southwest Symposium on Image Analysis and Interpretation*, Austin, Texas, May 2010.
25. Llamocca, D., Pattichis, M., Vera, A., Lyke, J., "Dynamic Partial Reconfiguration through Ethernet Link", in *Proceedings of the AIAA Infotech@Aerospace 2010 Conference and Exhibit*, Atlanta, Georgia, April 2010.
26. Llamocca, D., Pattichis, M., Vera, A., "A dynamically reconfigurable platform for Fixed-Point FIR Filters", in *Proceedings of the 2009 International Conference on Reconfigurable Computing and FPGAs (RECONFIG'09)*, Cancun, Mexico, Dec. 2009.
27. Vera, A., Llamocca. D., Pattichis, M., Lyke, J., "A Dynamically Reconfigurable Computing Model for Video Processing Applications", in *Proceedings of the 2009 Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, Nov. 2009.
28. Llamocca, D., Vera, A., Pattichis, M., "A Dynamic Computing Platform for Image and Video Processing Applications", in *Proceedings of the 2009 Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, Nov. 2009.
29. Llamocca, D., Pattichis, M., Vera, A., "A dynamically reconfigurable parallel pixel processing system", in *Proceedings of the 19th International Conference on Field Programmable Logic and Applications* (*FPL'2009)*, Prague, Czech Republic, Sept. 2009.
30. Vera, A., Llamocca, D., Fabula, J., Kemp, W., Marquez, R., Shedd, W., Alexander, D., "Xilinx Virtex V Field Programmable Gate Array Dose Rate Upset Investigations", in *Proceedings of the IEEE Radiation Effects Data Workshop*, Tucson, Arizona, July 2008.
31. Vera, A., Llamocca, D., Pattichis, M., Kemp, W., Sheed, W., Alexander, D., Lyke, J., "Dose Rate Upset Investigations on the Xilinx's Virtex IV Field Programmable Gate Arrays", in *Proceedings of the IEEE Radiation Effects Data Workshop*, Honolulu, Hawaii, July 2007.
32. Llamocca, D., Agurto, C., "A Fixed-point implementation of the expanded hyperbolic CORDIC algorithm", in *Proceedings XII Workshop IBERCHIP*, San Jose, Costa Rica, March 2006.
33. Llamocca, D., Agurto, C., "A Fixed-point implementation of the natural logarithm based on an expanded hyperbolic CORDIC algorithm", in *Proceedings XII Workshop IBERCHIP*, San Jose, Costa Rica, March 2006.
34. Llamocca, D., Crisostomo, P., "An architecture for real-time interaction between an analog radar and a personal computer", in *Proceedings XII Workshop IBERCHIP*, San Jose, Costa Rica, March 2006.
35. Llamocca, D., "A Core design to obtain square root based on a non-restoring algorithm", in *Proceedings XI Workshop IBERCHIP*, Salvador da Bahia, Brazil, March 2005.
36. Llamocca, D., "Implementation of a speech encoder based in the LPC-10 algorithm on a FPGA", in Proceedings ICED/CASTOUR, Veracruz, México, November 2004.
37. Llamocca, D., "Study of the implementation of speech processing algorithms in FPGAs", in Proceedings *X Workshop IBERCHIP*, Cartagena de Indias, Colombia, March 2004 (best paper award).

PRESENTATIONS

- "Instantaneous Cylinder Pressure Estimation", **Fiat Chrysler Automobiles (FCA)**, Auburn Hills, MI, Oct. 30, 2017.
- "Self-Reconfigurable Embedded Systems", **SECS-OU Advisory Board**, Rochester, MI, May 4, 2017.
- "A framework for Run-Time Reconfigurable Computing", **Oakland University**, Rochester, MI, October 24, 2014.
- "Introduction to Digital Logic Design: Stopwatch Design", **California State University-Chico**, Chico, CA, April 2, 2014.
- "Dynamically Reconfigurable Architecture Systems for Time-Varying Image Processing Constraints (DRASTIC) applied to Image Analysis", **California State University-Chico**, Chico, CA, April 2, 2014.
- "Dynamically Reconfigurable Architecture Systems for Time-Varying Image Processing Constraints (DRASTIC) applied to Image Analysis", **Oakland University**, Rochester, MI, March 31, 2014.
- "Dynamically Reconfigurable Architecture Systems for Time-Varying Image Processing Constraints (DRASTIC) applied to Image Analysis", **University of Texas - Pan American**, Edinburg, TX, March 19, 2014.
- "Dynamically Reconfigurable Architecture Systems for Time-Varying Image Processing Constraints (DRASTIC) applied to Image Analysis", **University of Colorado at Colorado Springs**, Colorado Springs, CO, Feb. 19, 2014.
- "A Framework for Dynamically Reconfigurable Architectures", **Lafayette College**, Easton, PA, January 27, 2014

- "Dynamically Reconfigurable Architecture Systems for Time-Varying Image Processing Constraints (DRASTIC) applied to Image Analysis", **University of Michigan-Dearborn**, Dearborn, MI, January 24, 2014.
- "Dynamically Reconfigurable Architectures under Time Varying Constraints", **University of Texas at El Paso**, El Paso, TX, December 11, 2013.
- "A Framework for Dynamic Management of Reconfigurable Architectures under Run-Time constraints", **Texas Tech University**, Lubbock, TX, March 25, 2013.
- "A Method for Optimized Management of Run-Time Reconfigurable Architectures", **Northern Illinois University**, DeKalb, IL, March 5, 2013.
- "Dynamic Management and Optimization of Reconfigurable Architectures under Run-Time Requirements", **San Francisco State University**, San Francisco, CA, Feb. 18, 2013.
- "Stack Frames", **Penn State Erie, The Behrend College**, Erie, PA, Feb. 15, 2013.
- "A Framework for Dynamic Management of Reconfigurable Architectures under Run-Time constraints", **Penn State Erie, The Behrend College**, Erie, PA, Feb. 15, 2013.
- "Dynamically Reconfigurable Computing under Time-varying Constraints", **Ohio Northern University**, Ada, OH, Jan. 23, 2013.

SERVICE

OAKLAND UNIVERSITY SERVICE

- University Senate
  - ✓ Academic Computing Committee: Member (Sep. 2018 – present).

- School of Engineering and Computer Science
  - ✓ Graduate Committee:
    - Chair (Sep. 2019 – present).
    - Member (Sep. 2018 – Sep. 2019).
  - ✓ Executive Committee:
    - Chair (Sep. 2016 – Aug. 2018).
    - Member (Aug. 2014 – Aug. 2016).

- Electrical and Computer Engineering Department:
  - ✓ Graduate Affairs Committee:
    - Chair (Sep. 2018 – present)
    - Member (Sep. 2014 – Aug. 2018).
  - ✓ Computer Engineering Program Committee:
    - Chair (Sep. 2017 – present)
    - Member (Sep. 2014 – Aug. 2017)

- IEEE @ Oakland University – Student Branch: Faculty Advisor (March 2016 – August 2019)

THESIS AND DISSERTATION COMMITTEES

Master Theses

- Oluwakemi Noro Adabonyan, M. Sc. Embedded Systems (OU), "Field Programmable Gate Array Implementation of a Fly Eye Sensor for Edge Detection", defended on March 9th, 2018. Chair: **Daniel Llamocca**.
- Lakshmi Padmaja Angaluru Venkata, M. Sc. Embedded Systems (OU), "HEVC Encoder: Software implementation and Embedded System Design for Transform and Scaling", defended on March 3rd, 2016. Chair: **Daniel Llamocca**.
- Ayomide Yusuf, M. Sc. Embedded Systems (OU), "GPU Implementation for Robust Lane Tracking in Self Driving Cars", defended on March 1, 2019. Chair: Shadi Alawneh.
- Gangadharan Esakki, M.S. Computer Engineering (UNM), "Dynamic Switching of GOP Configurations in High Efficiency Video Coding (HEVC) with Relational Databases for Multi-objective Optimization", defended on July 14, 2014. Chair: Prof. Marios Pattichis.

Doctoral Dissertations

- Jason Gorski, Ph. D. in Systems Engineering (OU), "The FPOA, A Medium-Grained Reconfigurable Architecture for High-Level Synthesis", defended on September 5th, 2018. Chair: Prof. Darrin Hanna.
- Bryant Jones, Ph. D. Electrical and Computer Engineering (OU), "Automatic Cache Partitioning Method for High-Level Synthesis", defended on March 9th, 2018. Chair: Prof. Darrin Hanna.

- Tri P. Doan, Ph. D. Electrical and Computer Engineering (OU), "CAN Crypto Chip to Secure Data Transmitted through CAN FD Bus by using AES-128 & SHA-1 with a symmetric key", defended on March 9th, 2017. Chair: Prof. Subramaniam Ganesan.
- Cesar Carranza, Ph.D., Computer Engineering (UNM), "Fast and Scalable Computation of the Forward and Inverse Discrete Periodic Radon Transform", defended on December 17, 2015. Chair: Prof. Marios Pattichis.

REVIEWER: JOURNALS AND CONFERENCES

- IEEE Transactions on Signal Processing
- Microprocessors and Microsystems Journal
- Circuits, Systems and Signal Processing Journal
- IET Circuits, Devices & Systems
- IEEE Transactions on Image Processing (2010 - present)
- IEEE Transactions on Circuits and Systems Part II: Express Briefs (2013 - present)
- IEEE Transactions on Industrial Informatics (2014 - present)
- Journal of Circuits, Systems, and Computers (JCSC) (2014 - present)
- Measurement - Journal of the International Measurement Confederation (2013 - present)
- IEEE International Conference on Image Processing (2013 - present)
- IEEE International Conference on BioInformatics and BioEngineering (2012 - present)

PROFESSIONAL MEMBERSHIPS

- Institute of Electrical and Electronics Engineers (IEEE), Senior Member
- IEEE Circuits and Systems Society
- Society of Automotive Engineers (SAE)

MISCELLANEOUS

GRADUATE STUDENT ASSOCIATION (GSA) - TREASURER

June 2008 – June 2009

Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, NM.

- Organized social activities and provided graduate students with funds for dissertation defense, conference travel, etc.

LANGUAGES

- Native Spanish speaker, fluent in English.

SELECTED RESEARCH PROJECTS

- ADAPTIVE WIRING PANEL FOR SPACE APPLICATIONS — August 2010 - December 2011
  Department of Electrical and Computer Engineering, The University of New Mexico
  - ✓ Design of an Adaptive Wiring Panel that can route power, analog, and digital signal through an array of solid state relays. This was an Airforce Research Labs (AFRL) project.
  - ✓ Development of a command-line software interface for the Adaptive Wiring Panel. The software utilized graph algorithms to perform optimized usage of the relays based on a user-defined circuit to implement.
  - ✓ Mechanical design of the prototypes as well as the layout of the hardware components. Three prototypes were designed and successfully tested.
  - ✓ Design of an array of Printed Circuit Board (PCB) layouts for the Adaptive Wiring Panel. Each PCB contained an FPGA, a set of solid state relays, and ancillary components.

- HIGH-PERFORMANCE MEDICAL IMAGING VISUALIZATION SYSTEM — August 2010 - December 2010
  K & A Wireless LLC, Albuquerque, NM.
  - ✓ Implementation of an image processing algorithm (MATLAB platform) that counts objects inside a box for medical purposes (Phase I SBIR) using segmentation, morphology, and filtering.
  - ✓ Assessment of the resource and memory requirements for the implementation of the algorithm inside an embedded microprocessor.
  - ✓ Result were included in a Phase II SBIR Proposal, which was eventually granted.

- GPU IMPLEMENTATION OF A SUPPORT VECTOR MACHINE (SVM) — September 2009 - October 2009
  Los Alamos National Laboratory, Los Alamos, NM.

- ✓ Implementation of a Support Vector Machine (testing) for Anomalous Change Detection on an array of Graphic Processing Units (GPU).
- ✓ Platform used: C++ for CUDA under a Linux environment.
- ✓ The GPU implementation resulted in a twenty-fold improvement in execution time compared to a multi-threaded CPU implementation.

REFERENCES

1. Marios Pattichis – Former Academic Advisor
   Full Professor
   Department of Electrical and Computer Engineering, MSC01 1100, 1 University of New Mexico, ECE Bldg., Room 229A, Albuquerque, NM, 87131
   email: pattichis@ece.unm.edu

2. Ingo Steinwart
   Full Professor
   Institute for Stochastics and Applications, Department of Mathematics,
   University of Stuttgart
   email: Ingo.Steinwart@mathematik.uni-stuttgart.de

3. Ramiro Jordán - Director of ECE-UNM Undergraduate Program
   Associate Professor
   Department of Electrical and Computer Engineering, MSC01 1100, 1 University of New Mexico, Albuquerque, NM, 87131.
   email: rjordan@ece.unm.edu

4. Carlos López-Leiva
   Assistant Professor
   College of Education, 1 University of New Mexico, Albuquerque, NM, 87131
   email: callopez@unm.edu

5. Alonzo Vera
   Configurable Space Microsystems Innovations & Applications Center (COSMIAC)
   2350 Alamo Ave. SE, Suite 100, Albuquerque, NM, 87106
   email: alonzo@ieee.org

6. Jorge Piovesan
   K&A Wireless, LLC
   2617 Juan Tabo Blvd. NE, Suite A, Albuquerque, NM 87112
   email: jpiovesan@ka-wireless.com