# *Simple Calculator with LCD*

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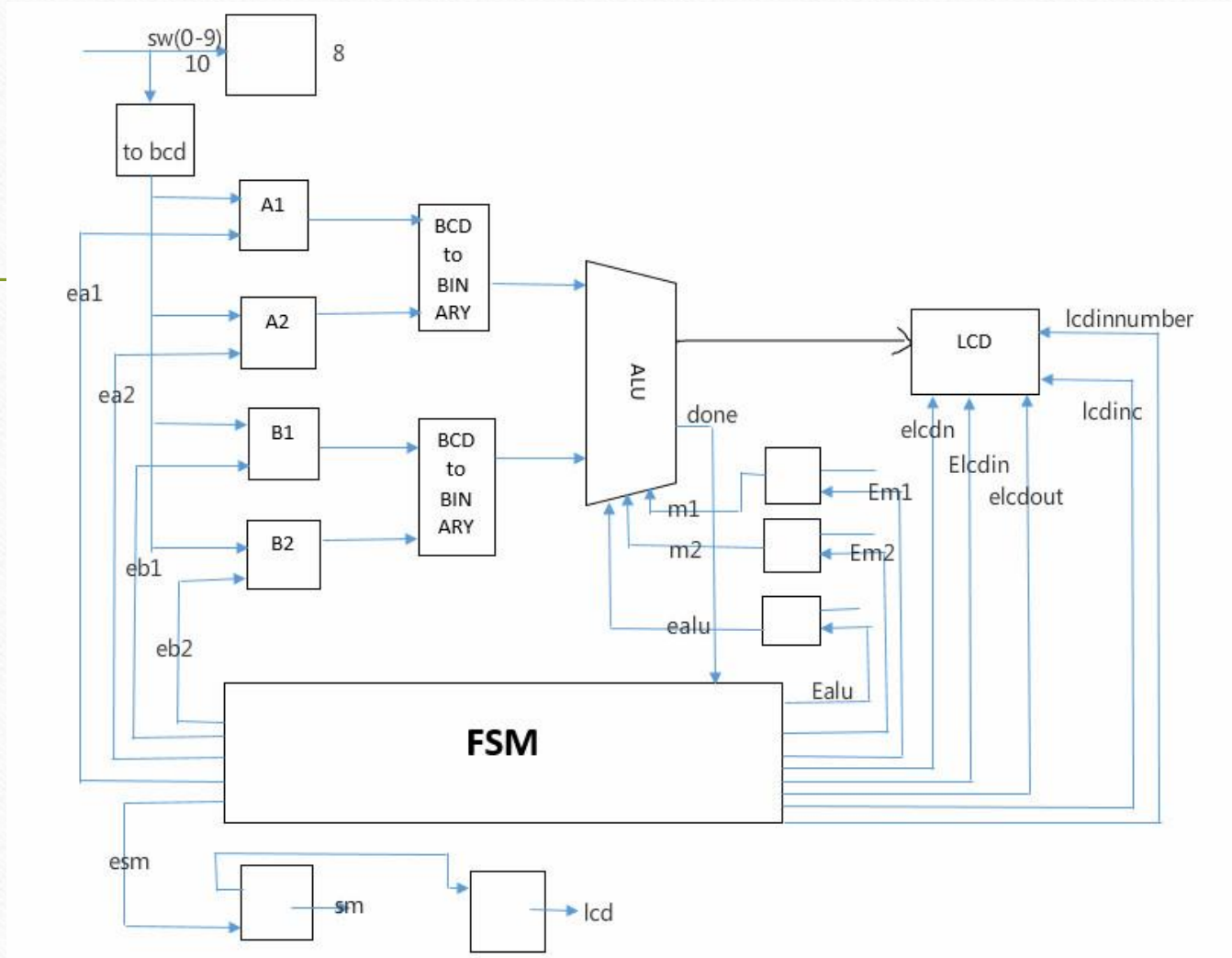
# *Modules*

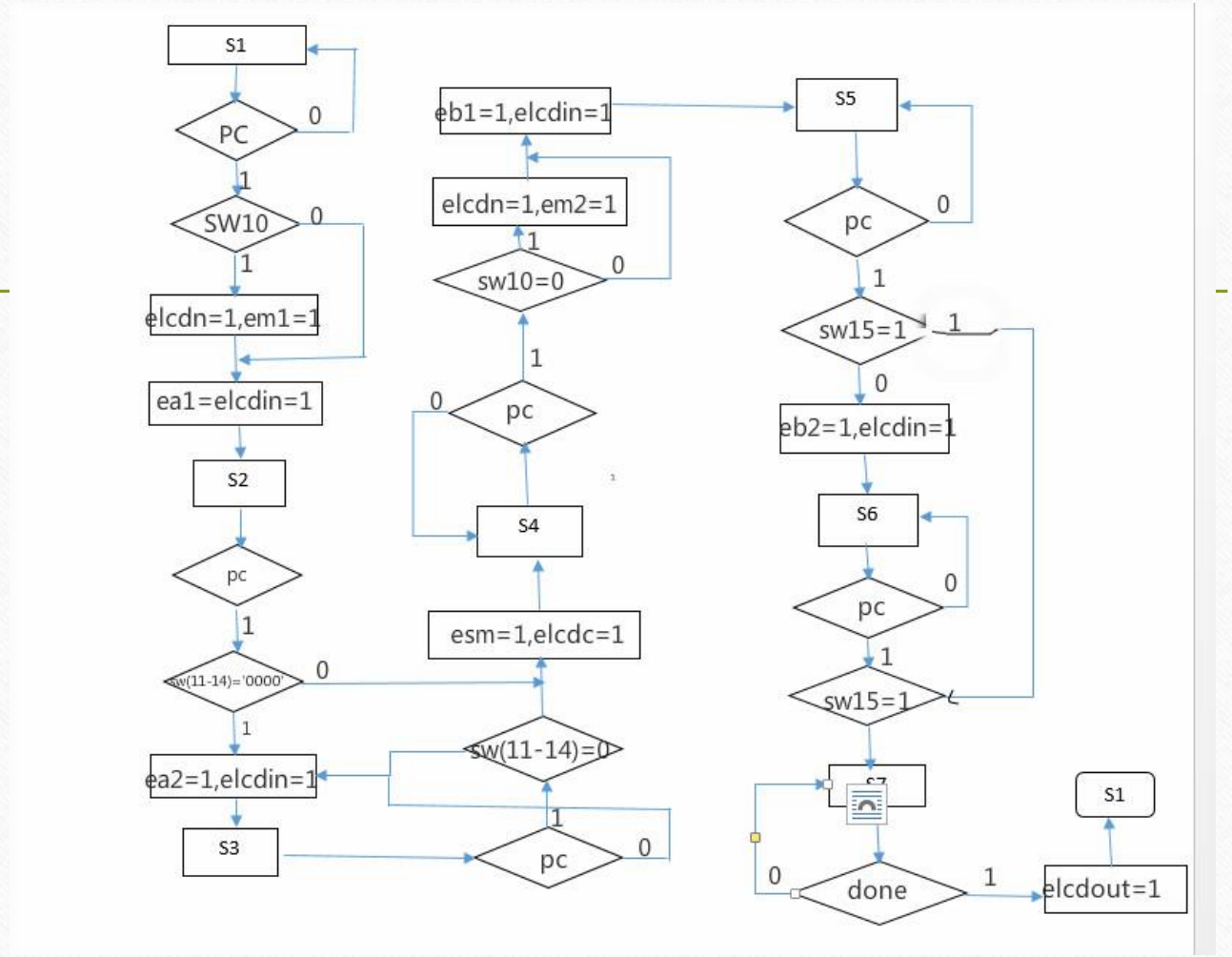
- Control Module.
- Add/Subtract Module.
- Multiply Module.
- Divide Module.
- Operations between signed numbers.

# SYSTEM

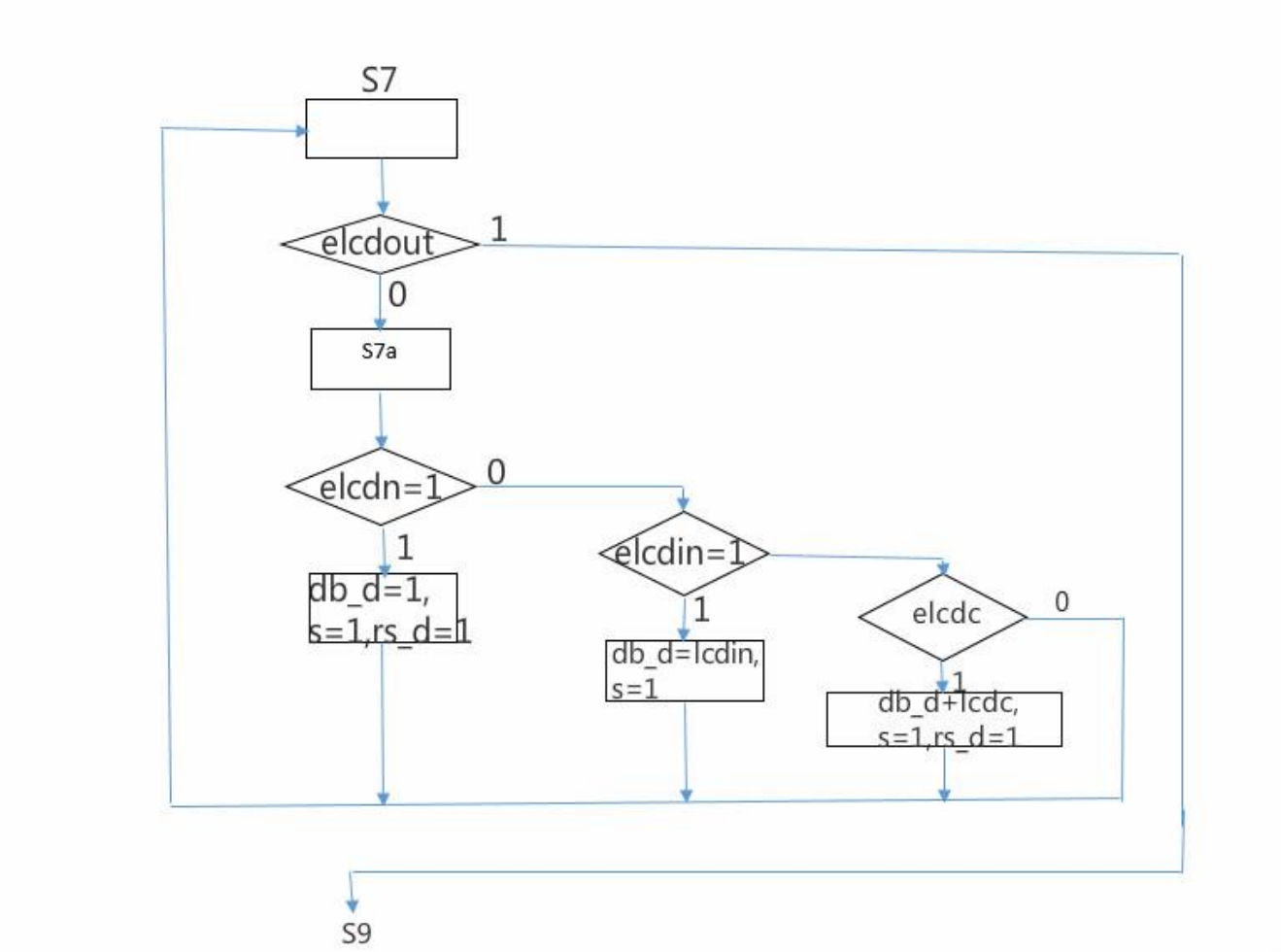
IN → BCD → Binary → ALU → Binary → BCD → Ascii



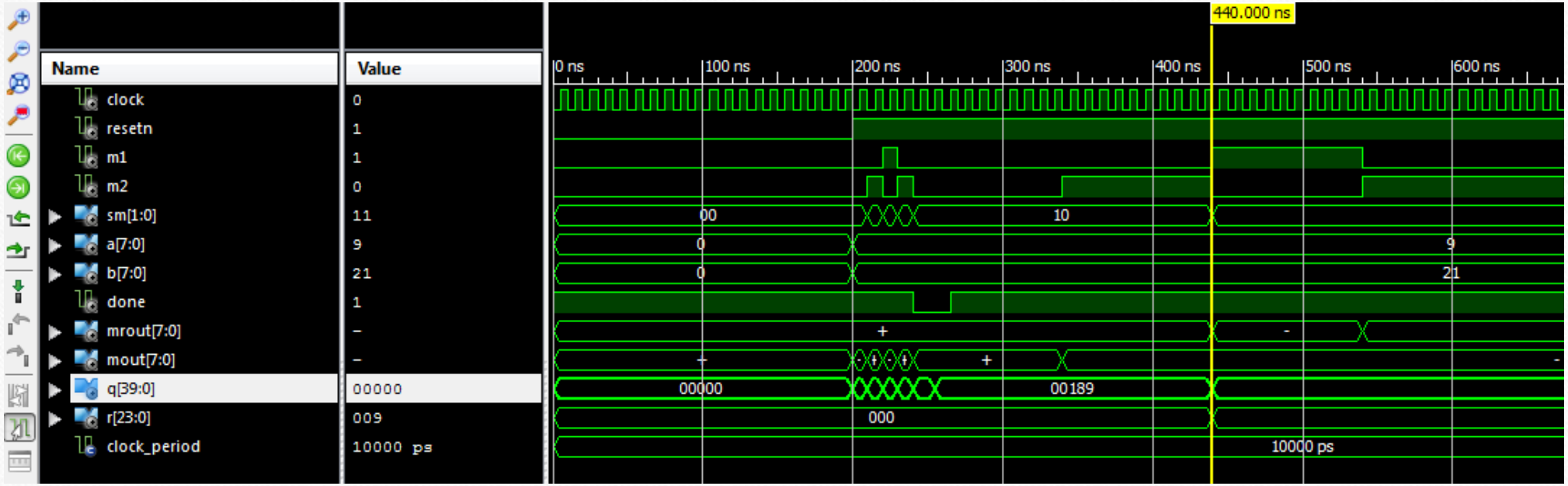
# FSM


S1
PC
0
1
SW10
0
1
elcdn=1,em1=1
ea1=elcdin=1
S2
pc
1
sw(11-14)='0000'
0
1
ea2=1,elcdin=1
S3
eb1=1,elcdin=1
elcdn=1,em2=1
1
sw10=0
0
1
0
pc
S4
esm=1,elcdc=1
sw(11-14)=0
1
pc
0
S5
pc
0
1
sw15=1
1
0
eb2=1,elcdin=1
S6
pc
0
1
sw15=1
0
done
1
S1
elcdout=1

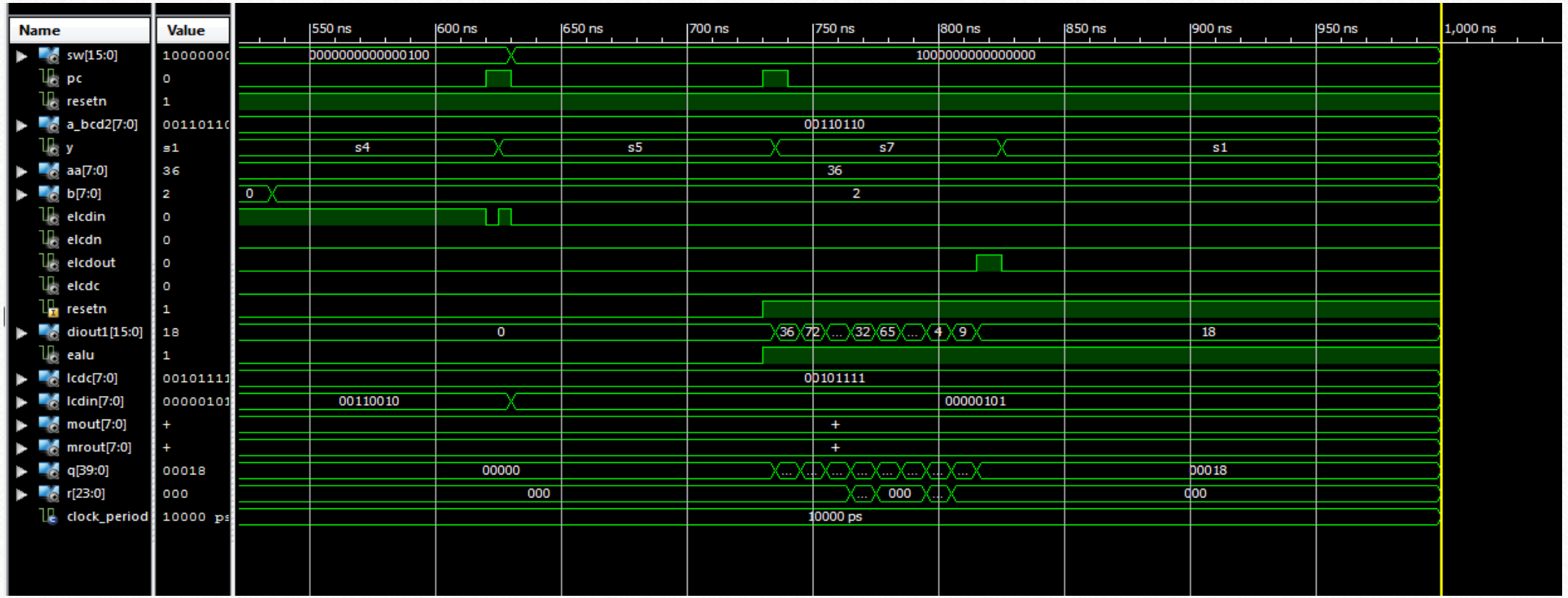
# FSM (lcd)


S7
elcdout
1
0
S7a
elcdn=1
0
1
db_d=1,
s=1,rs_d=1
elcdin=1
1
db_d=lcdin,
s=1
elcdc
0
1
db_d+lcdc,
s=1,rs_d=1
S9

# Functional Simulation

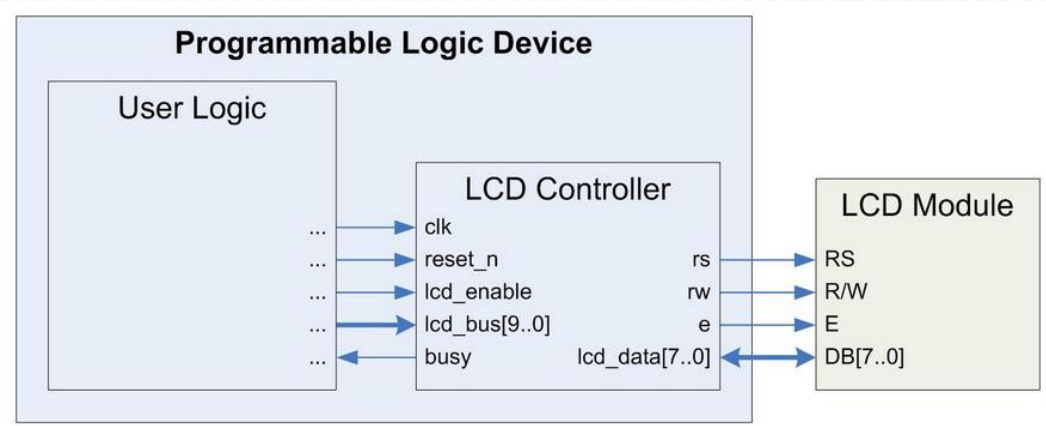


# Functional Simulation

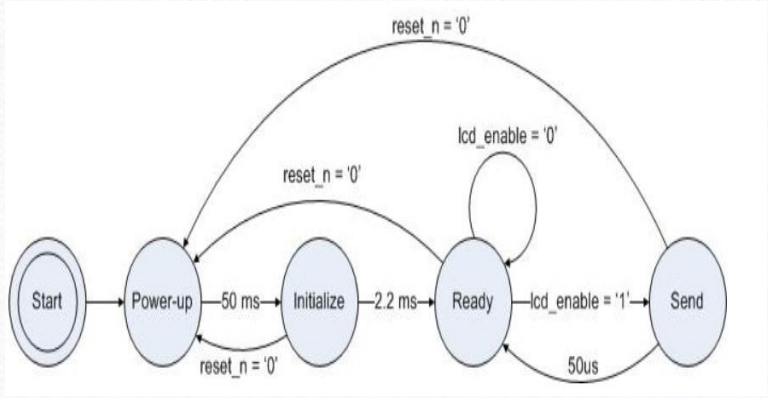


# *LCD Controller Implementation in PLD*

This LCD controller is a VHDL component for use in CPLDs and FPGAs. The controller manages the initialization and data flow to HD44780 compatible 8-bit interface character LCD modules. It was primarily developed pursuant to the Lumex LCD General Information datasheet. This example VHDL component allows simple LCD integration into practically any programmable logic application. Figure 1 depicts the controller implemented to interface between an LCD module and a user's custom logic.



# *LCD Controller State Machine*




The LCD controller state machine consists of five states. Upon startup, it immediately enters the Power-up state, where it waits 50ms to ensure the supply voltage has stabilized. It then proceeds to an Initialize state. The controller cycles the LCD through its initialization sequence, setting the LCD's parameters to default values defined in the hardware. This process completes in approximately 2.2ms, and the controller subsequently assumes a Ready state. It waits in this state until the lcd-enable input is asserted, then advances to the Send state. Here, it communicates the appropriate information to the LCD, as defined by the lcd-bus input. After 50us, it returns to the Ready state until further notice. If a low logic level is applied to the resetn input at any time for a minimum of one clock cycle, the controller resets to the Power-up state and re-initializes. Figure 2 illustrates the LCD controller state machine.