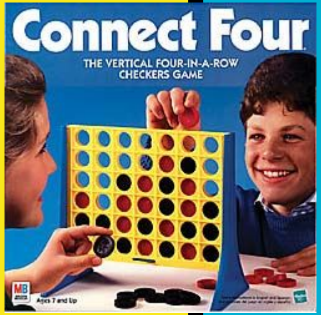
Connect Four

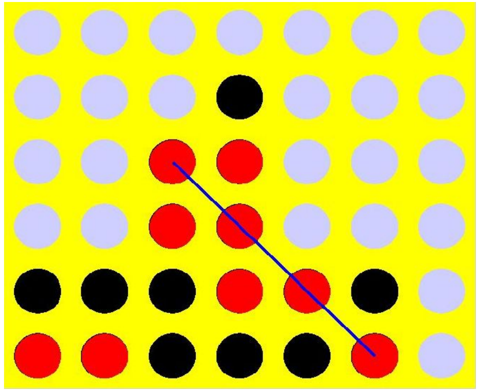
Kyle Johannes
Diana Szeto
James Vankoevering
Kevin Weinert



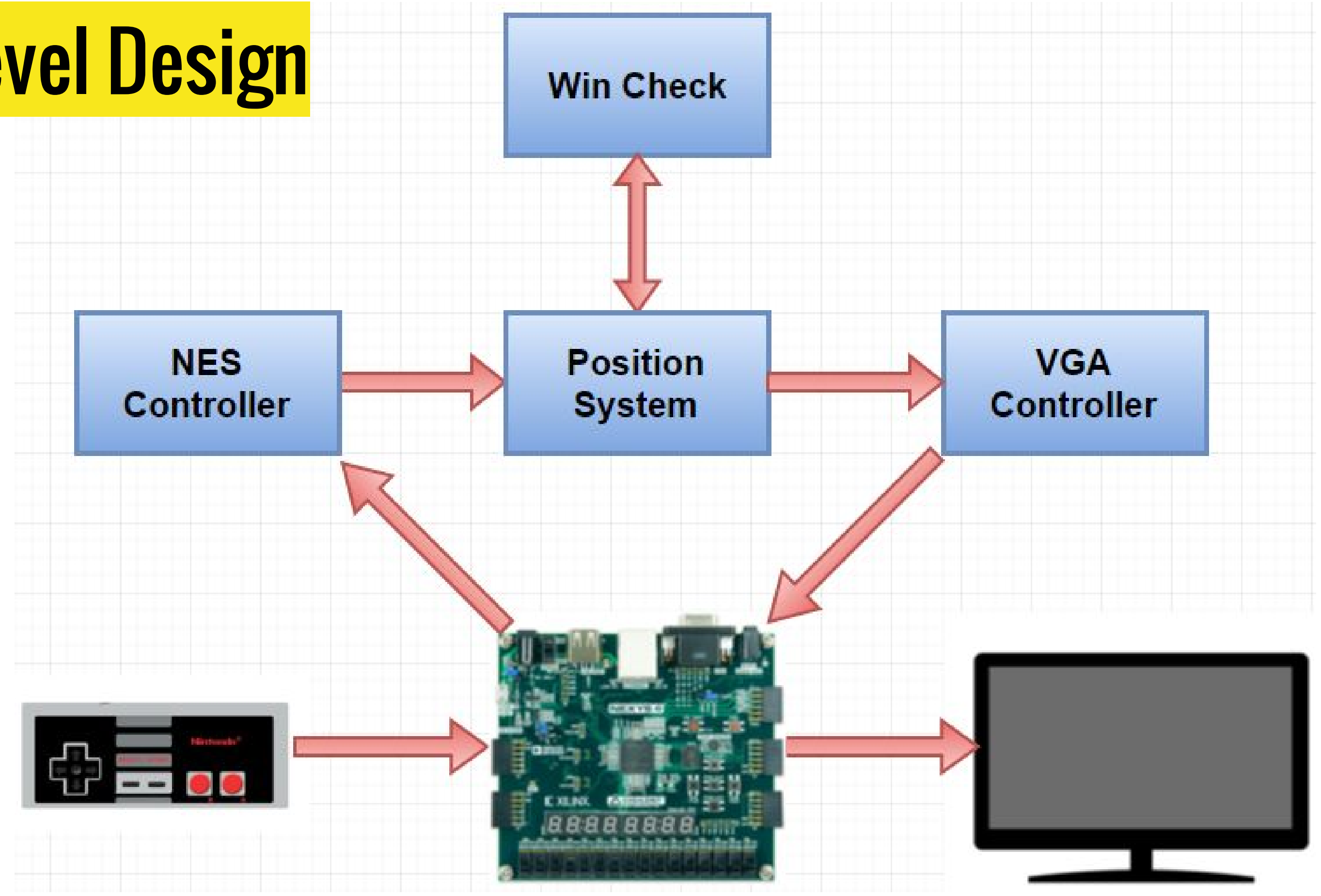
ECE 378 Winter 2016
Final Project
Instructor: Daniel Llamocca

Gameplay

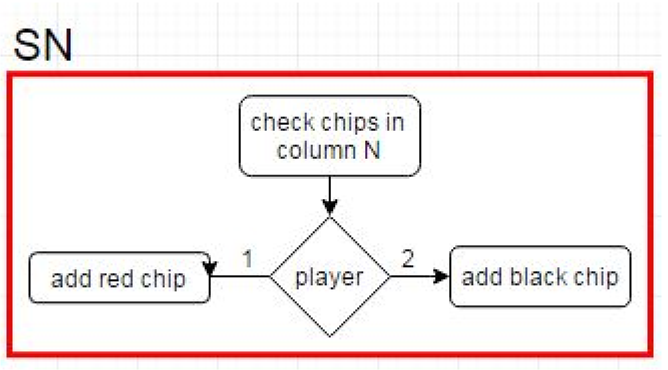
- Connect Four is a classic two-player game.
- The game board has 7 columns and 6 rows, allowing for 42 possible chip slot locations.
- Each player chooses one of two chip colors.
  - In our design, Player 1 is red while Player 2 is black.
- The players take turns dropping one chip into a column at a time.
- The objective of the game is to connect four of your own chips in a row before your opponent.
- The winning four-in-a-row can be vertical, horizontal, or diagonal.
- When a player wins, the board is cleared before beginning the next round.

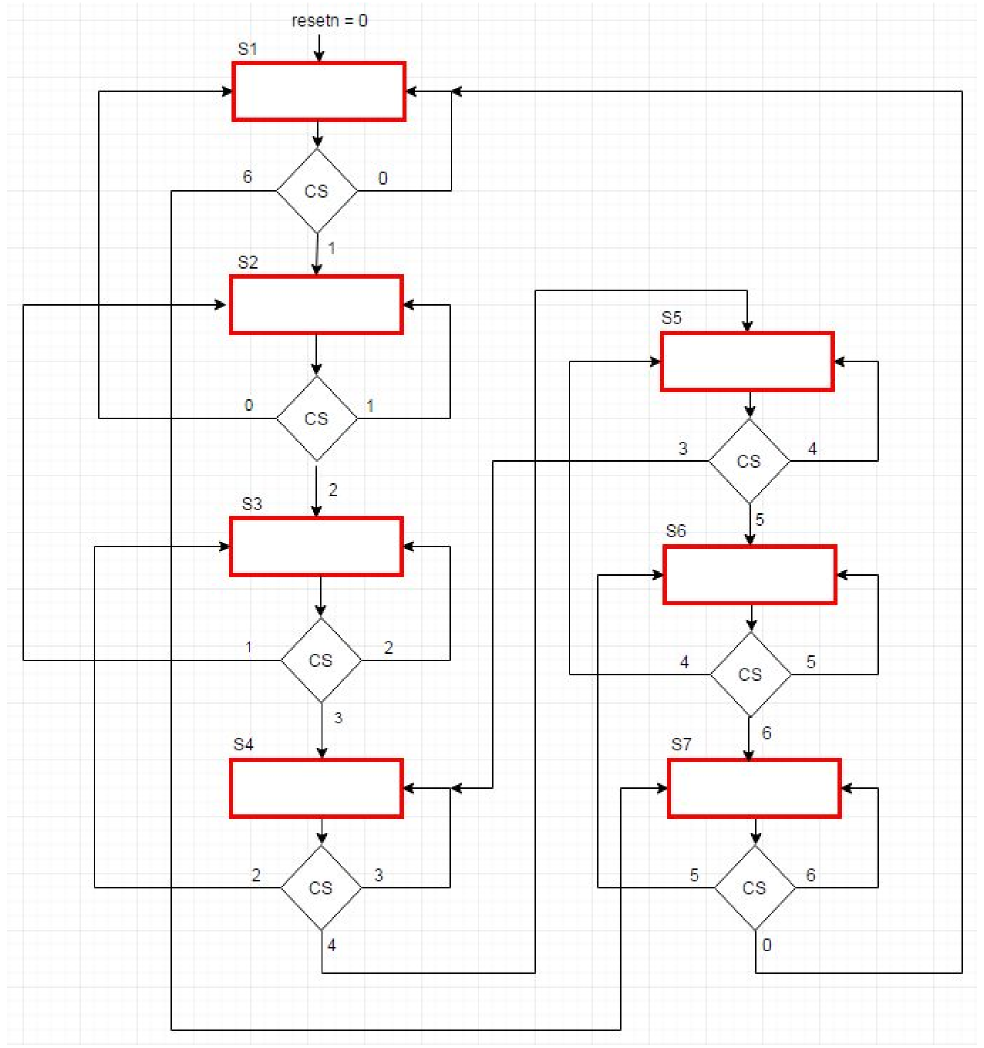


Top Level Design



Position System

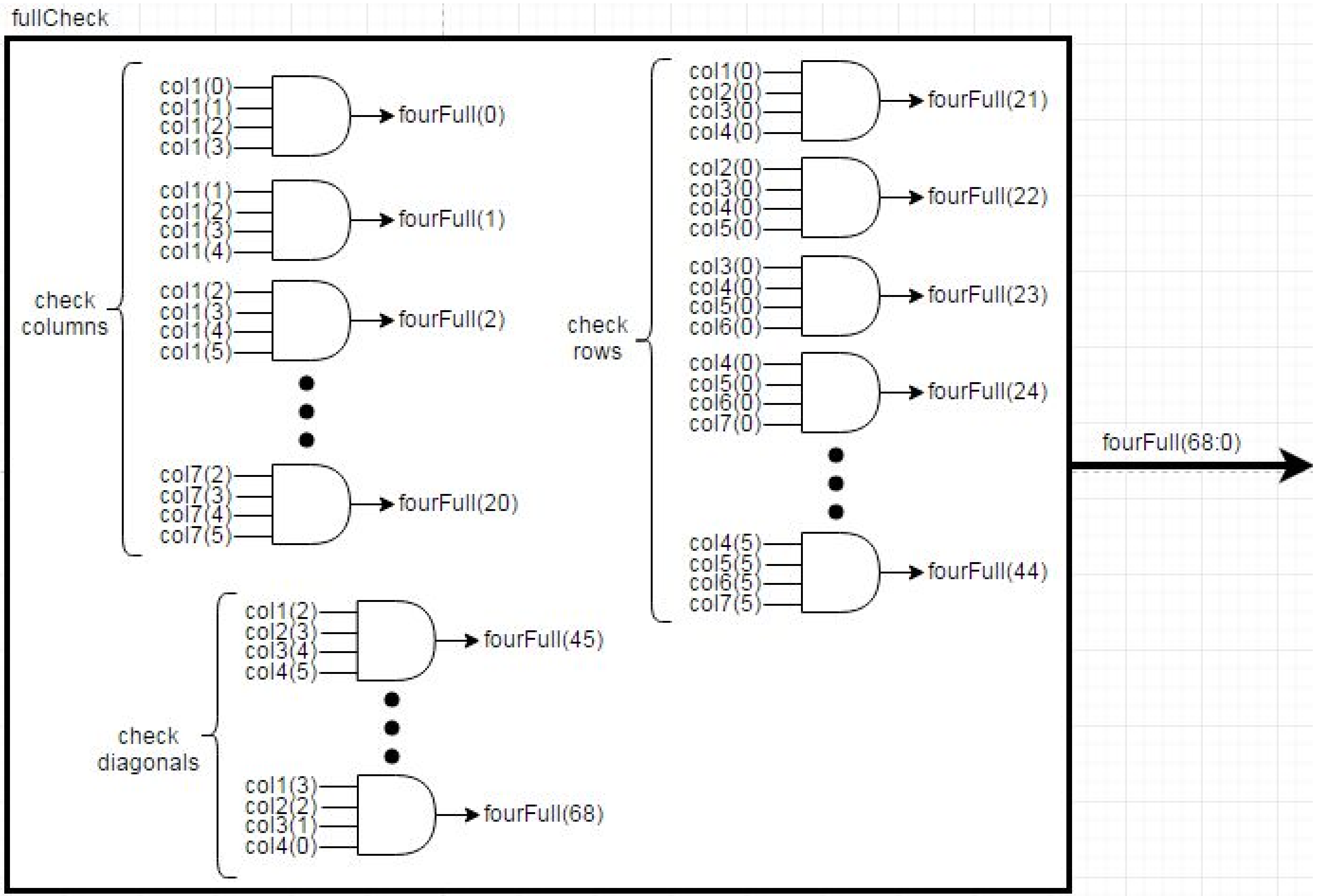




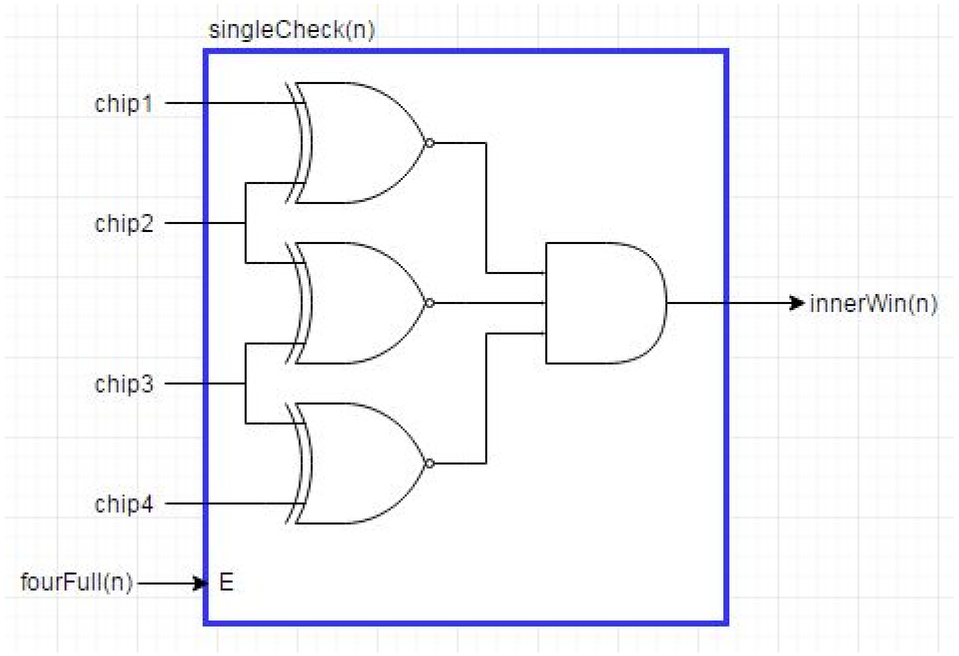
Win Check

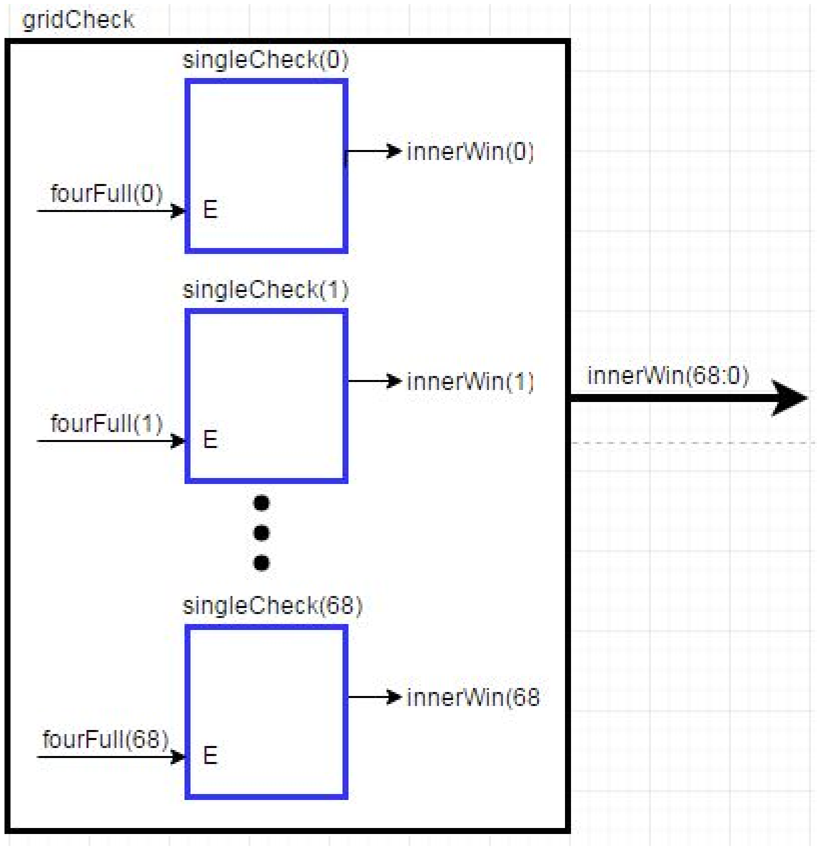
- The Win Check system is made of three main components.
- fullCheck.vhd checks if four adjacent slots in the board are occupied. Outputs a signal that specifies which combinations of four adjacent slots are occupied.
- gridCheck.vhd checks if any four adjacent slots in the board are occupied by the same players chip. Uses singleCheck.vhd to accomplish this. Takes input from the fullCheck.vhd as an enable for the singleCheck.vhd. Outputs a win signal if a player has won, by combining win signals from singleCheck.vhd components.
- singleCheck.vhd checks if the four specified input chips are of the same color. Enabled if four adjacent slots are occupied, the chips in those slots are input. Outputs a win signal if the four chips are the same color.

Win Check

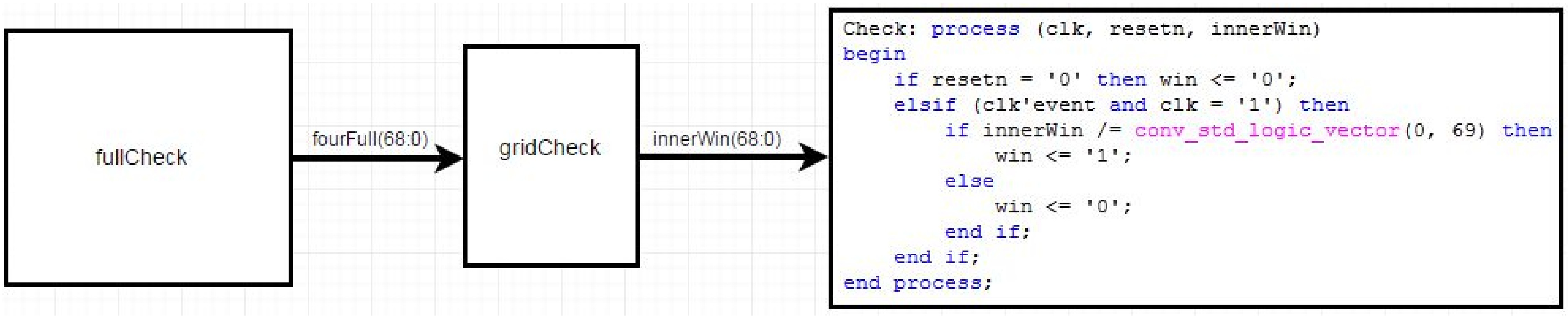

fullCheck
check columns
col1(0)
col1(1)
col1(2)
col1(3)
fourFull(0)
col1(1)
col1(2)
col1(3)
col1(4)
fourFull(1)
col1(2)
col1(3)
col1(4)
col1(5)
fourFull(2)
col7(2)
col7(3)
col7(4)
col7(5)
fourFull(20)
check rows
col1(0)
col2(0)
col3(0)
col4(0)
fourFull(21)
col2(0)
col3(0)
col4(0)
col5(0)
fourFull(22)
col3(0)
col4(0)
col5(0)
col6(0)
fourFull(23)
col4(0)
col5(0)
col6(0)
col7(0)
fourFull(24)
col4(5)
col5(5)
col6(5)
col7(5)
fourFull(44)
check diagonals
col1(2)
col2(3)
col3(4)
col4(5)
fourFull(45)
col1(3)
col2(2)
col3(1)
col4(0)
fourFull(68)
fourFull(68:0)

Win Check


singleCheck(n)
chip1
chip2
chip3
chip4
fourFull(n)
E
innerWin(n)


gridCheck
singleCheck(0)
fourFull(0)
E
innerWin(0)
singleCheck(1)
fourFull(1)
E
innerWin(1)
innerWin(68:0)
singleCheck(68)
fourFull(68)
E
innerWin(68

Win Check



```
Check: process (clk, resetn, innerWin)
begin
    if resetn = '0' then win <= '0';
    elsif (clk'event and clk = '1') then
        if innerWin /= conv_std_logic_vector(0, 69) then
            win <= '1';
        else
            win <= '0';
        end if;
    end if;
end process;
```

NES Controller

Hardware:

CD4021 parallel to serial shift register
 -buttons are pull-downs, register reads button state on latch
 -shifts data out serially

3 data lines: latch, clock, and data out

- Latch loads parallel data in

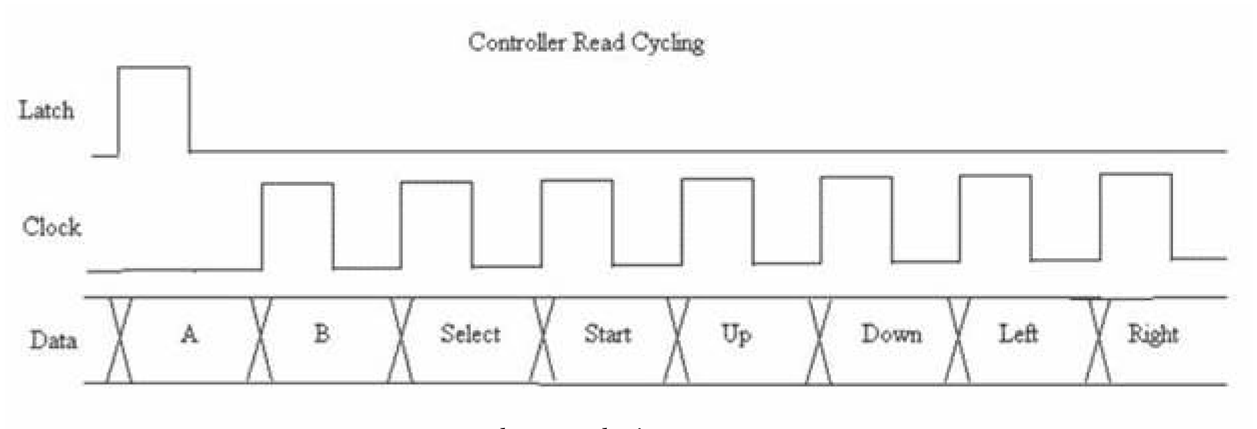


Image source: http://seb.riot.org/nescontr/

NES Controller

VHDL:

- Clock divider
  - Controller clock runs at 400 Hz, divided from 100MHz system clock
- Shift register
  - Receives serial data and reassembles as parallel
- Output register
  - Once data is shifted completely, the parallel output is stored in an output register until needed
- Timing state machine
  - Controller latch timing, output register latching
- “Button press” state machine
  - Looks for signal transitions, outputs based on button being pressed and released

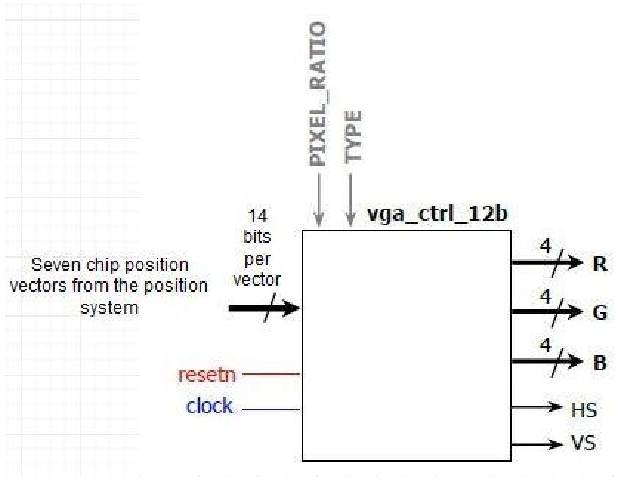
NES Controller

Diagram:

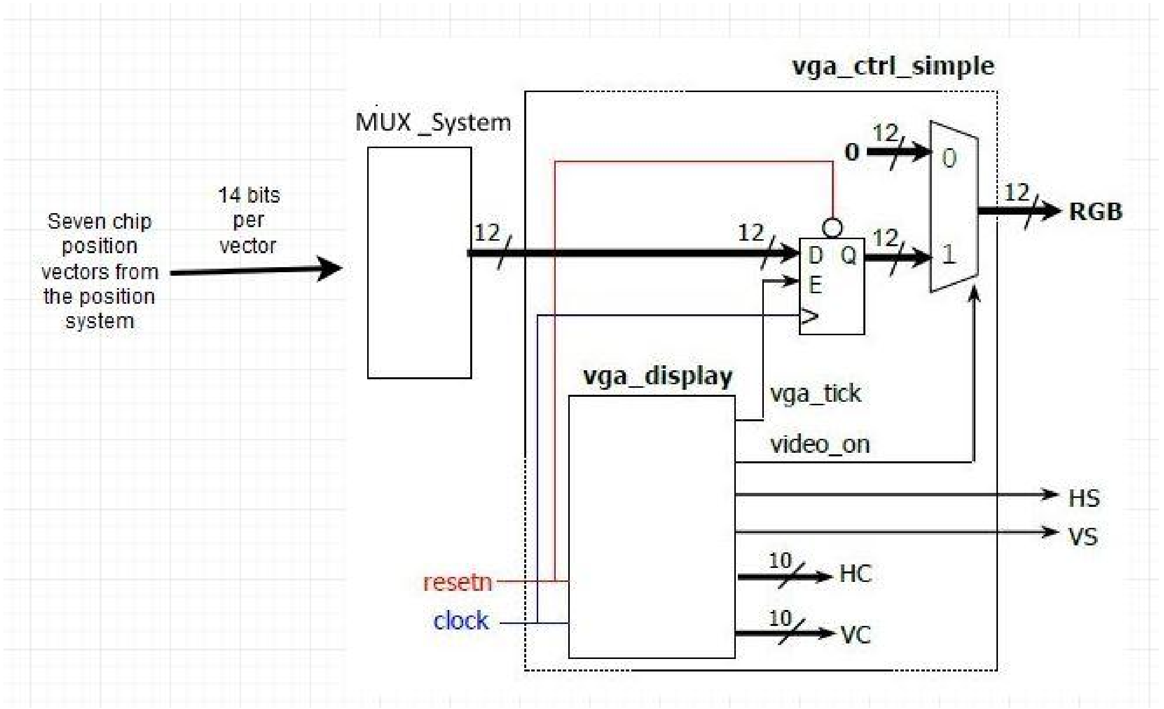
VGA Controller

- VGA screen used to display game board to players.
- VGA controller and state machine code from Professor Llamocca was used.
- A circuit was added to choose the color to display based on the values of HC and VC.
- That circuit used a decoder and multiple MUX to select the input for a particular region on the screen.
- Colors of the chips, whether Red, Black, or Blank were also chosen by a smaller MUX.

VGA Controller



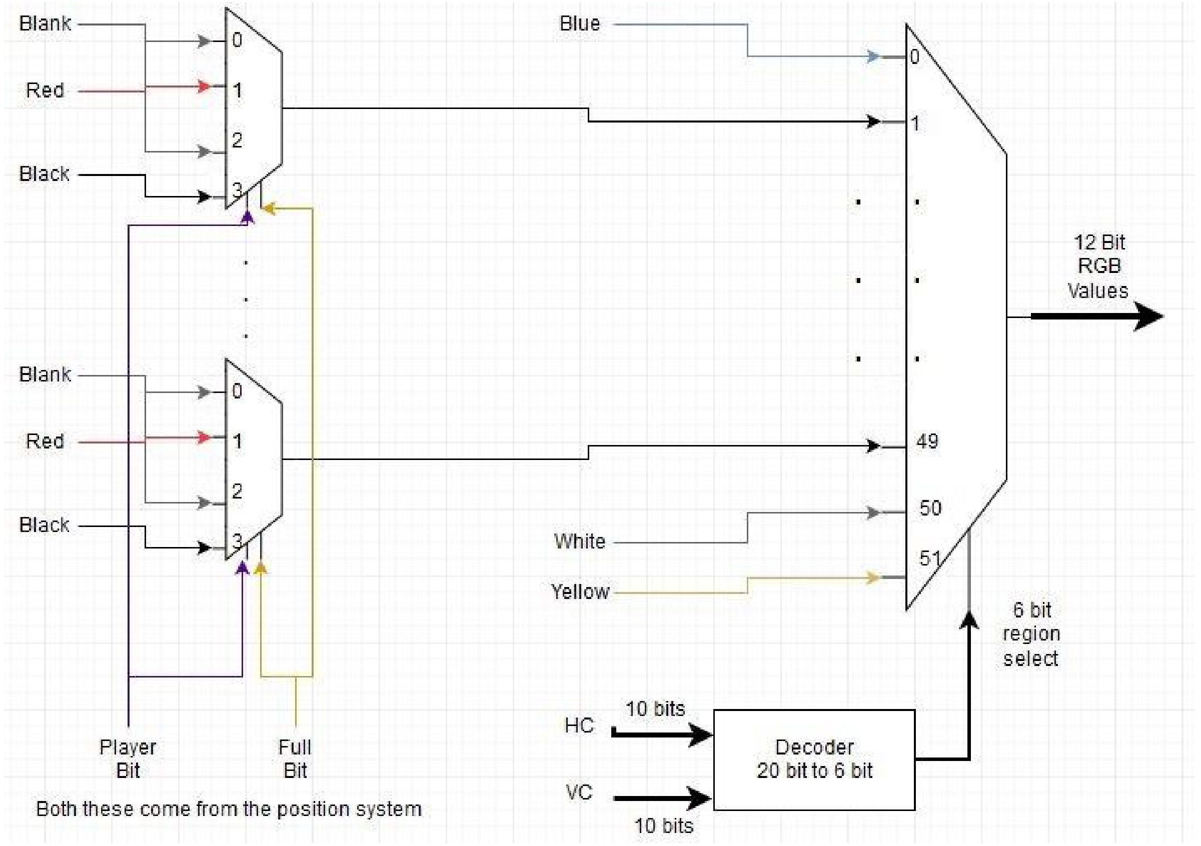
Top level of VGA controller



Internal circuits of the VGA controller

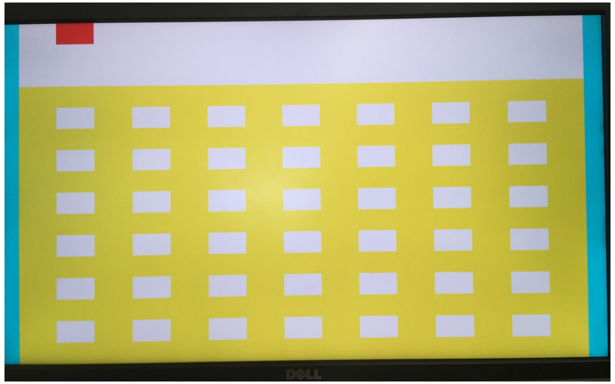
VGA Controller

Multiplexer system designed to determine which color the VGA needs to display based on the region of the display. Color names shown were encoded as standard logic vectors in the VHDL code. The blank chip space color was white.



Gameplay Pictures

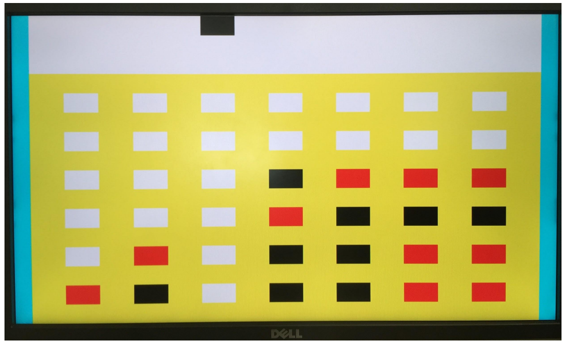
1.



Game start.

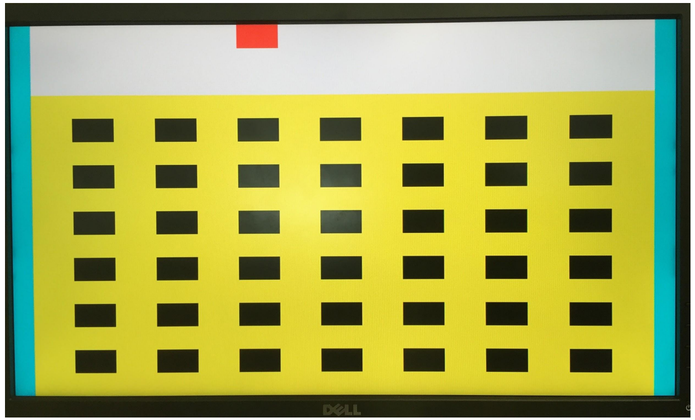
Player 1's turn.

2.

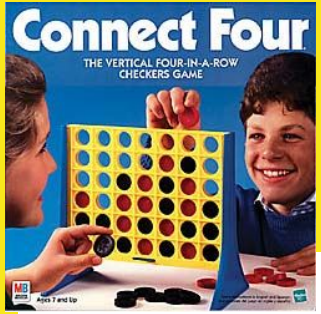
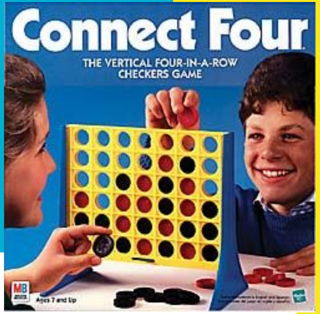


A few turns...

3.



Player 2 wins!


Connect Four
THE VERTICAL FOUR-IN-A-ROW CHECKERS GAME

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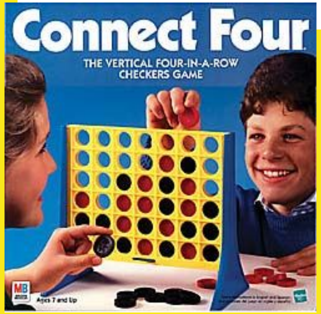
Wanna Play?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