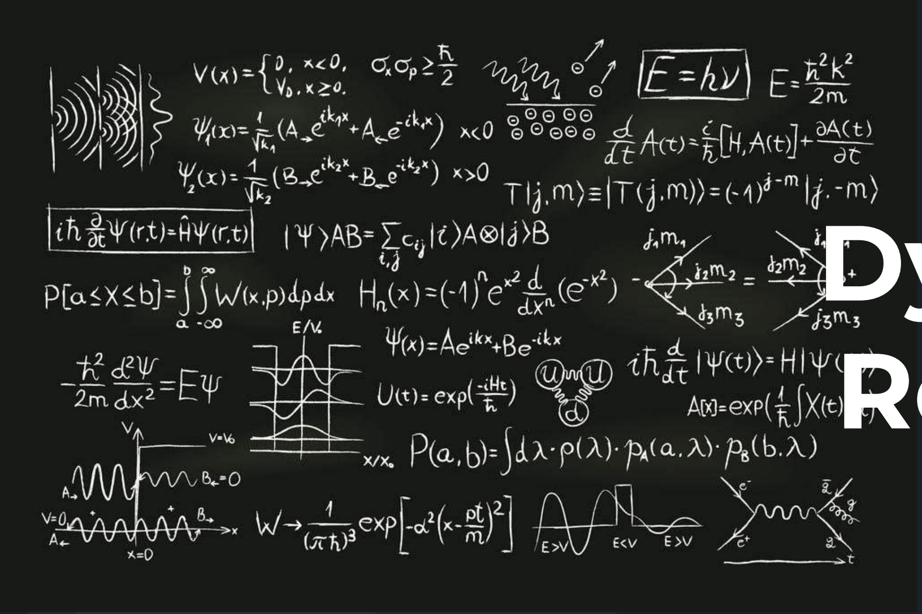


Dynamic Partial Reconfigurable Calculator Module

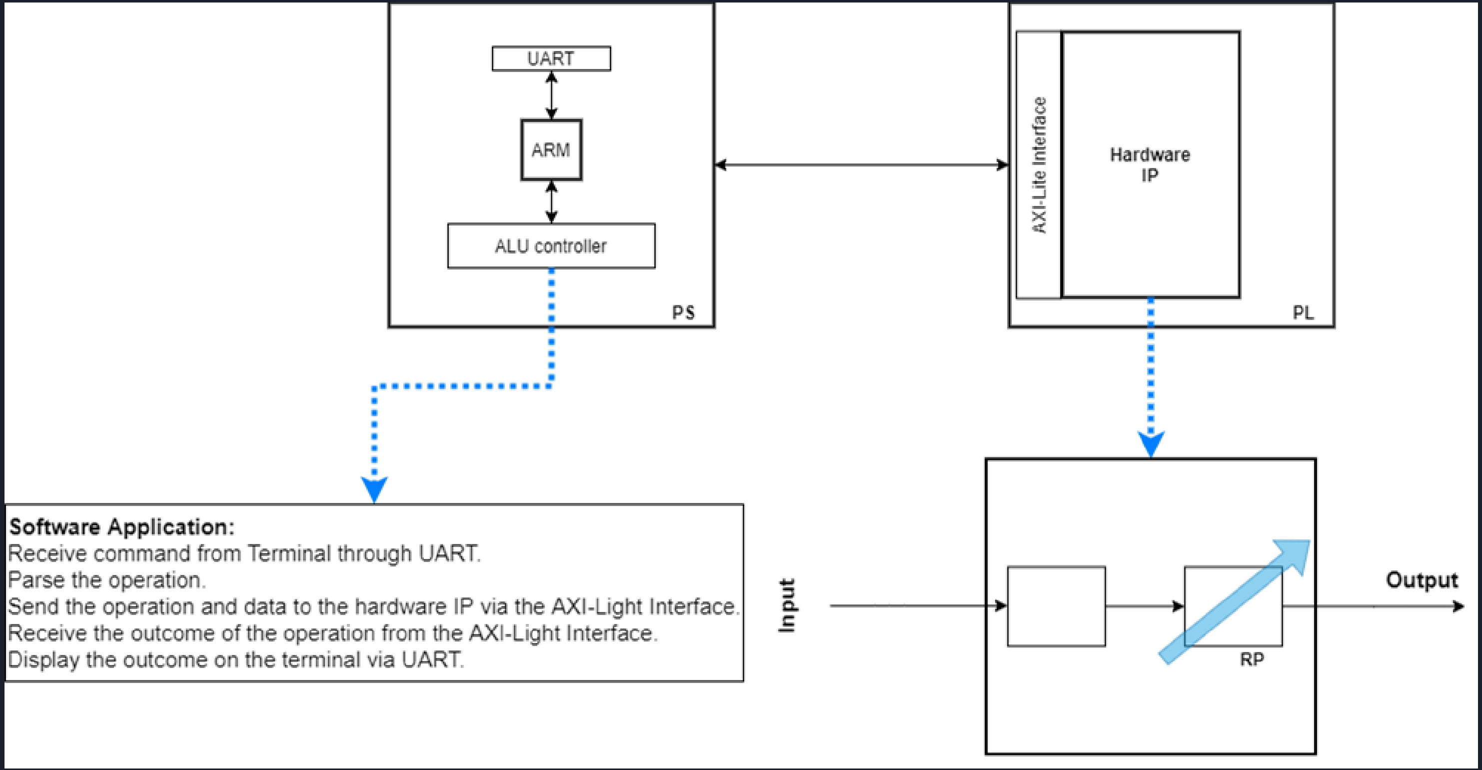
By Jeanne Beau and Zachary Martin

A DPR calculator design with a serial monitor based user interface to achieve a scalable arithmetic logic unit at a consistent size

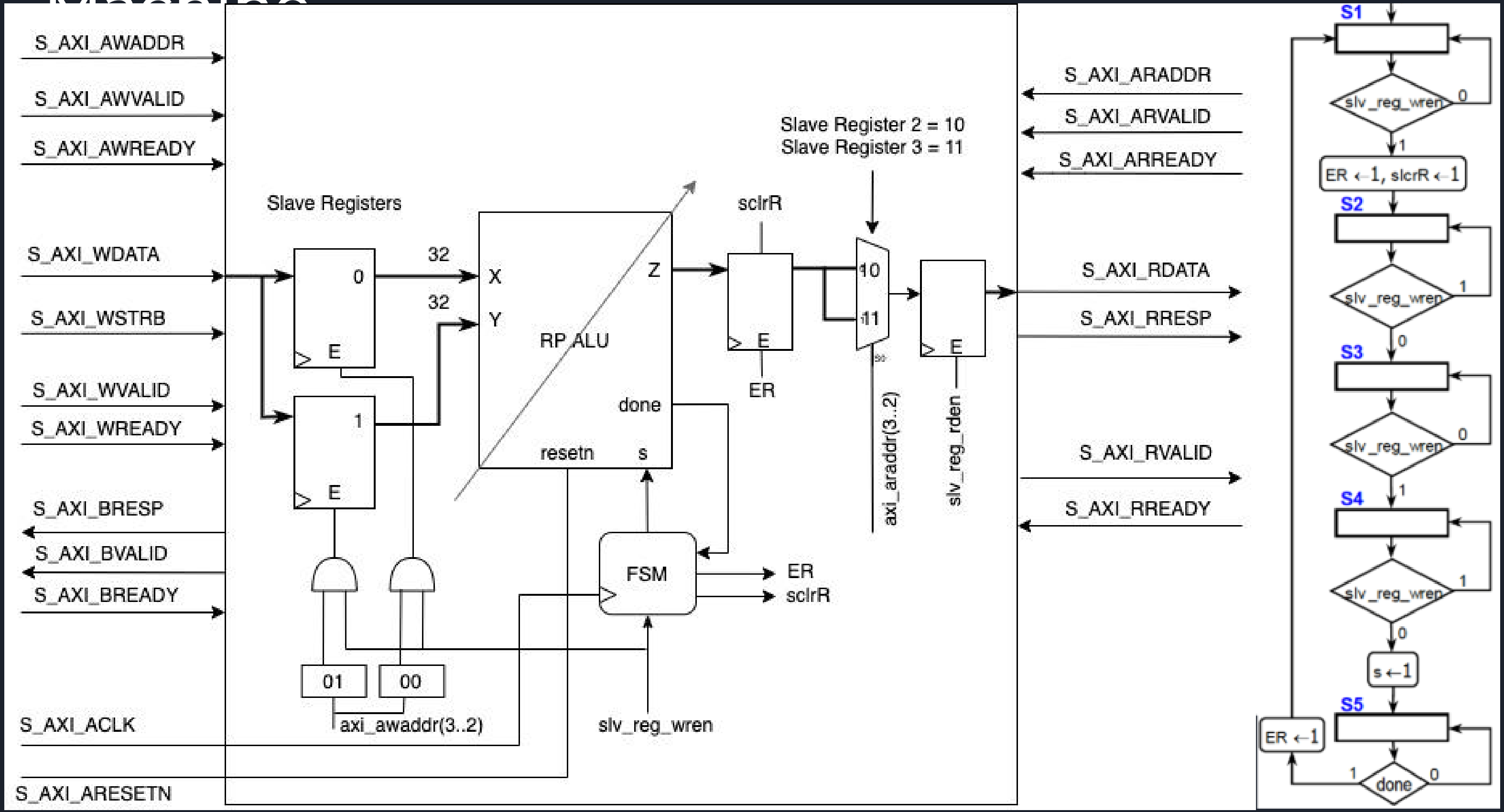
This system will:

- Receive a selected operator and two operands from the user
- Reconfigure itself to perform the operation
- Display the result of the operation on a serial terminal.

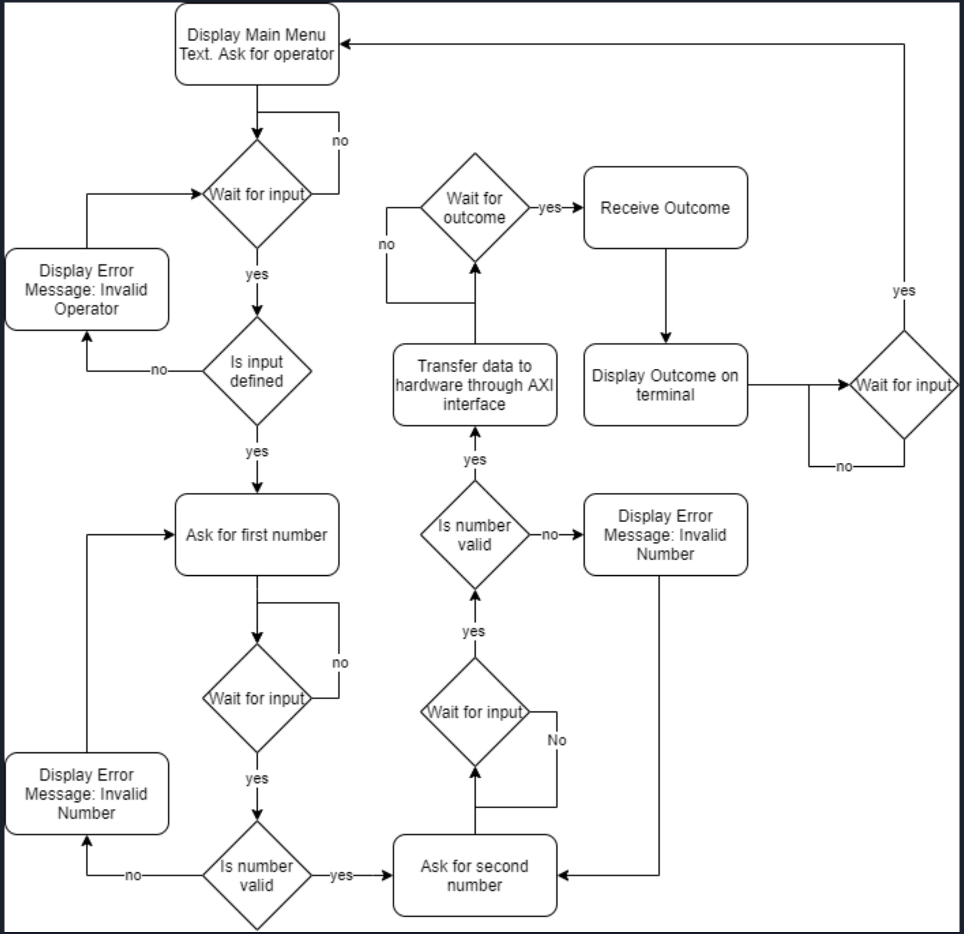
High-Level Architecture



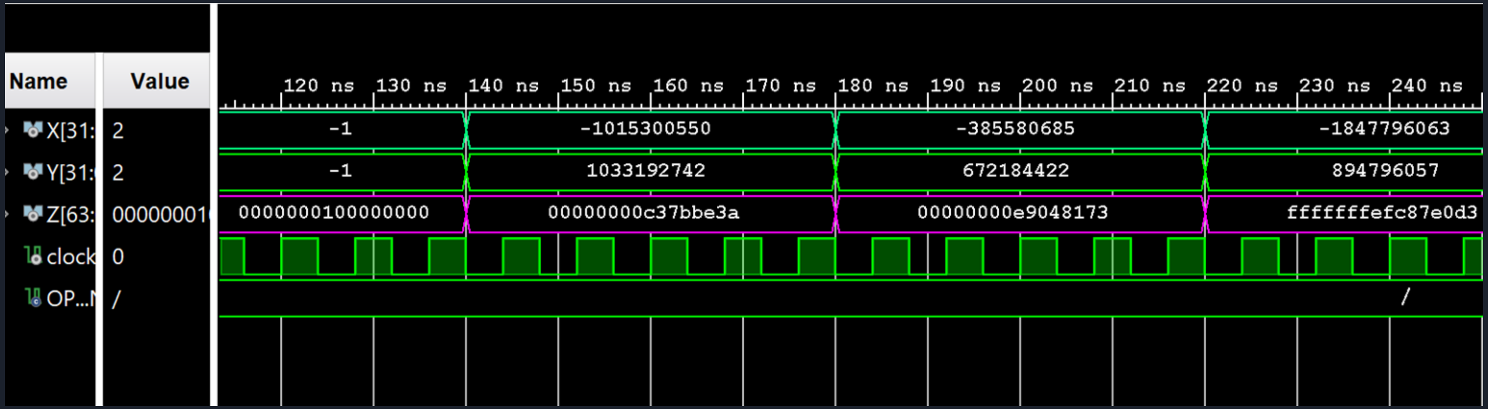
AXI4-Lite Datapath & State Machine



Software Control Logic



ALU Component - Division

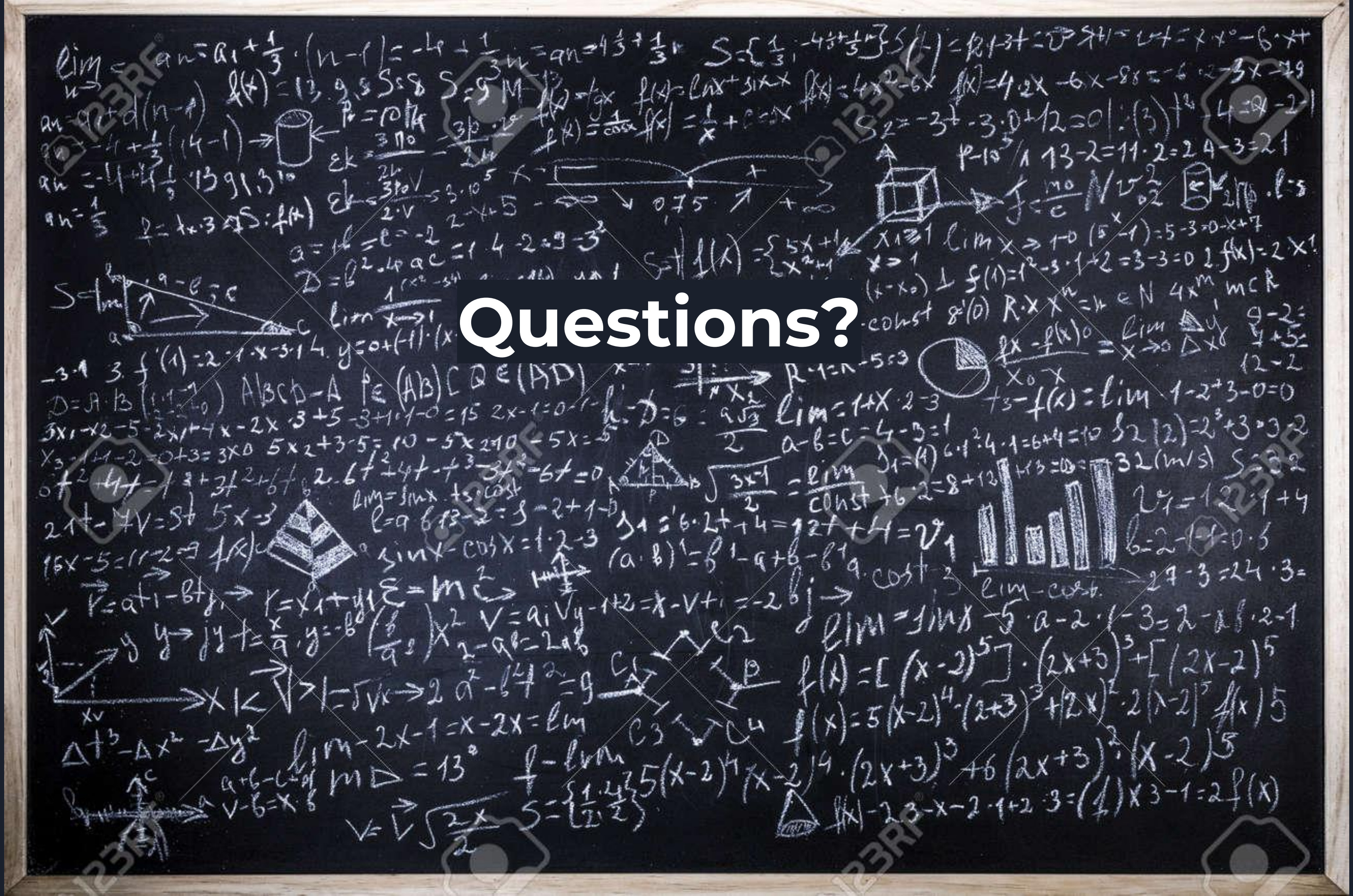


ALU Axi4-Lite - Addition

DEMO

Revelations & Conclusion

- Design Flow - floor plan constraints
  - 1st iteration - created fplan with division RM and multiplication needed DSP48 cells
  - 2nd iteration - created fplan with multiplication and division needed a larger size (more carry cells)
  - Ended up drawing a much larger block which included DSP48 cells
  - This might not be ideal because the hardware requirements are significantly varied for multiplication and division.
- Division operation limitations
  - Division results were inconsistent in software testing. This was previously simulated successfully in Vivado.
  - Results were correct when the data was written a second time. We now do this as a work around.
  - We speculate that the number of clock cycles needed is unpredictable, not given enough time to complete the computation by the time we’re ready to read the data.
  - The circuit is mostly combinational and we may be able to solve this with a more synchronous design, as discussed in a previous lecture about less clock cycles vs. combinational timing constraints.



Questions?