Course Information

INSTRUCTOR	Daniel Llamocca
CONTACT INFO	email: llamocca@oakland.edu
OFFICE HOURS	Tuesday 2:00 to 4:00 pm @ ~~Room EC 438~~, or by appointment (via Webex)
LECTURES	Monday/Tuesday/Thursday 5:30 pm - 7:35 pm @ ~~Room HH 113 (Hannah Hall)~~ Remote Lectures: ▪ Synchronous Sessions (Webex): Mondays (and Tuesday 05/26): 5:30 – 7:35 pm. ▪ Asynchronous Sessions: Panopto
LABORATORY	See schedule

COURSE CATALOG DESCRIPTION: ECE 5736 – Reconfigurable Computing (4 credits)

Analysis and design of reconfigurable computer architectures. Advanced topics in computer arithmetic. Hardware/Software co-design using Programmable System-on-Chip (ARM processor + FPGA fabric). Introduction to Self-Reconfigurable Architectures. With laboratory and design project. Offered: Summer I. Prerequisite(s): Background on digital logic and microprocessors.

COURSE WEBPAGE

- The course material will be hosted on Moodle (moodle.oakland.edu). Grades will be periodically posted via this system.
- As a backup resource, the material will also be posted at: www.secs.oakland.edu/~llamocca/Summer2020_ece5736.html
- Embedded System Design for Zynq PSoC: www.secs.oakland.edu/~llamocca/EmbSysZynq.html

TEXTBOOK:

- There is no required textbook. Students are encouraged to use the extra references.

EXTRA REFERENCES:

- Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, *The Zynq Book: Embedded Processing with the ARM® Cortex®-A9 on the Xilinx® Zynq®-7000 All Programmable SoC*, 1st ed., 2014.
  - ✓ Free download: http://www.zynqbook.com
- Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, *The Zynq Book Tutorials*, v 1.2, 2014.
  - ✓ Free download (including tutorial files): http://www.zynqbook.com
- VHDL for FPGAs Tutorial: www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html
- Peter J. Ashenden, The Designer's Guide to VHDL, 3rd ed., Elsevier, 2008.
- S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, 3rd ed., McGraw Hill, 2009
- B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd ed., Oxford University Press, Inc., 2009.

COURSE OBJECTIVES

1. Design custom architectures using fixed-point and floating-point arithmetic
2. Describe how to unfold a sequential algorithm to turn it into a fully pipelined architecture.
3. Learn advanced coding and testbench techniques in Hardware Description Language.
4. Design an embedded system using FPGA fabric and an embedded ARM® microprocessor.
5. Describe the process of Dynamic Partial Reconfiguration on an All-Programmable System-on-Chip device.
6. Design high-performance application-specific reconfigurable systems.
7. Work in a team environment to design a reconfigurable system and communicate the results in a written report and an oral presentation.

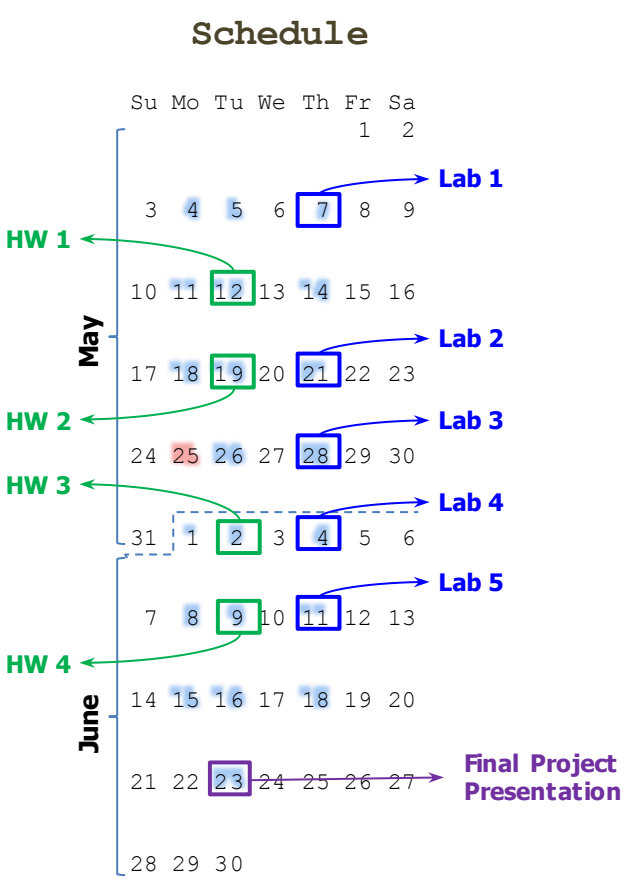
GRADING SCHEME:

Homeworks: 20%	**Laboratory:** 50%	**Final Project:** 30% (June 23rd, 5:30 – 7:35 pm)

- **Homeworks:** Homework assignments are meant to strengthen your conceptual understanding of the topics. Completing homework assignments is a key component of this course as it will help students master the course material and prepare them for the examinations.
  Homeworks will be posted according to the schedule (green rectangles). Students have one week to turn in the completed assignments in class. Late submissions are NOT accepted.

- **Laboratory:** This important component of the class will reinforce your understanding of the topics. There will be five (5) labs throughout the semester.
  Lab assignments will be posted according to the schedule (blue rectangles). Students have one week to complete the lab assignments and have them checked off by the instructor.

- **Final Project:** Students will work in groups in a Final Project. Each group will prepare an oral presentation and submit a final research paper for conference presentation.



GRADE ASSIGNMENT:

96-100	A	4.0
90-95	A-	3.7
85-89	B+	3.3
80-84	B	3.0
72-79	B-	2.7
66-71	C+	2.3
60-65	C	2.0
56-59	C-	1.7
53-55	D+	1.3
50-52	D	1.0
49 and below	F	0.0

LABORATORY MATERIALS

- **Hardware**:
  - ✓ Zybo Z7 Board – Select the Zybo Z7-10 option ($125.00).
    To order the board: https://store.digilentinc.com/zybo-z7-zynq-7000-arm-fpga-soc-development-board/
    Select the Academic Version

  - ✓ Any other Zynq-7000 board will work as well, e.g: ZYBO board, ZED Board.

- **Software**:
  - ✓ Vivado HL Webpack Edition 2019.1 with SDK and Partial Reconfiguration Feature.
    To download:
    https://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html
    Go to Downloads → 2019.1 → Vivado Design Suite - HLx Editions → 2019.1 Full Product Installation

  - ✓ MATLAB® or Octave (open-source version of MATLAB)

OUTLINE OF TOPICS

Computer Arithmetic	▪ Unsigned and signed integer numbers: binary representation ▪ Fixed-point (FX) arithmetic: addition/subtraction, multiplication, division ▪ Floating-point (FP) arithmetic: addition/subtraction, multiplication, division ▪ Dual fixed-point (DFX) arithmetic: addition/subtraction, multiplication	
Digital System Design	▪ Components: Datapath circuit, Control circuit. ✓ Algorithmic State Machine (ASM) Charts ✓ Design examples: Bit counting circuit, 7-segment serializer, Serial Multiplier. ▪ Timing Diagrams	
	VHDL coding	▪ Structural description: hierarchical design (port-map, for-generate). ▪ Use of common parametric components: counter, register, shift-register ▪ ASM description ▪ Testbench generation
Special-Purpose Arithmetic Circuits and Techniques	▪ Arithmetic units for fixed-point, floating-point and dual fixed-point. ▪ CORDIC Algorithm: circular, linear, and hyperbolic. Special functions: exp, ln, sqrt ▪ Square Root: Iterative version ▪ LUT approach: Pixel processor example (gamma correction, contrast stretching) ▪ Distributed Arithmetic: FIR Filter, DCT	
	VHDL coding:	▪ Custom-defined datatypes, arrays, packages, functions ▪ Parameterization: for-generate, if-generate ▪ Embedding counters and registers into ASM diagrams
Pipelining and unfolding	▪ Iterative, array, and pipelined array design ▪ Multi-operand addition: iterative (accumulator) vs. pipelined array (adder tree) ▪ Multiplier and Divider: iterative vs. pipelined array ▪ CORDIC: iterative vs. pipelined array	
Embedded System in a SoC	Hardware	Zynq architecture: FPGA fabric + ARM® microprocessor AXI bus: AXI4, AXI4-Lite, and AXI4-Stream Interfaces Interface development for AXI4
	Software	Introduction to SDK ARM processor SD card
	▪ Hardware/software co-design ▪ Custom IP and driver generator for AXI in Vivado ▪ Writing software applications in SDK ▪ Direct Memory Access ▪ Interrupts (from PS and PL) ▪ FPGA features: FIFOs, MMCMs, Dual-port RAMs	
	Case examples	▪ Pixel processor ▪ Pipelined Divider ▪ Pipelined 2D Convolution Kernel ▪ 2D DCT (matrix multiplication with constant)
Dynamic Partial Reconfiguration	▪ Introduction to Self-Reconfigurable Systems ▪ Static vs dynamic reconfiguration. ▪ DPR requirements: reconfiguration controller, generating and downloading bitstreams. ▪ Time and memory overhead ▪ Dynamic Frequency Control ▪ JTAG-based reconfiguration and PCAP-based reconfiguration. ▪ Case examples: ✓ 4-bit LED pattern controller (1 RP and 2 RPs). ✓ Pixel processor. ✓ 2D DCT (matrix multiplication with constant).	
Applications	▪ Dynamic Circular CORDIC. ▪ Dynamic Arithmetic: Dynamic Dual Fixed Point Adder/Subtractor. ▪ Image processing: Dynamic Pixel Processor, 2D FIR Filter ▪ DSP: Audio filter ▪ Video Compression: Transform and Quantization for HEVC ▪ Communications	

OUTLINE OF COURSE TOPICS, ASSOCIATED ASSIGNMENTS AND REFERENCE MATERIAL.

TOPICS SHADED IN GRAY: SYNCHRONOUS LECTURES (WEBEX)

TOPICS SHADED IN RED: ASYNCHRONOUS LECTURES (PANOPTO)

Week		Unit	Topic	Associated Material	Assignments
1	05/04		Class policies, class structure Unit 2, Unit 5: Quick Overview	Syllabus Zynq Book	*Laboratory 1*
	05/05	2	Bit Counting circuit: timing diagram Bit Counting circuit (n=8): VHDL coding Serial Multiplier 4x4: VHDL coding	Lecture Notes – Unit 2	
			Experiment: Serial Multiplier 2x2 (ZYBO)	Emb. Sys. on PSoCs Tutorial # 1	
	05/07	5	Experiment: Introduction to Hardware/Software Design (ZYBO Z7-10)	Zynq Book Tutorials (1. First Design on Zynq) Emb. Sys. on PSoCs Tutorial # 2	
2	05/11	2	Experiment: Serial Multiplier 2x2: (ZYBO Z7-10)	Zynq Book Lecture Notes – Unit 5	
		5	Intro to Zynq PS/PL. AXI Timing Diagrams. Overview		
			Final Project Guidelines		
	05/12	5	AXI Timing Diagrams. AXI Lite examples: pixel processor, seq. divider, pip.divider, 2D convolver	Lecture Notes – Unit 5	Homework 1
	05/14	5	Experiment: AXI Lite Custom Peripheral: pixel processor (ZYBO Z7-10) Experiment: AXI Lite Custom Peripheral: 2D convolver (ZYBO Z7-10)	Zynq Book Tutorials (4. IP Creation) Emb. Sys. on PSoCs Tutorial # 3	
3	05/18	1	Fixed-Point (FX) Arithmetic: examples	Lecture Notes – Unit 1	
		3	CORDIC	Lecture Notes – Unit 3	
		5	AXI Lite: pipelined divider Experiment: AXI Lite pipelined divider (ZYBO Z7-10) AXI Lite: CORDIC circuit	Lecture Notes – Unit 5 Emb. Sys. on PSoCs Tutorial # 3	
	05/19	5	AXI Full examples: pixel processor, pip. Divider, 2D convolver	Lecture Notes – Unit 5	Homework 2
	05/21	5	Experiment: AXI Full: pixel processor (ZYBO Z7-10) Experiment: AXI Full: convolver 2D (ZYBO Z7-10)	Emb. Sys. on PSoCs Tutorial # 4	*Laboratory 2*
4	05/26	5	AXI Full: pipelined divider Experiment: AXI Full pipelined divider (ZYBO Z7-10) AXI Full: CORDIC circuit	Lecture Notes – Unit 5 Emb. Sys. on PSoCs Tutorial # 4	
	05/28	5	Experiment: SD Card and AXI4-Full Pixel Processor	Emb. Sys. on PSoCs Tutorial # 5	*Laboratory 3*
5	06/01	4	Pipelining: examples	Lecture Notes – Unit 4	
		6	DPR explanation: JTAG-based, PS+PL, TCL-based flow Pixel processor and DCT circuits. File Organization	Lecture Notes – Unit 6	
	06/02	6	DPR Intro. Design Steps. Tcl-based design flow. File organization for hardware-only project and PS+PL project. Experiment: DPR – Only PL using JTAG: 4-bit LED Pattern Controller	Lecture Notes – Unit 6 Emb. Sys. on PSoCs Tutorial # 6	Homework 3
	06/04	6	Experiment: DPR – PS+PL using PCAP: on Pixel processor Experiment: DPR – PS+PL using PCAP: on DCT	Lecture Notes – Unit 6 Emb. Sys. on PSoCs Tutorial # 7	*Laboratory 4*
6	06/08	6	DPR: review of pixel processor and DCT designs: circuit, AXI interface	Lecture Notes – Unit 6	
		1	DFX, FP: examples	Lecture Notes – Unit 1	
		5	Direct Memory Access, Interrupts	Lecture Notes – Unit 5	
	06/09	5	Experiment: DMA	Lecture Notes – Unit 5 Emb. Sys. on PSoCs Tutorial # 8	Homework 4
	06/11	5	Experiment: Interrupts: Pixel Processor	Lecture Notes – Unit 5 Emb. Sys. on PSoCs Tutorial # 9	*Laboratory 5*
7	06/15	3	DFX Adder/Subtractor	Lecture Notes – Unit 3	
		7	DPR and Interrupts: DDFX add/sub design	Lecture Notes – Unit 7	
	06/16	7	Experiment: DPR and CORDIC: Dynamic CORDIC	Lecture Notes – Unit 7	
	06/18	7	Experiment: DPR and Interrupt: DDFX add/sub design	Lecture Notes – Unit 7	
8	06/23		Final Project - Presentation		

CLASS POLICIES

- **Assignments (Homeworks, Laboratory)**: Unless specifically stated otherwise, the homeworks and laboratory work is individual, and students are not allowed to submit their work in groups.

- **Academic conduct policy**: All members of the academic community at Oakland University are expected to practice and uphold standards of academic integrity and honesty. Academic integrity means representing oneself and one's work honestly. Misrepresentation is cheating since it means students are claiming credit for ideas or work not actually theirs and are thereby seeking a grade that is not actually learned. Academic dishonesty will be dealt with seriously and appropriately. Academic dishonesty includes, but it is not limited to cheating on examinations, plagiarizing the works of others, cheating on lab reports, unauthorized collaboration in assignments, hindering the academic work of other students.

- **Special Considerations**: Students with disabilities who may require special consideration should make an appointment with campus Disability Support Services, 106 North Foundation Hall, phone 248 370-3266. Students should also bring their needs to the attention of the instructor as soon as possible. For academic help, such as study and reading skills, contact the Academic Skills/Tutoring Center, 103 North Foundation Hall, phone 248 370-4215.

- **Add/Drops**: The university policy will be explicitly followed. It is the student's responsibility to be aware of deadline dates for dropping courses.

- **Attendance**: It is assumed that the students are aware of and understand the university attendance policy. Attendance is mandatory and maybe monitored. Students are responsible for all material covered in classes that they miss. There will no excuses for being late to exams.

- **Athlete Excused Absences**: Students shall inform the instructor of dates they will miss class due to an excused absence prior to the date of that anticipated absence. For activities such as athletic competitions whose schedules are known prior to the start of a term, students must provide their instructors during the first week of each term a written schedule showing days they expect to miss classes. For other university excused absences, students must provide the instructor at the earliest possible the dates that they will miss.

- **Special Circumstances:** The instructor should be notified as early as possible regarding any special conditions or circumstances which may affect a student's performance during the course timeframe (e.g., medical emergencies, family circumstances).

- **Cellphones**: A ringing cellphone going off during a lecture is disruptive to other students as well as the instructor. Students are strongly advised to set their cellphones to vibrate (not ringing) and leave the classroom discretely to answer the phone.