Floating Point Calculator

ECE 5736 - Professor Llamocca

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Objective

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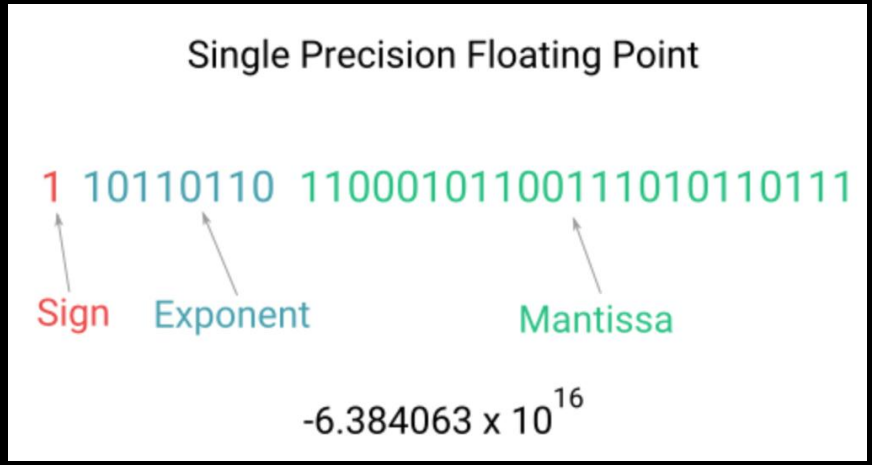
- Floating Point Calculator
  - Addition
  - Subtraction
  - Multiplication



Block Diagram of the Digital System

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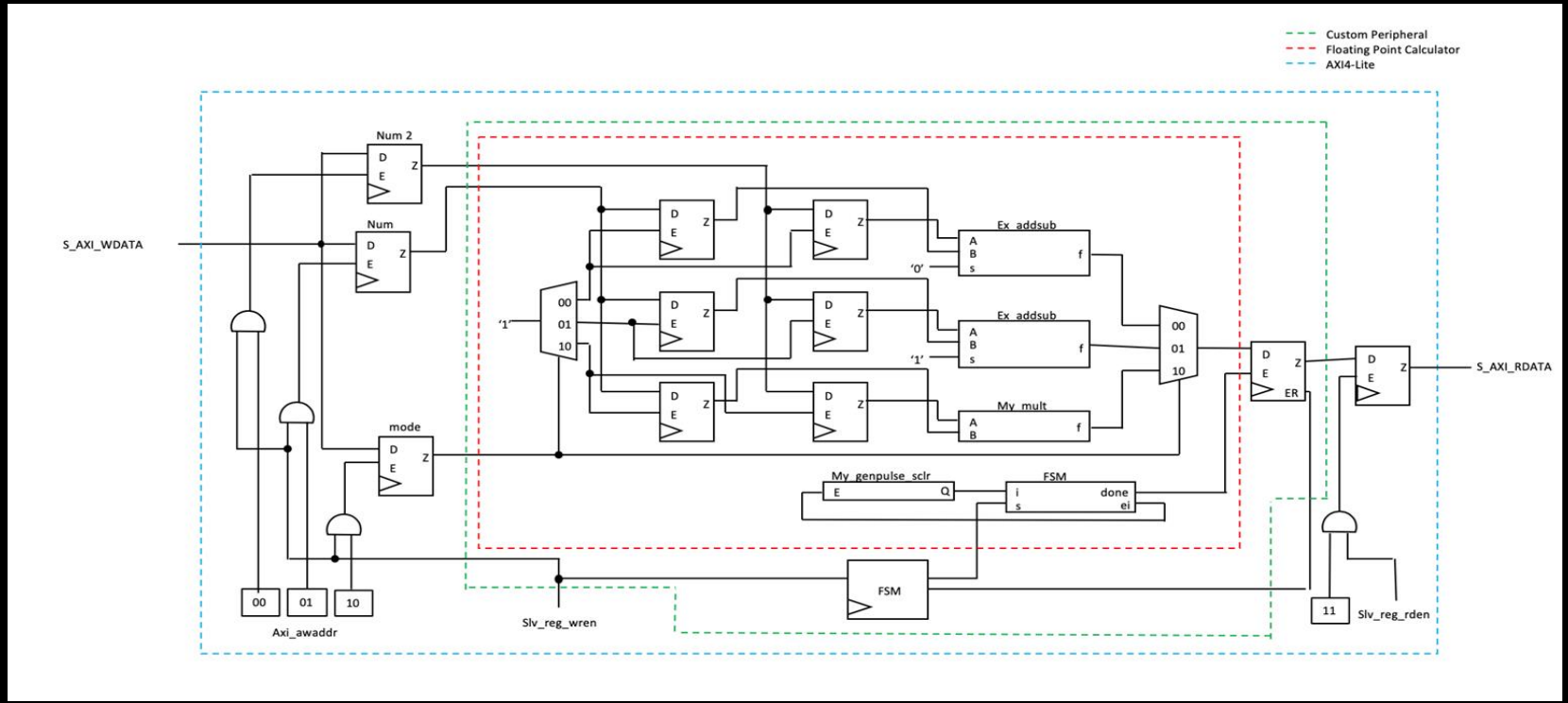

Bus Interface

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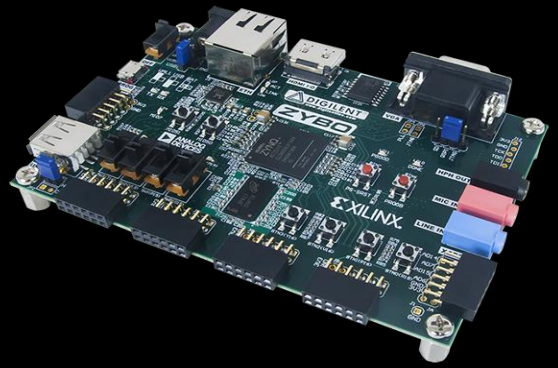
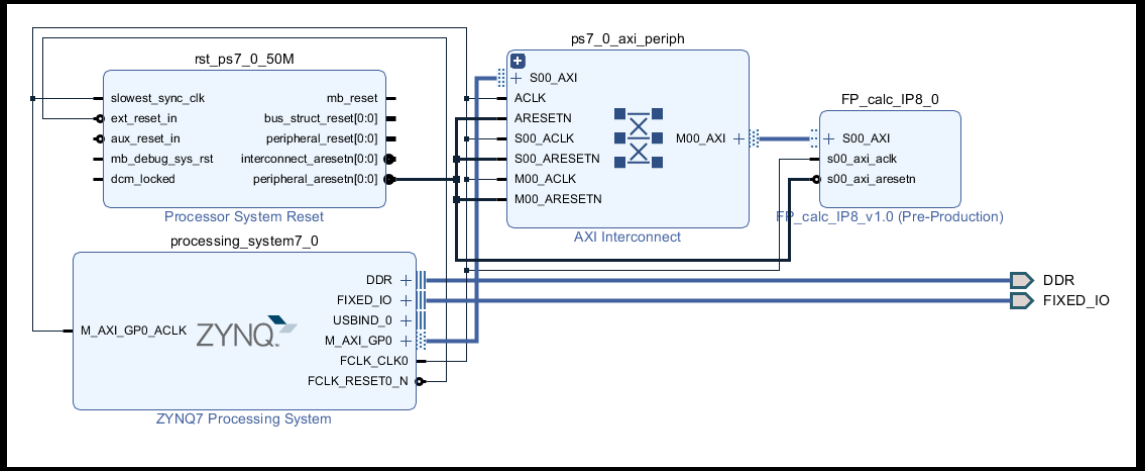
- Connects the digital system to the ARM processor on the ZYBO Z-10





Software Routine

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- Using the SDK terminal to read the results over UART

1. Define the base address.

2. Write a 32-bit word to slave_register_0. This is number 1.

3. Write a 32-bit word to slave_register_1. This is number 2.

4. Write a 32-bit word to slave_register_2. This is the operation.

5. Display the calculated value from the output register, slave_register_3.

FSM

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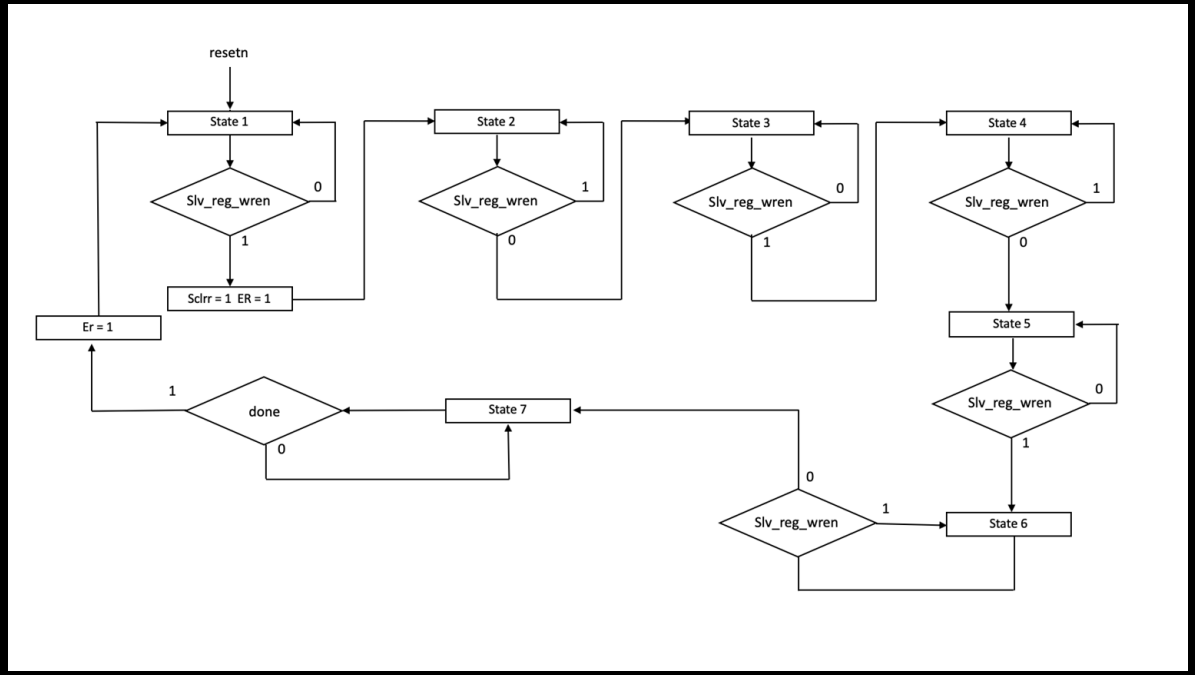

Problems

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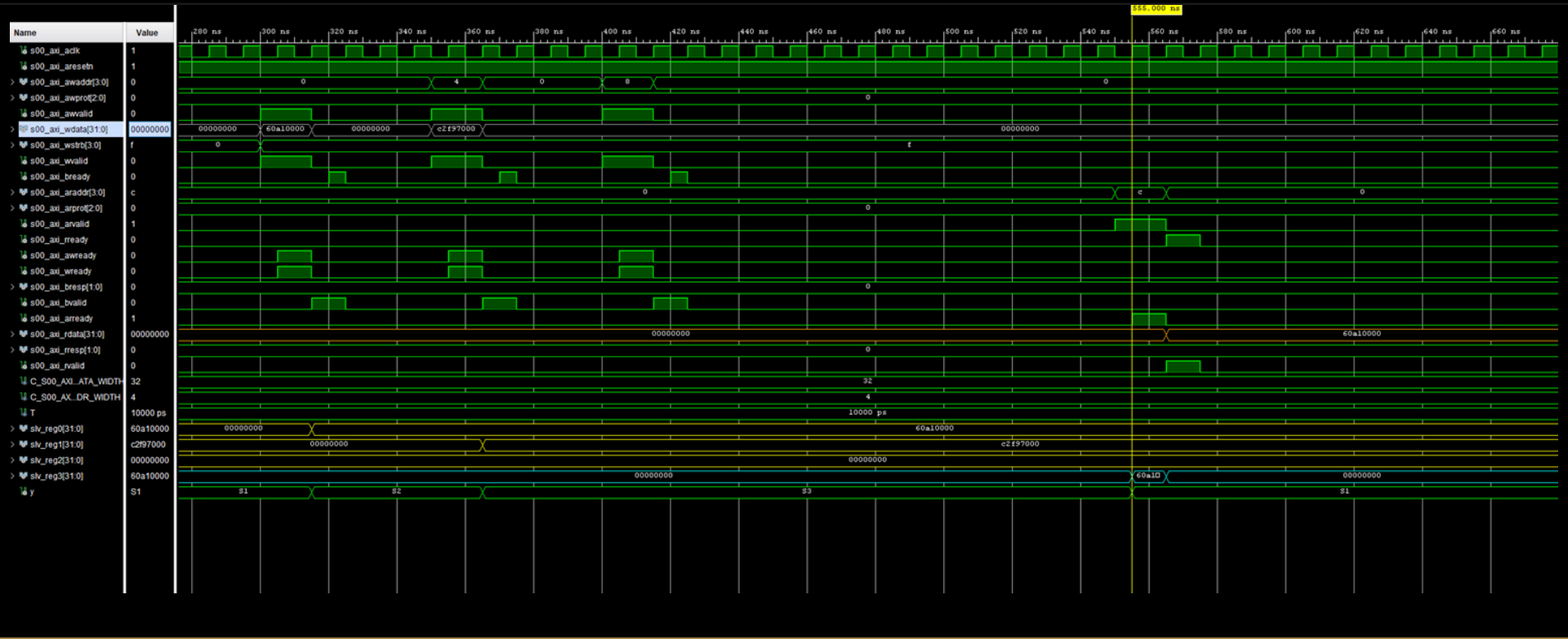

Problems

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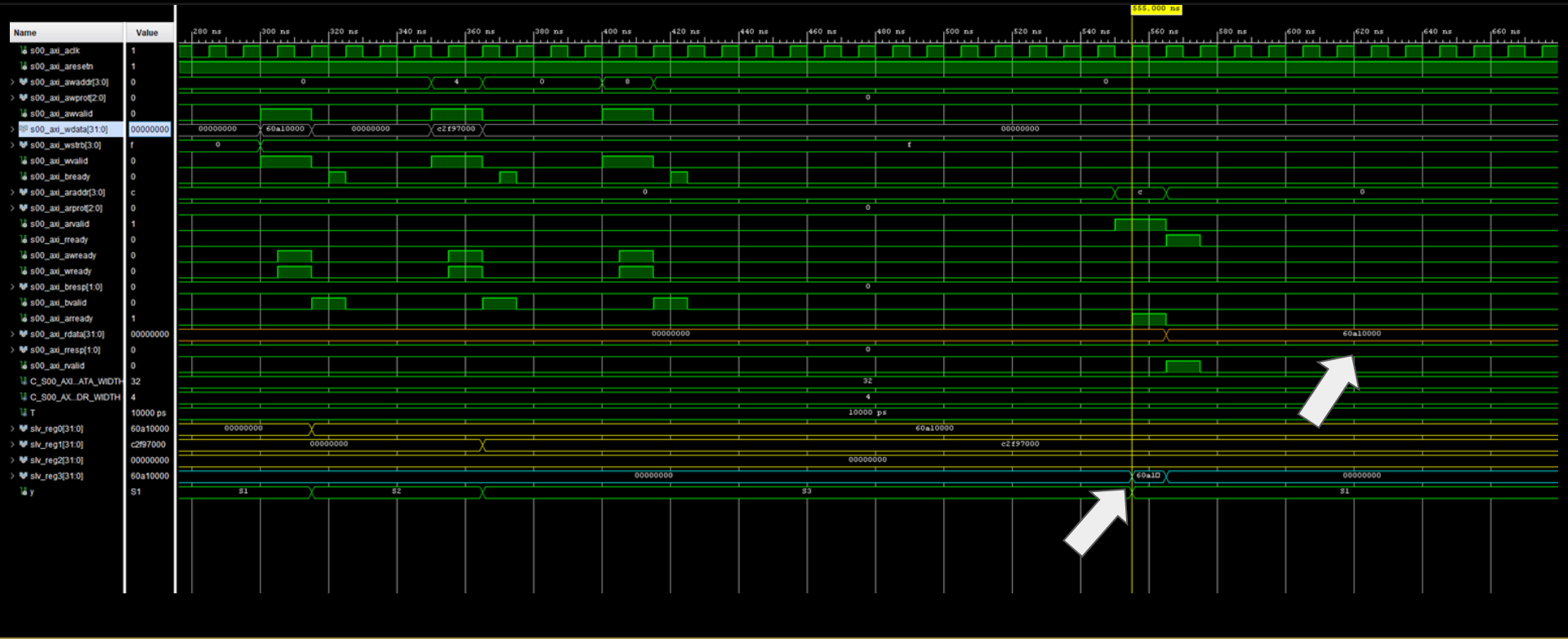

Problems

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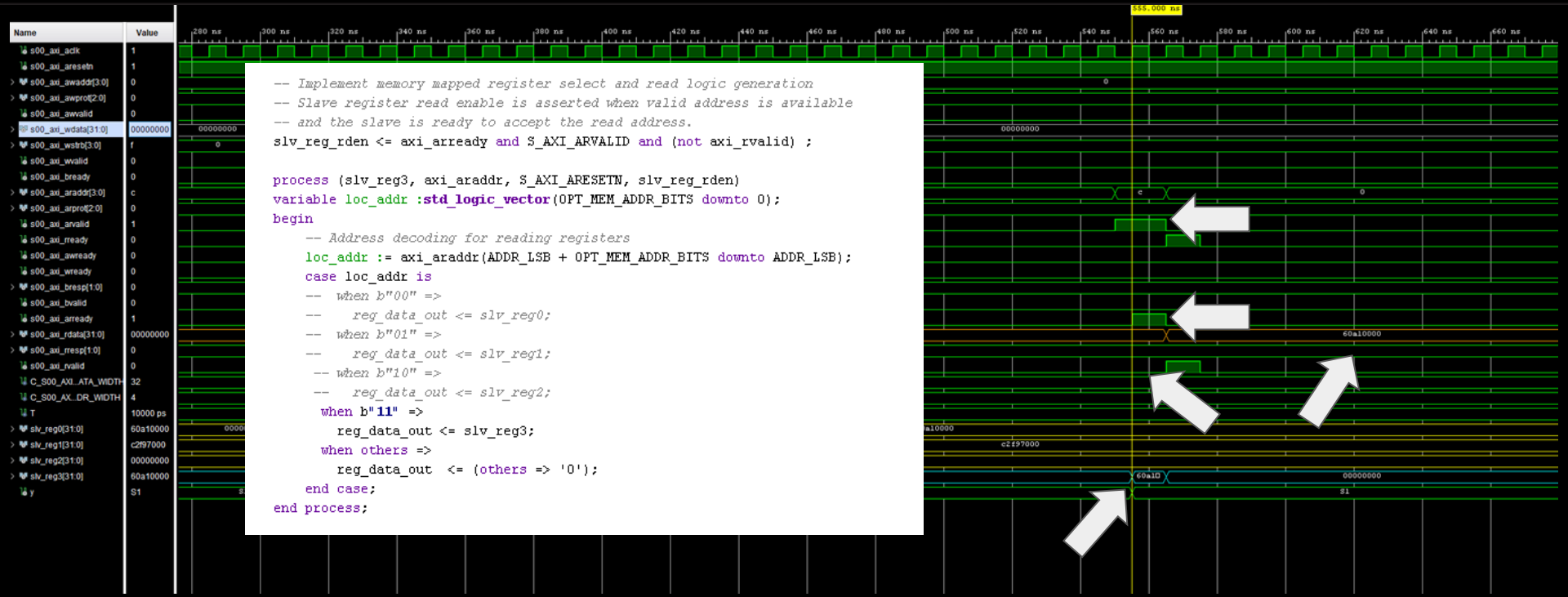


```
-- Implement memory mapped register select and read logic generation
-- Slave register read enable is asserted when valid address is available
-- and the slave is ready to accept the read address.
slv_reg_rden <= axi_arready and S_AXI_ARVALID and (not axi_rvalid) ;

process (slv_reg3, axi_araddr, S_AXI_ARESETN, slv_reg_rden)
variable loc_addr :std_logic_vector(OPT_MEM_ADDR_BITS downto 0);
begin
    -- Address decoding for reading registers
    loc_addr := axi_araddr(ADDR_LSB + OPT_MEM_ADDR_BITS downto ADDR_LSB);
    case loc_addr is
    --  when b"00" =>
    --    reg_data_out <= slv_reg0;
    --  when b"01" =>
    --    reg_data_out <= slv_reg1;
     -- when b"10" =>
     --   reg_data_out <= slv_reg2;
      when b"11" =>
        reg_data_out <= slv_reg3;
      when others =>
        reg_data_out  <= (others => '0');
    end case;
end process;
```

Problems

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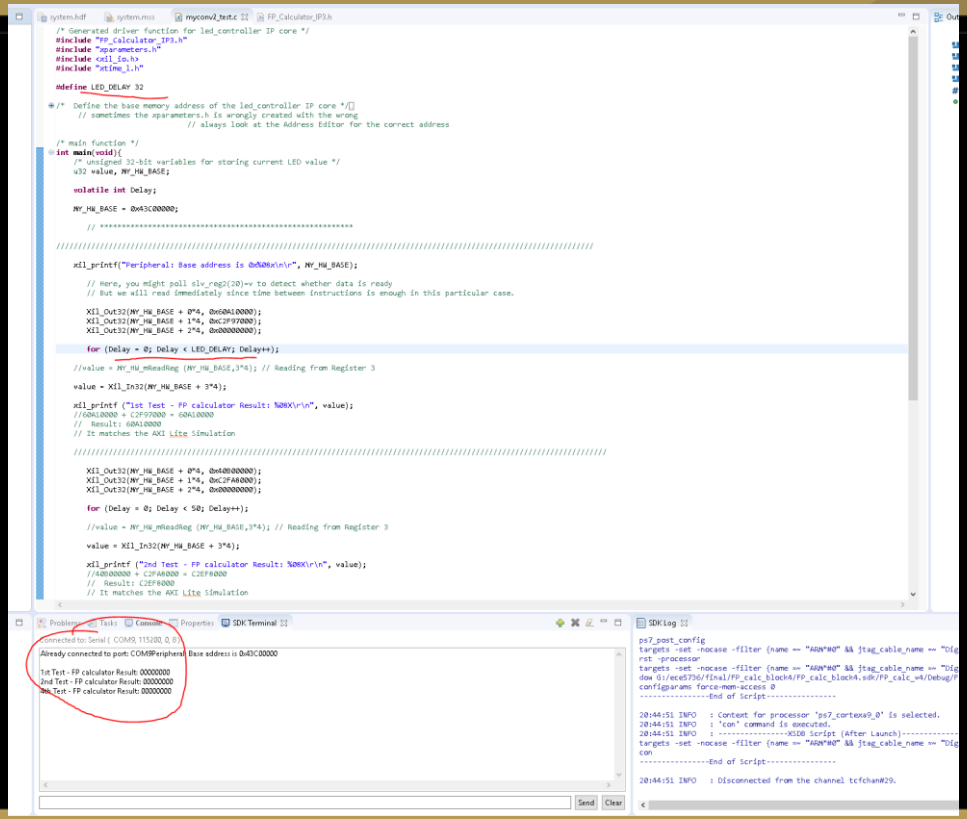

- Improper implementation of the FSM caused data to be read incorrectly in the software routine

Problems

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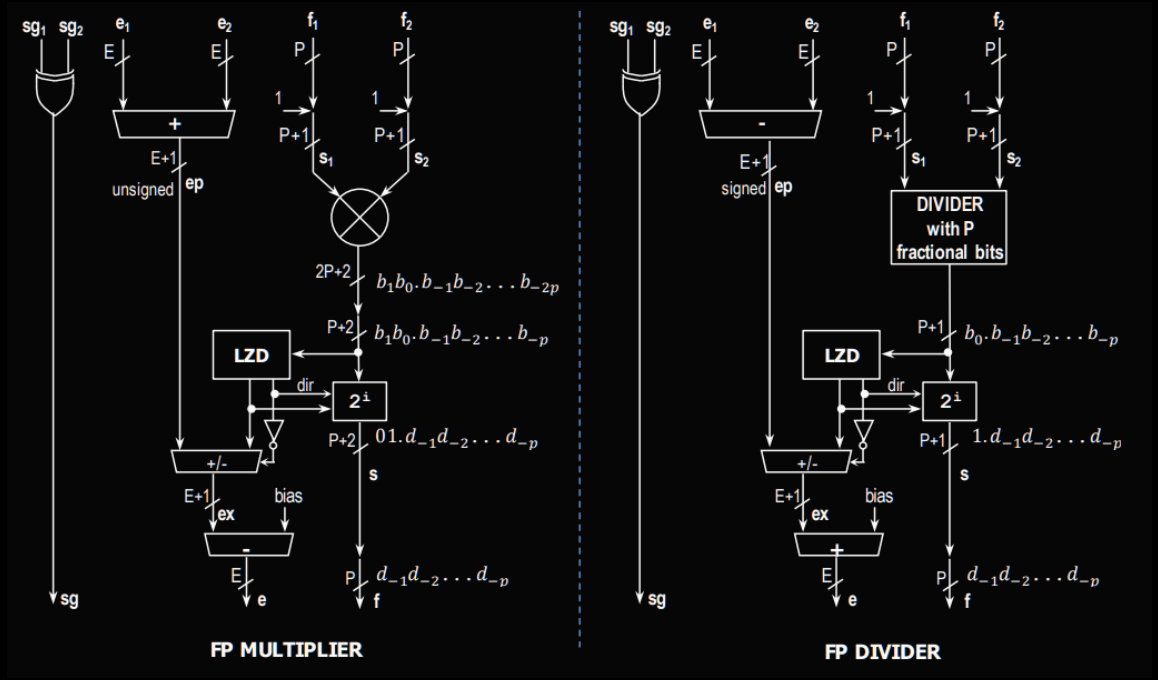
- Unable to properly implement the unsigned floating point divider
- Overflow and underflow conditions for the multiplier



Testbench

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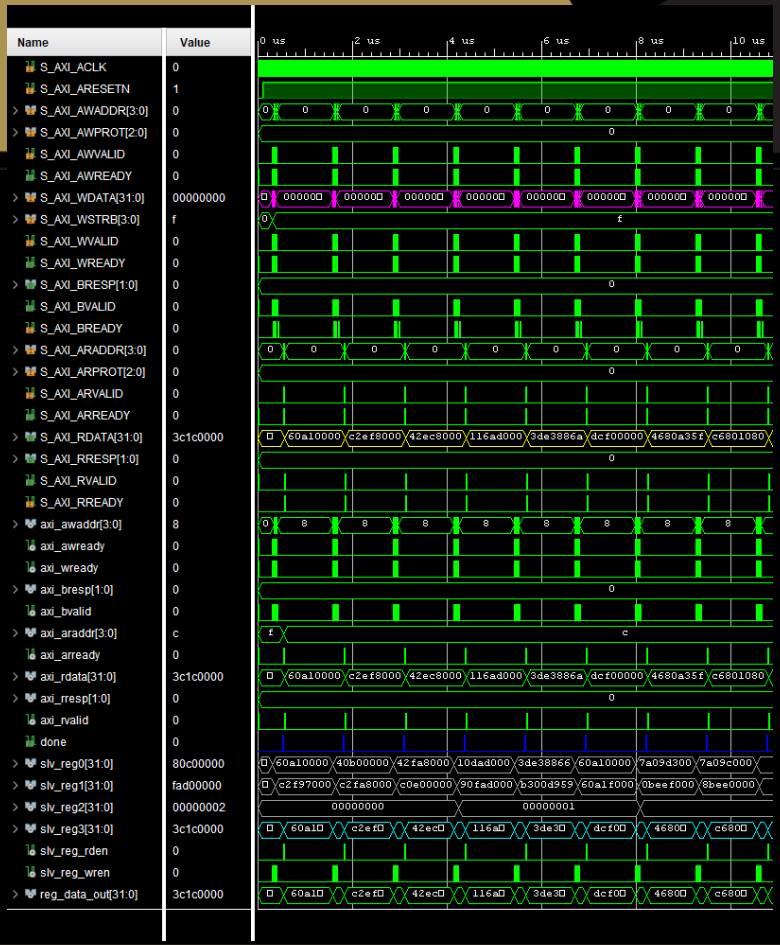
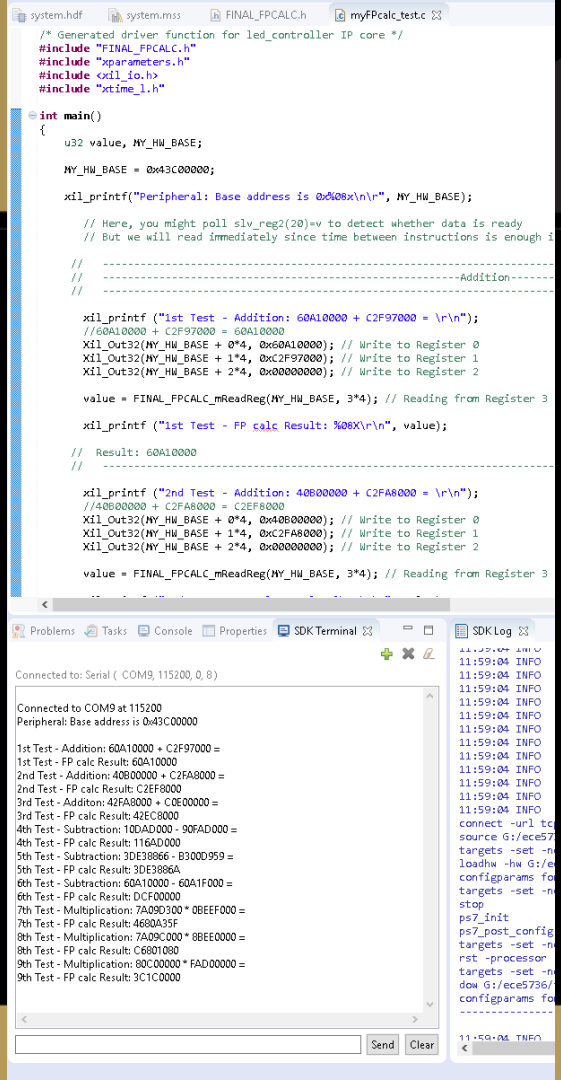
- Implemented simulation tests at the FP calculator and AXI level



- Magenta = write data
- Gray = input to slave registers
- Dark Blue = done bit sent to FSM
- Light Blue = output to slave register
- Yellow = read data

Results

- Successful writing and reading of the circuit



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Lessons Learned

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- Importance of testbench simulations
- Time constraints

Questions?