Image Processing using Dynamic Partial Reconfiguration on Zynq 7020

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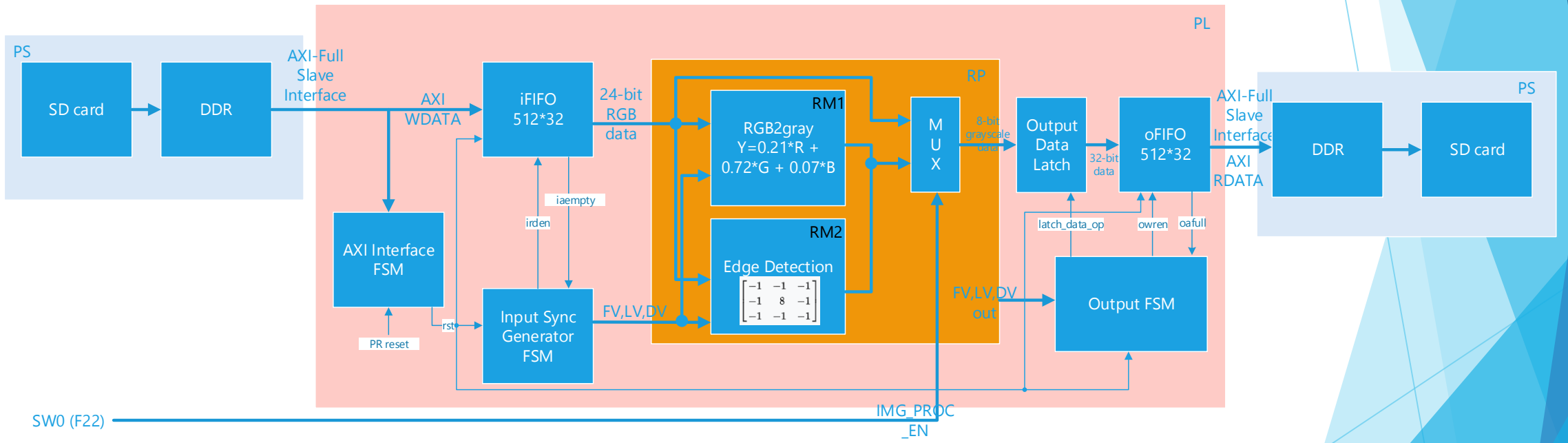
December 10, 2018

Motivation

- Image processing algorithms can be resource intensive
- Depending on the algorithm, they could require multiple DSP elements and block RAMs.
- DPR provides the ability to selectively swap algorithms in and out of the PL
  - Done using the PCAP interface
  - Required device size can be reduced in this case

System Overview

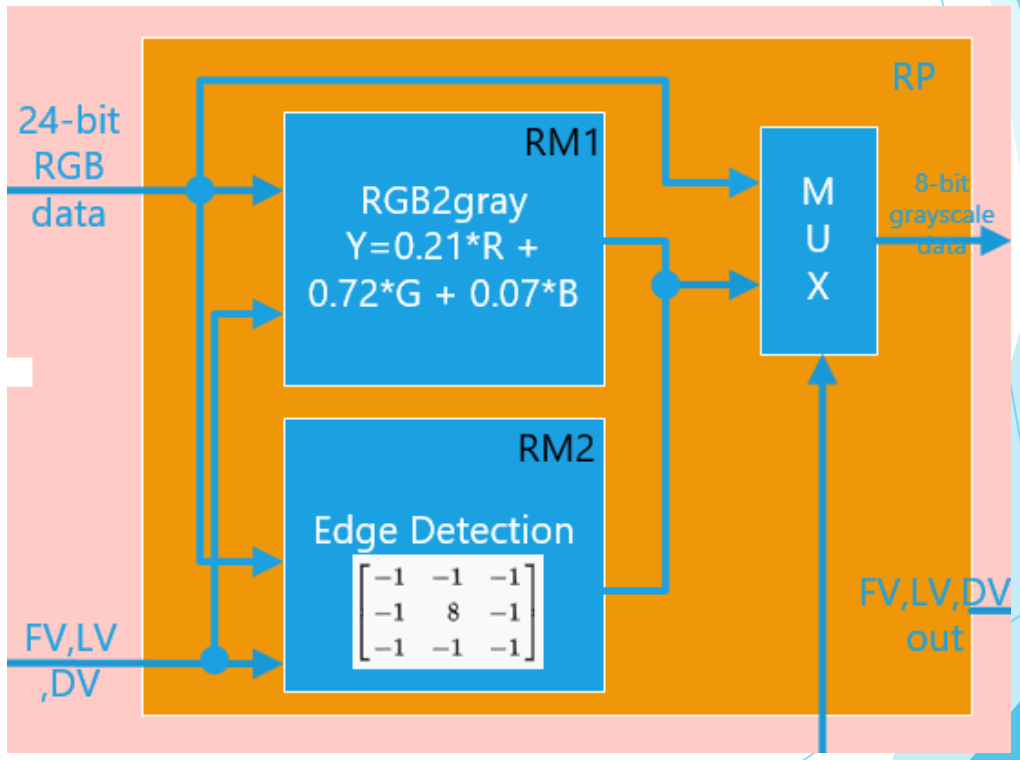


Reconfigurable Partition (RP) Overview

- 1 Reconfigurable Partition
- 2 Reconfigurable Modules
- RM1: RGB2gray
  - Y=0.21*R + 0.72*G + 0.07*B
- RM2: Edge Detection
  - 2-D convolution using the kernel

$$\begin{bmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix}$$

  - The result from 3 channels is averaged to get the final 8-bit value
- MUX is used to select between bypassed image or processed image for debugging purpose

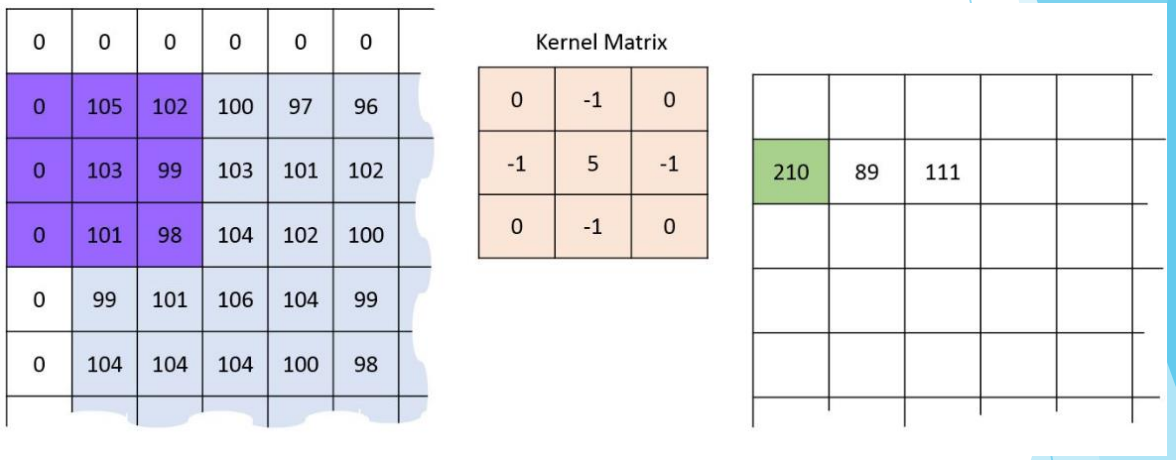


RM2: Edge Detection

- 2-D convolution using the kernel

$$\begin{bmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix}$$

- Border pixels don't have enough context
  - Output is set to zero
- Negative values after convolution are converted to their absolute values
- The result from 3 channels is averaged to get the final 8-bit value
- If the result of the average is more than 255, it is clipped to 255
- 2 Line Buffers to provide data for context



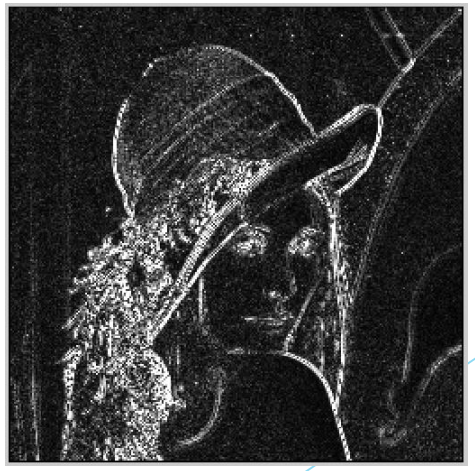
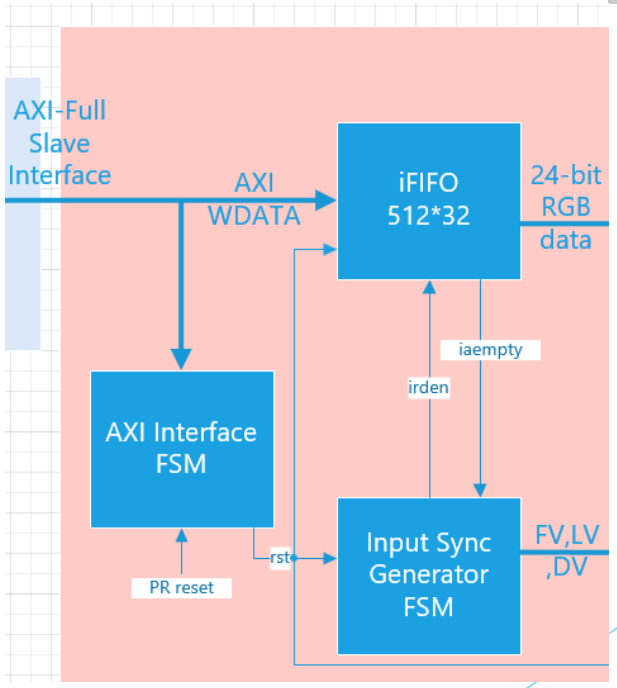
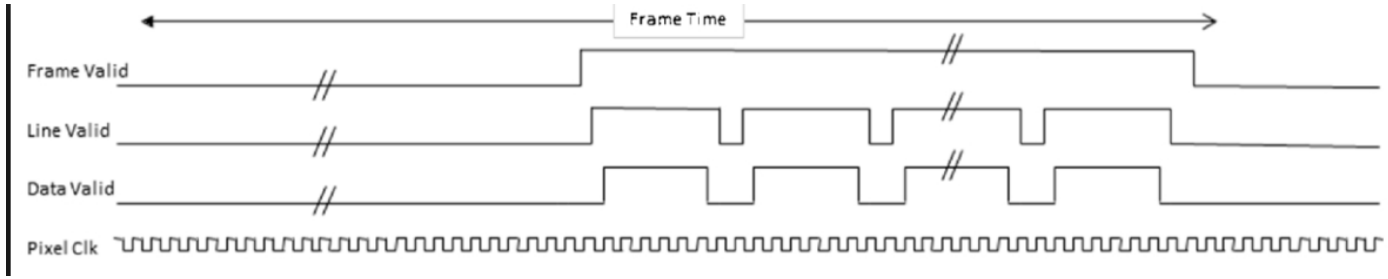


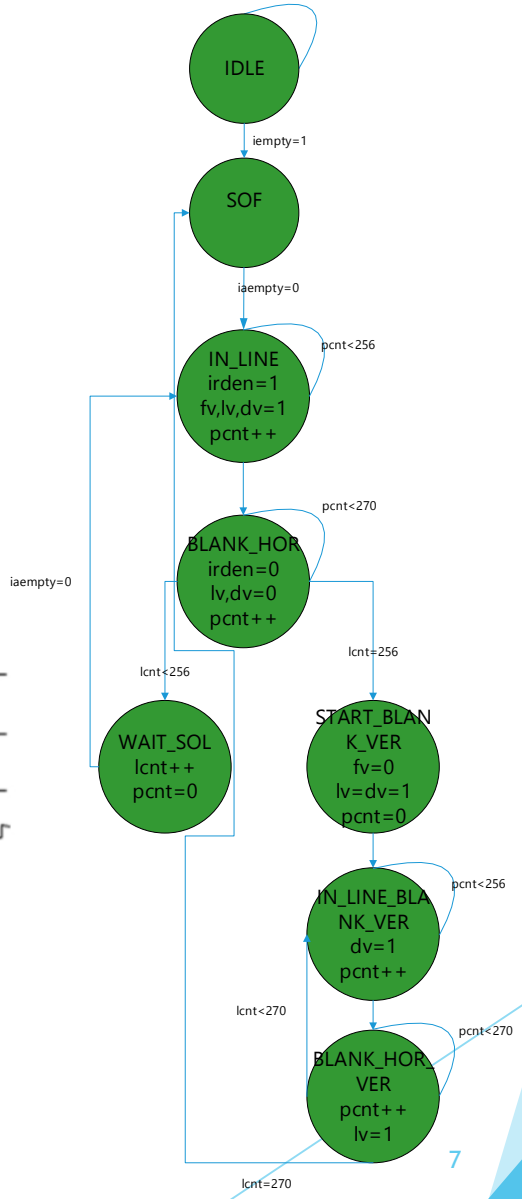
Image Input Process

- Input image is 256x256 24-bit RGB
- PS sends one line (256 32-bit words) to PL
  - 24-bit RGB data is padded with zeros
- The almost empty flag of the input FIFO deasserts
  - Almost empty threshold is 256
- One line of data is sent to the RM
- Process continues until all the lines are written



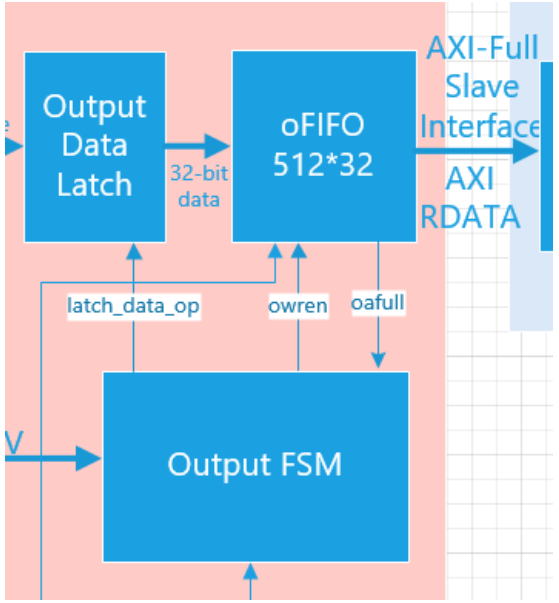
PL: Input Sync Gen FSM



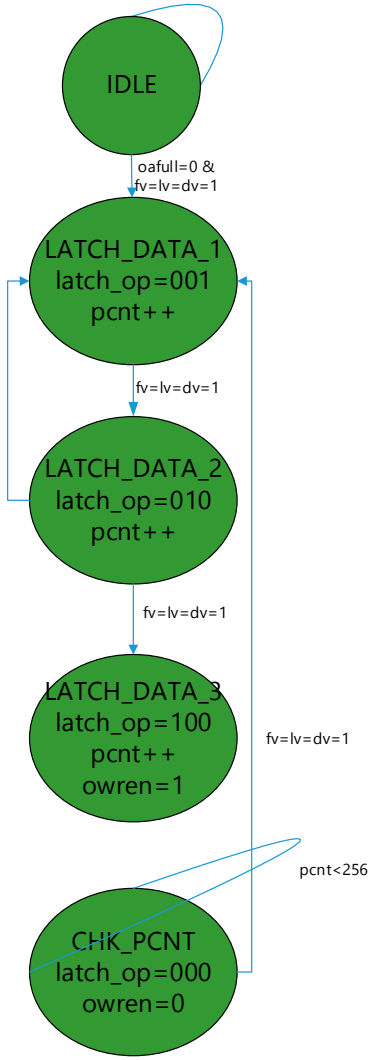


PL: Image Output Process

- Output image is 256x256 8-bit grayscale
- 4 8-bit pixels are latched and combined to make a 32-bit word
  - i.e. one line = 256/4 = 64 words
- The almost full flag of the output FIFO deasserts
  - Almost full threshold is 64
- One line of data is sent from the RM



PL: Image Output FSM



Dynamic Partial Reconfiguration Process

- Start with RGB2Gray bitfile
  - Send image
  - Run image processing
  - Retrieve image
- Transfer Edge Detection bitfile
- Reset the RP
  - Send image
  - Run image processing
  - Retrieve image
- Transfer RGB2Gray bitfile
- Reset the RP
  - Send image
  - Run image processing
  - Retrieve image

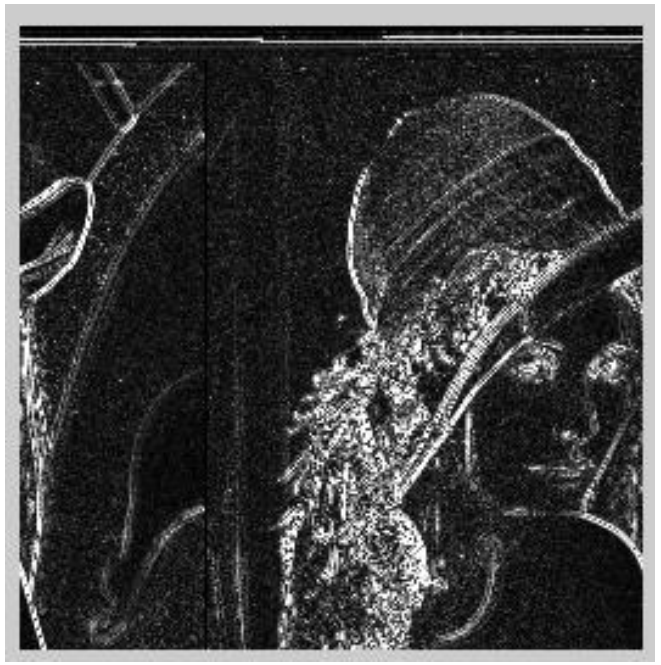
Results:RGB2Gray

Matlab reference

HW output

Results: Edge detection

Matlab reference



HW output

Conclusion

- DPR Challenges
  - Floorplanning
    - Selected Pblock should accommodate elements required by all RMs in the least amount of space
  - Interface definition
    - The interface should be common between the two RMs
  - Proper reset procedure should be followed to ensure the RP starts from an idle state
  - Ability to effectively debug in hardware

Thank You