# Course Information

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|---|---|
| INSTRUCTOR | Daniel Llamocca |
| CONTACT INFO | email: llamocca@oakland.edu |
| OFFICE HOURS | Tuesday 2:00 to 4:00 pm @ Room EC-438, or by appointment<br>Virtual Office hours also available (on Moodle → Virtual Office hours via Zoom) |
| LECTURES | CRN 13477: Tuesday/Thursday 7:30 pm - 9:17 pm @ Room MSC-384 (Math & Science Center)<br>* This is an "In-Person" class (the online method of instruction is not available). Exams and laboratories will not be administered online. |
| TAs | ~~Andrew Dejonge adejonge@oakland.edu~~<br>Nathan Kelley nkelley@oakland.edu<br>Mike Bowers mkbowers@oakland.edu |

LABORATORY

| Section | CRN | Time | TAs | | |
|---|---|---|---|---|---|
| 005 | 13478 | Wednesday 7:30 pm – 10:30 pm @ Room EC-562 | ~~Andrew~~ | Nathan | Mike |
| 006 | 13479 | Thursday 11:30 am – 2:30 pm @ Room EC-562 | ~~Andrew~~ | Nathan | Mike |

## COURSE CATALOG DESCRIPTION: ECE 4710 – Computer Hardware Design (4 credits)

Development of components and techniques needed to design digital circuits and systems for controllers, computers, communication and related applications. Design and analysis of combinational and sequential logic circuits using a hardware description language such as VHDL, timing simulations, test benches, embedded cores. Design of special-purpose processors and their implementation in an FPGA. With Laboratory. Offered fall, winter, summer.
Prerequisite(s): ECE2700 or ECE 278 and major standing.

## COURSE MATERIALS

- The course material will be hosted on Moodle (moodle.oakland.edu). Grades will be periodically posted via this system.
- As a backup resource, the material will also be posted at: www.secs.oakland.edu/~llamocca/Winter2022_ece4710.html
- VHDL for FPGAs Tutorial: Available at the following permanent link: www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

### TEXTBOOK

- There is no required textbook. Students are encouraged to use the extra references.

### EXTRA REFERENCES:

- Pong P. Chu, *FPGA Prototyping by VHDL examples: Xilinx Spartan-3 version*. John Wiley & Sons, 2011.
- M. Morris, C. Kime, T. Martin, *Logic and Computer Design Fundamentals*, Pearson Education , 5th edition, 2015
- S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, 3rd ed., McGraw Hill, 2009.
- Bryan J. Mealy, James T. Mealy, *Digital McLogic Design*, Free Range Factory, 2012.
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- Bryan Mealy, Fabrizio Tappero, Free Range VHDL, Free Range Factory, 2013
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- Peter J. Ashenden, The Designer's Guide to VHDL, 3rd ed., Elsevier, 2008.

## COURSE OBJECTIVES

1. Design combinational and sequential components in VHDL. (1)
2. Describe how combinational and sequential components can be used to design a datapath and control unit for implementing digital systems. (1, 4)
3. Design custom architectures to interact with external peripherals. (2)
4. Design dedicated special-purpose processors using VHDL and synthesize them to an FPGA. (1,2,4)
5. Build a testbench for a digital system. (6)
6. Perform functional and timing simulation of a digital circuit described in VHDL. (1,2,4)
7. Work in a team environment to design a digital system and communicate the results in a written report and an oral presentation. (1,2,3,4,5,7)

**ABET Course Outcomes**:

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|

## GRADING SCHEME:

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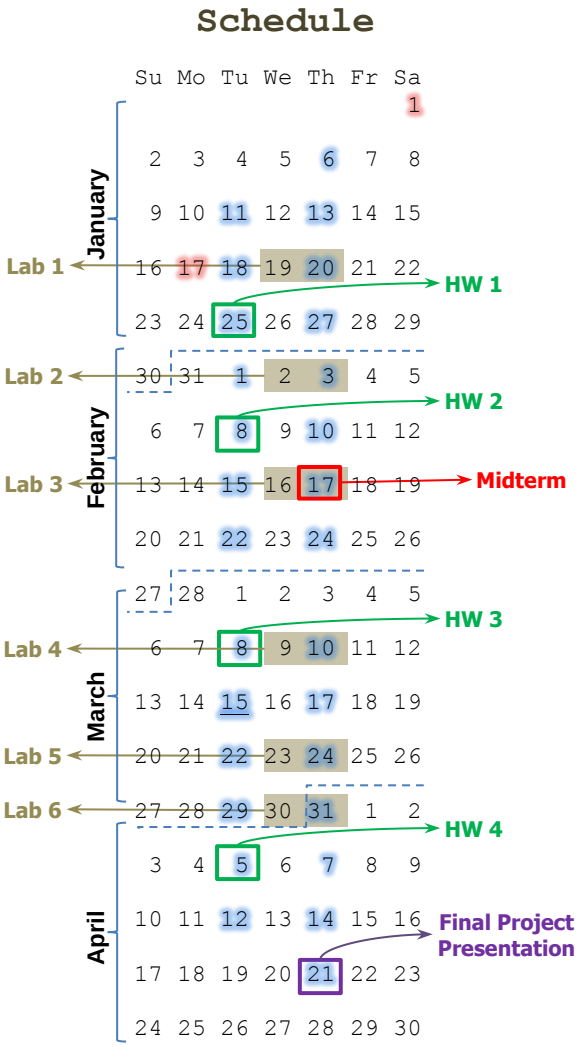
|---|---|---|---|
| **Homeworks:** | 20% | **Midterm Exam**: | 22% (February 17th, 7:30 – 9:17 pm) |
| **Laboratory:** | 36% | **Final Project**: | 22% (April 21st, 7:00 – 10:00 pm) |

- **Homeworks:** Homework assignments are meant to strengthen your conceptual understanding of the topics. Completing homework assignments is a key component of this course as it will help students master the course material and prepare them for the exams.
  Homeworks will be posted according to the schedule (green rectangles). Students have one week to turn in the completed assignments in class. Late submissions are NOT accepted.

- **Midterm Exam:** Closed-books, closed-notes, in-class exams. Students are not allowed to take the exams neither before nor after the exam date. Make-up exams are given *only* under extreme circumstances (e.g.: medical emergency, jury duty).

- **Laboratory:** This important component of the class will reinforce your understanding of the topics. There will be six (6) labs throughout the semester.
  TAs will be present every week during the regularly scheduled laboratory times. Students can work during those times or at any other time and place.
  Depending on the lab assignment, students have 1 or 2 weeks to complete them and have them checked off by the TA.
  * *There is a late policy on laboratory assignments*

- **Final Project:** Students will work in groups (up to 4) in a Final Project. Each group will prepare an oral presentation and submit a final report. Presentations will take place on April 21st.




## GRADE ASSIGNMENT:

| | | |
|---|---|---|
| 96-100 | A | 4.0 |
| 90-95 | A- | 3.7 |
| 85-89 | B+ | 3.3 |
| 80-84 | B | 3.0 |
| 72-79 | B- | 2.7 |
| 66-71 | C+ | 2.3 |
| 60-65 | C | 2.0 |
| 56-59 | C- | 1.7 |
| 53-55 | D+ | 1.3 |
| 50-52 | D | 1.0 |
| 49 and below | F | 0.0 |

## LABORATORY MATERIALS

- **Hardware**: Nexys™ A7 FPGA Trainer Board - Option: A7-50T (you can also use the Nexys™-4 DDR Artix-7 FPGA Board)
  ✓ To order: https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
  Go to: Get Academic Pricing ($171.75)

- **Software**:
  ✓ MATLAB® or Octave (open-source version of MATLAB).
  ✓ Vivado ML Standard Edition (2021.1 version or earlier) (free software, formerly known as Vivado HL Webpack)
  To download: http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

# OUTLINE OF TOPICS

| | | |
|---|---|---|
| **Digital System Design** | ▪ Components: Datapath circuit, Control circuit.<br>▪ Design examples: Simple processor, Debouncer, Banner on 7-seg displays, Binary to BCD algorithm.<br>▪ Extra Topics:<br>✓ Counter Design.<br>✓ Linear Feedback Shift Registers (Example: CRC), Memory Decoding.<br>✓ Practical aspects: flip flop timing parameters, reducing output rate. | |
| **Computer Arithmetic** | Unsigned/signed integer numbers | ▪ Addition/subtraction, multiplication, division<br>▪ Arithmetic units for integers. Comparators, Arithmetic Logic Unit (ALU), Barrel Shifter. |
| | Fixed-point (FX) arithmetic | ▪ Addition/subtraction, multiplication, division.<br>▪ FX arithmetic units.<br>▪ Truncation/Rounding/Saturation. |
| | Floating-point (FP) arithmetic | ▪ Addition/subtraction, multiplication, division.<br>▪ FP Arithmetic units |
| **External Peripherals: Interfacing** | ▪ Serial Comm.: UART, PS/2 (Keyboard/mouse), SPI (accelerometer), $I^2C$ (Temp. Sensor)<br>▪ PWM: Tri-color LEDs, Audio output.<br>▪ PDM: Microphone: ADMP421.<br>▪ Display: 7-segments, LCD, VGA, HDMI<br>▪ SRAM/DDRRAM, SD card. | |
| **Special-Purpose Circuits and Techniques** | ▪ CORDIC: Computation of trigonometric and hyperbolic functions<br>▪ Square Root, BCD Adder, CSA: Adder and Multiplier.<br>▪ Look-Up Table method: Pixel processor for gamma correction, contrast stretching, etc.<br>▪ Multiply-and-accumulate (MAC) circuit, Wallace multipliers, Booth recording.<br>▪ FPGA Resources: CLBs, FIFOs, BlockRAMs, DSPs, Clock Managers, XADCs. | |
| **Pipelining and unfolding** | ▪ Iterative, array, and pipelined array designs<br>▪ Multi-operand addition: iterative (accumulator) vs. pipelined array (adder tree)<br>▪ Multiplier and Divider: iterative vs. pipelined array<br>▪ CORDIC: iterative vs. pipelined array | |
| **Microprocessor Design** | ▪ Computer Hardware Organization: Single/Multiple-Cycle Hardwired Control, Instruction Set<br>▪ Memory technology: RAM/ROM, FIFOs. SRAMs, DDRRAM, Flash. | |

VHDL: The shaded rows are the aspects of VHDL description and coding techniques that will be covered in this course.

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|---|---|
| **Introduction** | ▪ Design Flow: Design Entry, Behavioral/Timing Simulation, Mapping, Implementation<br>▪ Data Types and Description of Logic Gates<br>▪ VHDL Testbench Generation |
| **Concurrent Description** | ▪ Concurrent statements: 'with-select', 'when-else'<br>▪ Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux. |
| **Behavioral Description** | ▪ Asynchronous processes.<br>▪ Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux.<br>▪ Sequential statements: 'if-else', 'case', 'for-loop' |
| **Structural Description** | ▪ Hierarchical design: Use of port-map, for-generate<br>▪ Examples: Adder, Multiplier, Arithmetic Logic Unit, Look-up Table |
| **Sequential Circuits** | ▪ Synchronous processes: flip-flops, counters, registers<br>▪ Description of Finite State Machines (FSMs)<br>▪ Testbench: generating clock stimulus |
| **Parameterization** | ▪ Use of for-generate, if-generate in VHDL.<br>▪ Custom-defined data types, arrays (e.g.: std_logic_2d), packages, functions, procedures.<br>▪ Generic testbenches |
| **I/O Text files** | ▪ Synthesis: Reading input text files<br>▪ Simulation: Reading input text files and writing output text files. |
| **Miscellaneous Topics** | ▪ Embedding counters and registers inside ASM diagrams.<br>▪ Using Xilinx primitives: BRAMs, FIFOs, etc. |

# OUTLINE OF COURSE TOPICS, ASSOCIATED ASSIGNMENTS AND REFERENCE MATERIAL.

TOPICS SHADED IN GRAY: SYNCHRONOUS LECTURES (ZOOM)

TOPICS SHADED IN RED: ASYNCHRONOUS LECTURES (PANOPTO)

| Week | | Unit | Topics | Associated Material | Assignments |
|---|---|---|---|---|---|
| 1 | 01/06 | 1 | Class policies. Class structure. Abstraction Layers in Computing | Syllabus | |
| | | | Digital System Design, Debouncer, Bit-counting circuit, log2, GCD | Lecture Notes – Unit 1 | |
| 2 | 01/11 | 1 | Digital System: Leading Zero Detector (LZD), Timing Diagram | Lecture Notes – Unit 1 | |
| | | 1 | *VHDL*: digital system design: log2 | VHDL for FPGAs Tutorial # 7 | |
| | 01/13 | 1 | Digital System: Microprocessor, Binary to BCD algorithm<br>*VHDL*: digital system design: super counter<br>LFSRs, Practical Aspects | Lecture Notes – Unit 1<br>VHDL for FPGAs Tutorial #7 | |
| 3 | 01/18 | 2 | Computer Arithmetic: Unsigned/signed integer numbers<br>Addition/subtraction, Multiplication, Division | Lecture Notes – Unit 2 | *Laboratory 1* |
| | 01/20 | 2 | Fixed-point (FX) Arithmetic<br>Operations: addition/subtraction | Lecture Notes – Unit 2 | |
| 4 | 01/25 | 2 | Fixed-point (FX) Arithmetic: multiplication, division<br>FX Arithmetic Units. Truncation/Rounding/Saturation | Lecture Notes – Unit 2 | Homework 1 |
| | 01/27 | 2 | Floating-Point (FP) Arithmetic | Lecture Notes – Unit 2 | |
| 5 | 02/01 | 2 | Floating-Point (FP) Arithmetic: addition/subtraction, multiplication, division | Lecture Notes – Unit 2 | *Laboratory 2* |
| | 02/03 | 2 | Floating-Point (FP) Arithmetic: hardware architectures | Lecture Notes – Unit 2 | |
| 6 | 02/08 | 3 | External Peripherals – Interfacing: 7-seg serializer, stopwatch, UART, PS/2.<br>*VHDL: Embedding counters, registers inside ASM diagrams* | Lecture Notes – Unit 3<br>VHDL for FPGAs Tutorial # 7 | Homework 2 |
| | 02/10 | 3 | Overview of Digital Sensors<br>External Peripherals: SPI | Lecture Notes – Unit 3 | |
| 7 | 02/15 | 3 | External Peripherals: I²C<br>*VHDL: parameterization introduction* | Lecture Notes – Unit 3<br>VHDL for FPGAs Tutorial # 8 | *Laboratory 3* |
| | 02/17 | | Midterm Exam | | |
| 8 | 02/22 | 3 | External Peripherals - Interfacing: PWM, PDM<br>*VHDL: custom-defined data types, packages, functions, procedures* | Lecture Notes – Unit 3<br>VHDL for FPGAs Tutorial # 9 | |
| | 02/24 | 4 | CORDIC<br>Square Root architectures | Lecture Notes – Unit 4 | |
| 10 | 03/08 | 4 | *VHDL: Synthesis: Reading input files*<br>*VHDL: Simulation: Reading/writing text files* | Lecture Notes – Unit 4<br>VHDL for FPGAs Tutorial # 9 | *Laboratory 4*<br>Homework 3 |
| | 03/10 | 4 | BCD Adder, CSA (Adder, multiplier)<br>Look-Up Table Method. MAC<br>FPGA Resources (BRAM, MMCM). | Lecture Notes – Unit 4 | |
| 11 | 03/15 | 5 | Pipelining and Unfolding: Introduction<br>Pipelining and Unfolding: Examples | Lecture Notes – Unit 5 | |
| | 03/17 | 6 | Microprocessor Design: Intro, Generic CPU Model | Lecture Notes – Unit 6 | |
| 12 | 03/22 | 6 | Single-Cycle Hardwired Control – VBC: Intro, Instruction Set | Lecture Notes – Unit 6 | *Laboratory 5* |
| | 03/24 | 6 | Memory Overview | Lecture Notes – Unit 6 | |
| 13 | 03/29 | 6 | Single-Cycle Hardwired Control – i) VBC (example), ii) Simple Computer | Lecture Notes – Unit 6 | *Laboratory 6* |
| | 03/31 | 6 | Simple Computer: examples, instruction decoder. Instruction load control | Lecture Notes – Unit 7 | |
| 14 | 04/05 | 6 | PicoBlaze: Introduction, components, Instruction Set | Lecture Notes – Unit 6 | Homework 4 |
| | 04/07 | 6 | PicoBlaze: Program Flow Control: Subroutines, execution examples. | Lecture Notes – Unit 6 | |
| 15 | 04/12 | 6 | Picoblaze: Program Flow Control: I/O, Interrupts | Lecture Notes – Unit 6 | |
| | 04/14 | 6 | PicoBlaze: Examples | Lecture Notes – Unit 6 | |
| 16 | 04/21 | | Final Project – Presentation | | |

# TECHNICAL ASSISTANCE

- If you have general questions about the course (such as due dates, content, etc.) or trouble accessing any of the content in this course, please contact the instructor.
- For Moodle (or Zoom) technical issues that you cannot resolve on your own, please contact the e-LIS (e-Learning and Instructional Support) office:
  - ✓ e-LIS Helpdesk Phone: (248) 805-1625
  - ✓ Submit a Moodle help ticket

# REQUIRED TECHNOLOGY AND BACKUP PLAN

- To fully participate in this class, you will need an internet connected computer with the most updated version of your favorite web browser installed.
  - ✓ In the event that your computer crashes or internet goes down, it is essential to have a "backup plan" in place where you are able to log in using a different computer or travel another location that has working internet.
  - ✓ Students can access the SECS lab software (including Vivado) via Remote Desktop service. For assistance, contact the SECS technology office.
    - This can be helpful for code design, syntax checking, and simulation. However, for hardware verification, students need to physically connect the FPGA Board to the computer and test the circuit on the board (this step cannot be done remotely).
- Your computer should be able to run the Vivado software. Go here for a description of operating system support.
- Any files you intend to use for your course should be saved to a cloud solution (Google Drive, Dropbox, etc.) and not to a local hard drive, USB stick or external disk. Saving files this way guarantees your files are not dependent on computer hardware that can fail.
- In the event of a snow day that coincides with a quiz or exam, the test might (at the instructor's discretion) be administered online. The instructor will post the quiz or exam as a pdf file and students need to post their work as a pdf file. In order to do this, students need to be proficient in editing pdfs or generating pdfs out of scanned pages or pictures.

## OPTIONAL ONLINE HOMEWORK SUBMISSION

- Students have the option to submit homework assignments online (via Moodle) as one pdf file. If a student uses this option, it is the student's responsibility to:
  - ✓ Ensure that the submitted file is correct. Corrupted, unrelated, or invalid files will be assigned **0** (no exceptions).
  - ✓ Submit the assignment on time (by 9:17 pm on the due date). Late submissions will NOT be accepted.
- If the student submits an online and a hard-copy assignment, only the hard-copy submission will be graded.

# CLASS POLICIES

- **No Credit Policy**: A grade of 0.0 will be given to students not receiving 60% in the Laboratory category and to students not participating in the Final Project, regardless of their performance in other parts of the course.

- **The instructor is expected to**:
  - ✓ Grade assignments within a week (or two when it comes to homeworks) of the assignment deadline.
  - ✓ The instructor will login into the course every day, at least 5 days a week.
  - ✓ Respond to emails and to Q&A forums replies within 1-2 days.

- **Students are expected to**:
  - ✓ Ensure that their computer is compatible with Moodle.
  - ✓ Follow the calendar of events and complete all assignments by their deadline. Students are responsible for ensuring the timely and correct submission of their assignments (should an issue arise with Moodle; students can email the assignment to the instructor as a last resort by the deadline).
  - ✓ Respond to emails within 2 days
  - ✓ Participate in a thoughtful manner
  - ✓ Respect rules of etiquette
    - Respect your peers and their privacy
    - Use constructive criticism
    - Refrain from engaging in inflammatory comments.

- **E-mail communication**: The instructor will only respond to emails from students that use their Oakland.edu account. Answering student emails from an email other than an Oakland.edu email is in violation of FERPA because the identity of the sender or receiver cannot be verified.

- **Course Questions & Answer Forum**: Students are encouraged to use this forum to post questions (associated with the course content) that they deem of interest to their classmates. The instructor will intervene periodically.

- **Laboratory**: Students must be aware of their Laboratory section (e.g.: 002, 003, …). This will be used to determine whether a student is late in their laboratory submission. Students are advised to attend on the day of their respective Laboratory Section. However, students can attend any other Laboratory Section if there is space available.
  - ✓ For every laboratory, students must demo their work to the TA. Then, they must submit their work files to Moodle. Work files submitted without demoing will not be considered.
    - The TA will sign off the lab sheet. Students must also submit the signed lab sheet to Moodle.
  - ✓ Note that the laboratory work is individual, and students are not allowed to submit their work in groups.

- **COVID-19 guidelines:** Students are strongly advised to refer to the following site for up-to-date information regarding Daily Health Screenings, Masking, Social Distancing, etc. Classroom procedures are outlined here.
  - ✓ Students can only join the classroom or laboratory when they are cleared with the appropriate green banner display on the Daily Screening Form.
  - ✓ OU has instituted a mandatory indoor mask policy on campus regardless of vaccination status. A properly worn mask must cover the nose and mouth. Face shields alone will NOT serve to meet the mandatory mask policy. If a student comes to the classroom or laboratory without a mask (or improperly worn), the instructor or TA will ask the student to properly put a mask or leave.
  - ✓ OU takes these guidelines very seriously. Any non-compliance incident will be immediately referred to the Dean of Students' Office (OUPD may be called if a student is disruptive). The instructor or TA may cancel the class lecture or laboratory session for the day.

- **Academic conduct policy**: All members of the academic community at Oakland University are expected to practice and uphold standards of academic integrity and honesty. Academic integrity means representing oneself and one's work honestly. Misrepresentation is cheating since it means students are claiming credit for ideas or work not actually theirs and are thereby seeking a grade that is not actually learned. Academic dishonesty will be dealt with seriously and appropriately. Academic dishonesty includes, but it is not limited to cheating on examinations, plagiarizing the works of others, cheating on lab reports, unauthorized collaboration in assignments, hindering the academic work of other students.

- **Special Considerations**: Students with disabilities who may require special consideration should make an appointment with campus Disability Support Services, 106 North Foundation Hall, phone 248 370-3266. Students should also bring their needs to the attention of the instructor as soon as possible. For academic help, such as study and reading skills, contact the Academic Skills/Tutoring Center, 103 North Foundation Hall, phone 248 370-4215.

- **Add/Drops**: The university policy will be explicitly followed. It is the student's responsibility to be aware of deadline dates for dropping courses.

- **Attendance**: It is assumed that the students are aware of and understand the university attendance policy. Attendance is mandatory and maybe monitored. Students are responsible for all material covered in classes that they miss. There will be no excuses for being late to exams.

- **Athlete Excused Absences**: Students shall inform the instructor of dates they will miss class due to an excused absence prior to the date of that anticipated absence. For activities such as athletic competitions whose schedules are known prior to the start of a term, students must provide their instructors during the first week of each term a written schedule showing days they expect to miss classes. For other university excused absences, students must provide the instructor at the earliest possible the dates that they will miss.

- **Special Circumstances:** The instructor should be notified as early as possible regarding any special conditions or circumstances which may affect a student's performance during the course timeframe (e.g., medical emergencies, family circumstances).

- **Mental Health Resources**: Oakland University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of support, services are available. For help, contact the OU Counseling Center in the Human Health Building at (248) 370-3465 or the SEHS Counseling Center at 250A Pawley Hall, (248) 370-2633, https://oakland.edu/counseling/sehs-cc/. Student resources can also be found at https://www.oakland.edu/deanofstudents/student-health-safety-resources/. For immediate 24/7 services contact Common Ground at https://commongroundhelps.org/#/ via chat or call or text the word "hello" to 1-800-231-1127.

- **Cellphones**: A ringing cellphone going off during a lecture is disruptive to other students as well as the instructor. Students are strongly advised to set their cellphones to vibrate (not ringing) and leave the classroom discretely to answer the phone.