

FLAPPY BIRD



VHDL FPGA

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PRESENTATION OVERVIEW



BACKGROUND

Group motivation
behind project



BREAKDOWN

Individual program
block analysis



OVERVIEW

Top-level block
diagram and overall
functionality



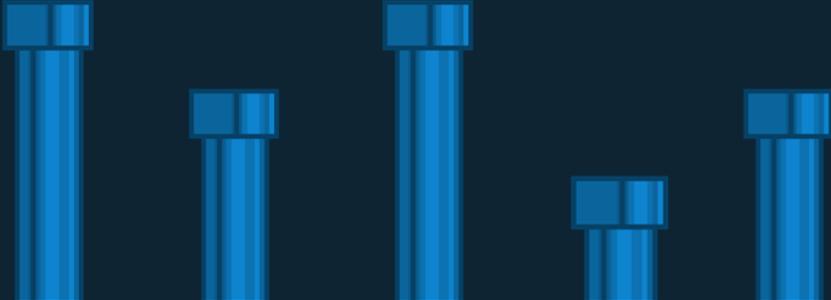
LESSONS LEARNED

Takeaways from
project and future
improvements



PERFORMANCE

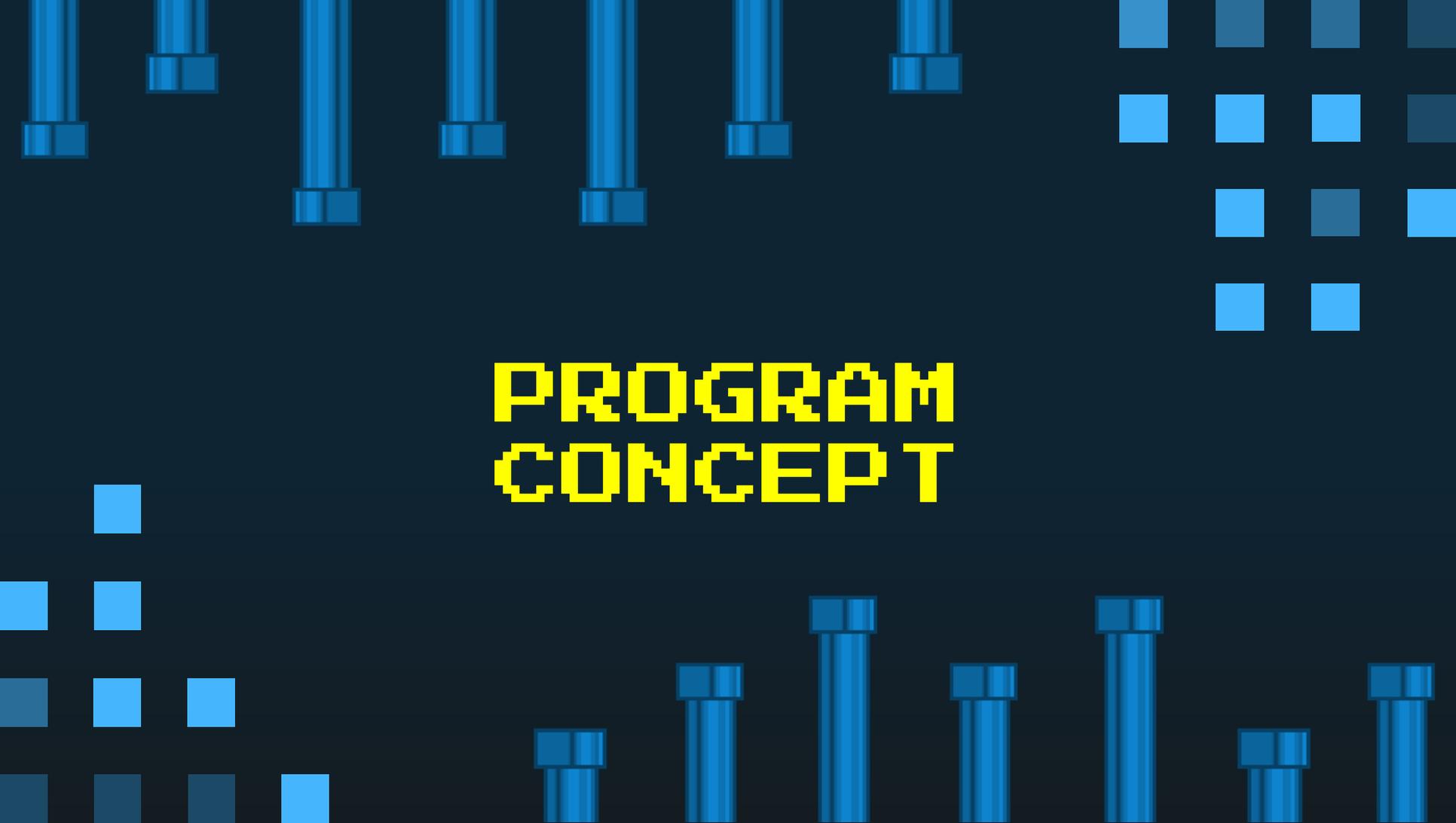
How well the design
performs overall



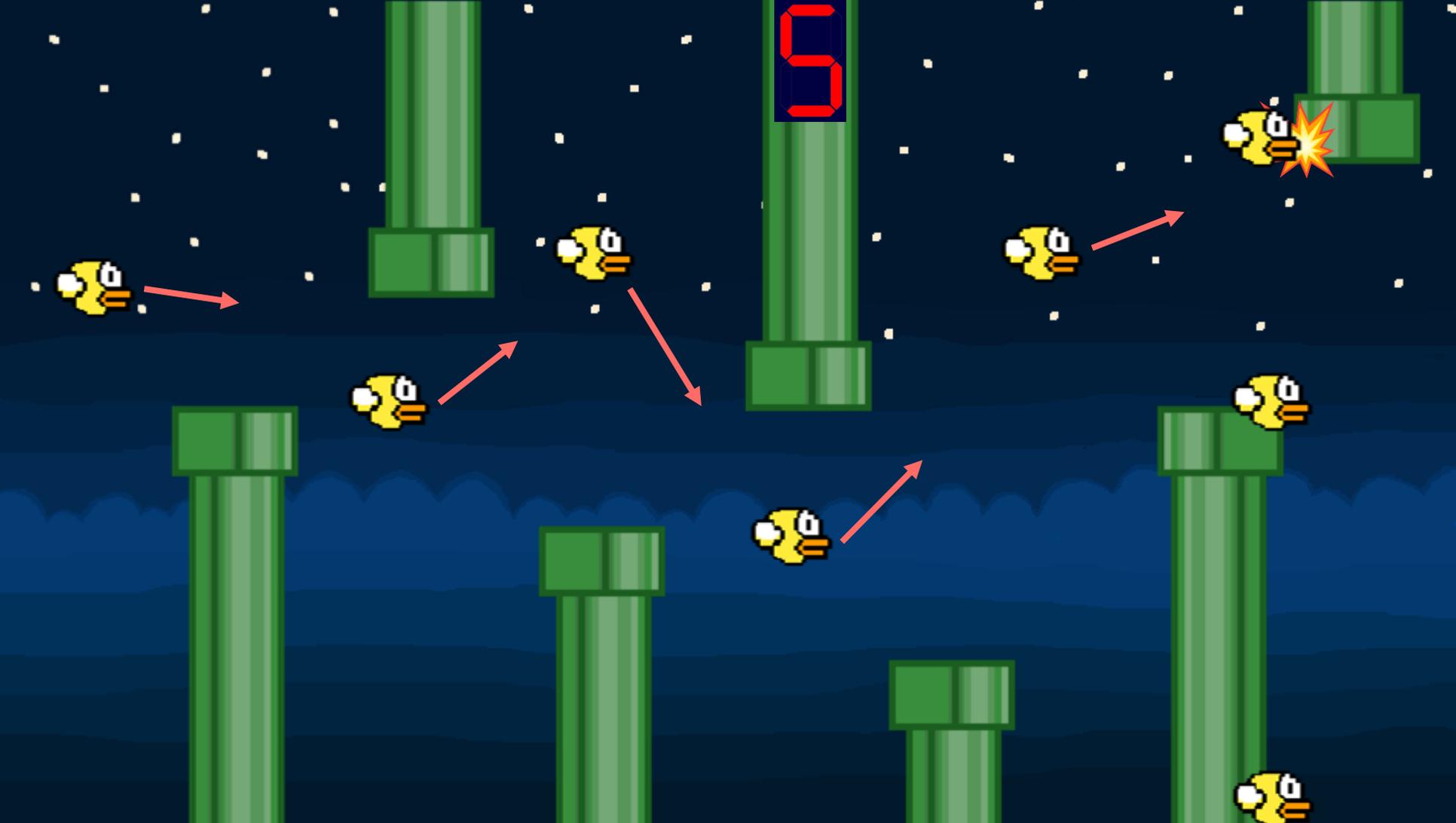
BACKGROUND

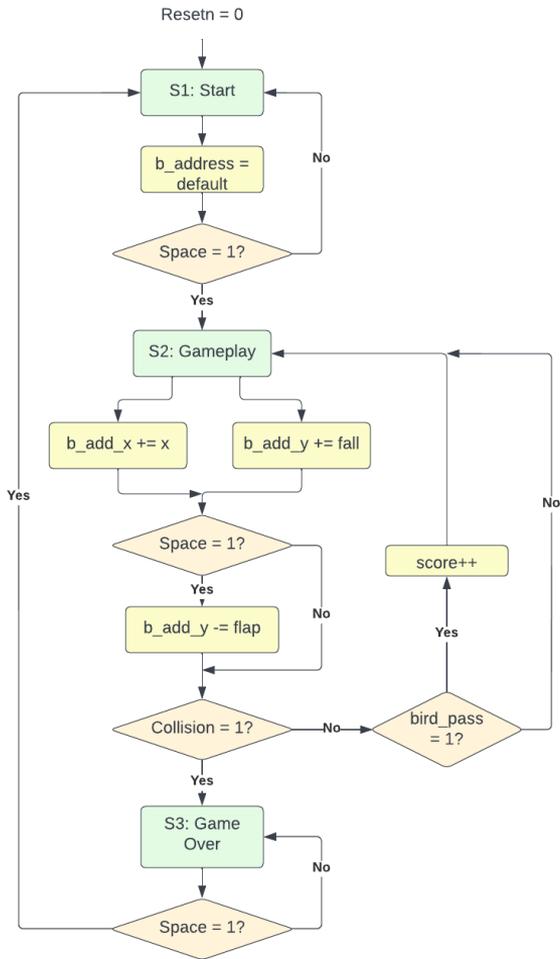
What motivated us to do this project?

- Common enjoyment of games
- VGA and PS/2 interfacing

The background features a dark blue field with several vertical blue bars of varying heights and widths, some with a darker blue base. On the right side, there is a grid of blue squares, some of which are slightly darker than others, creating a subtle pattern.

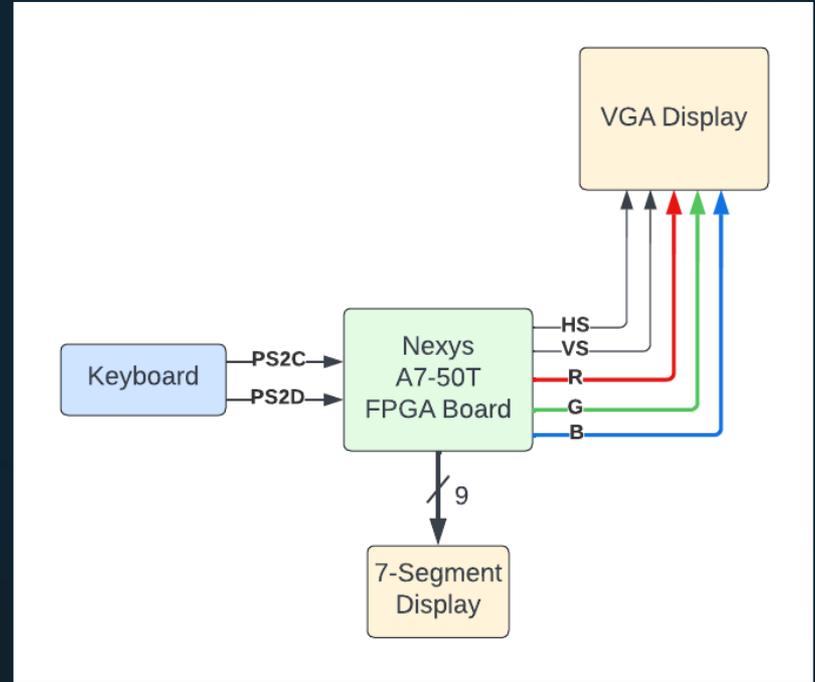
PROGRAM CONCEPT





PROGRAM FLOWCHART

PERIPHERAL CONNECTIONS

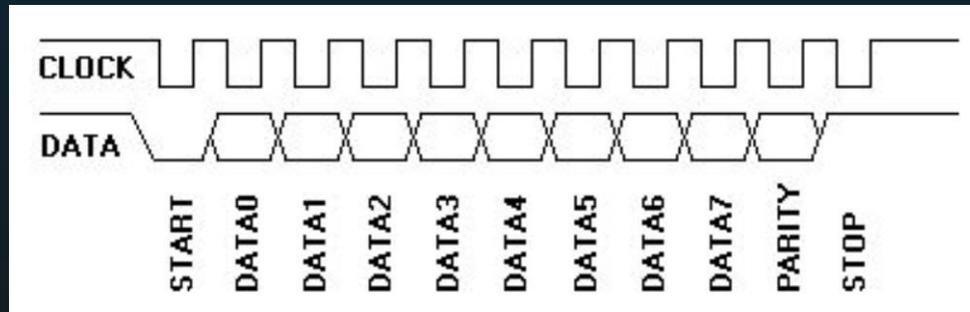


The background features a dark blue field with various decorative elements. On the left, there are several vertical blue bars of varying heights and widths, some with a darker blue base. On the right, there is a grid of blue squares, some solid and some with a darker blue center. The central text is in a bright yellow, pixelated font.

PROGRAM BREAKDOWN

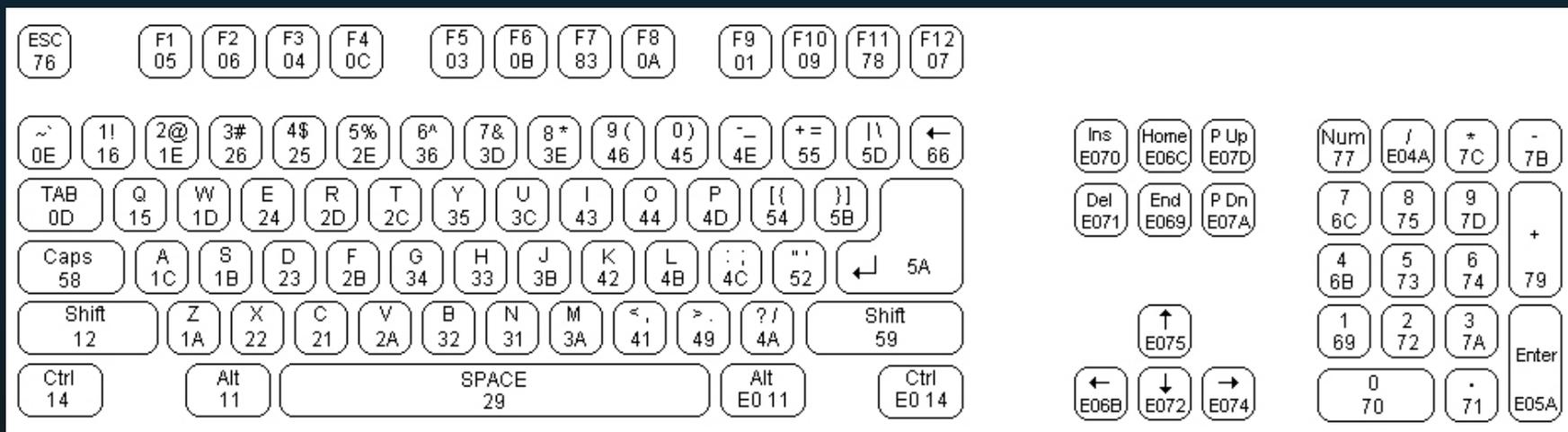
PS/2 PROTOCOL

- User game control
- Bidirectional synchronous serial protocol
- Data transmission = 11-12 bits
 - Start bit = '0'
 - 8 data bits
 - Little endian
 - Parity bit
 - Odd
 - Stop bit = '1'

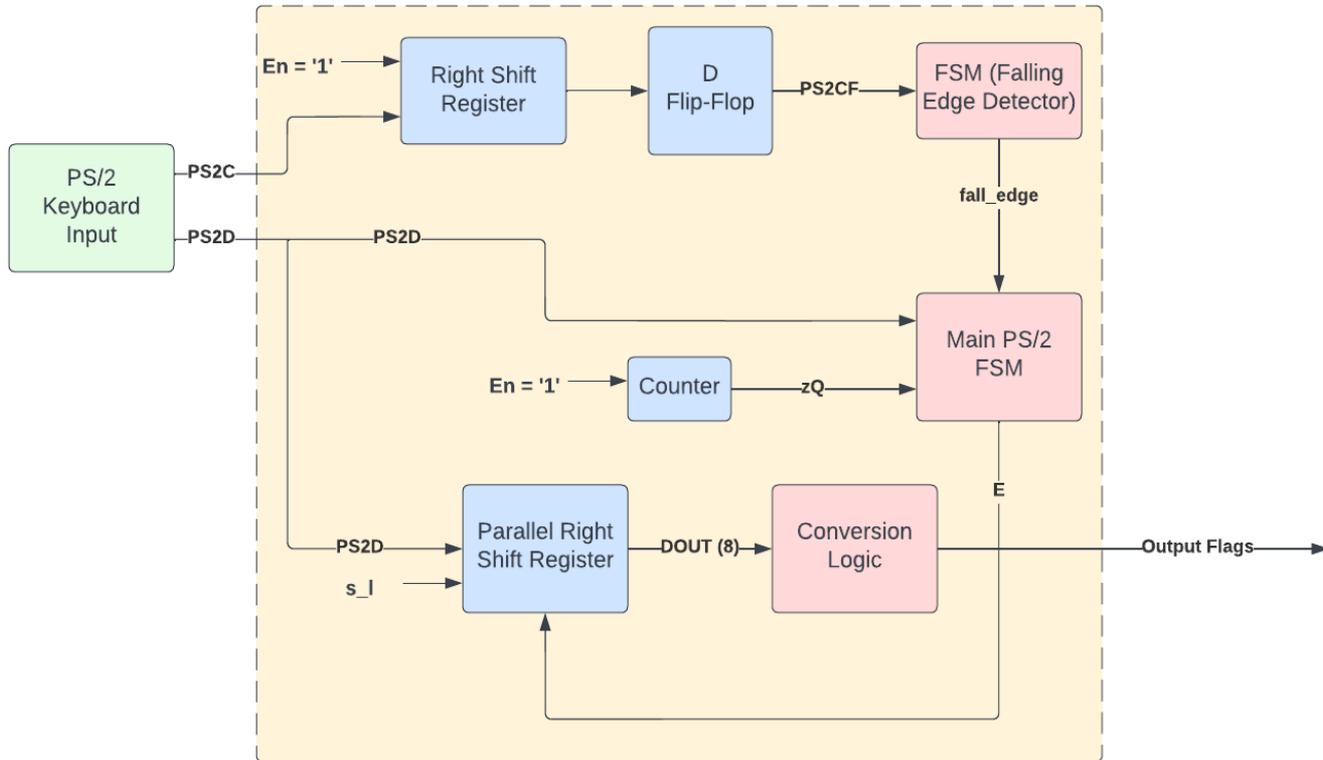


PS/2 PROTOCOL

- Strategy:
 - Decode 'DATA' signal
 - Set flags when desired keys pressed



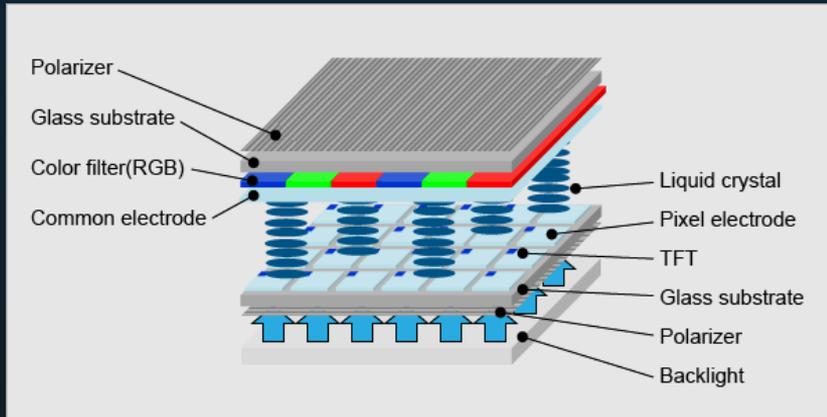
PS/2 PROTOCOL



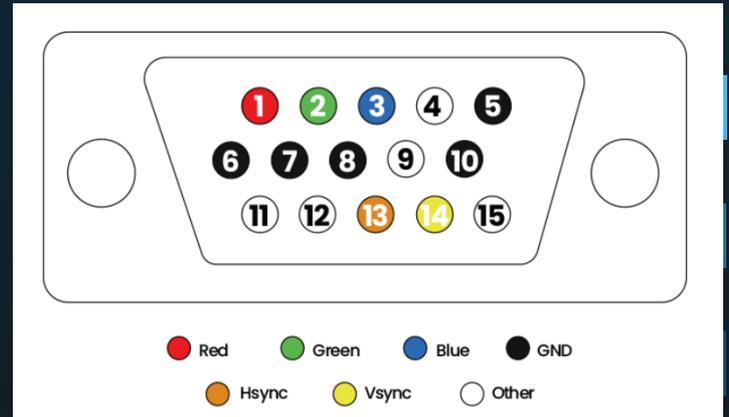
VGA DISPLAY PROTOCOL

Video Graphics Array

- 640 x 480 resolution (pixels)
- 256 color combinations
- 60 Hz refresh rate
- 15-pin connector



LCD Display

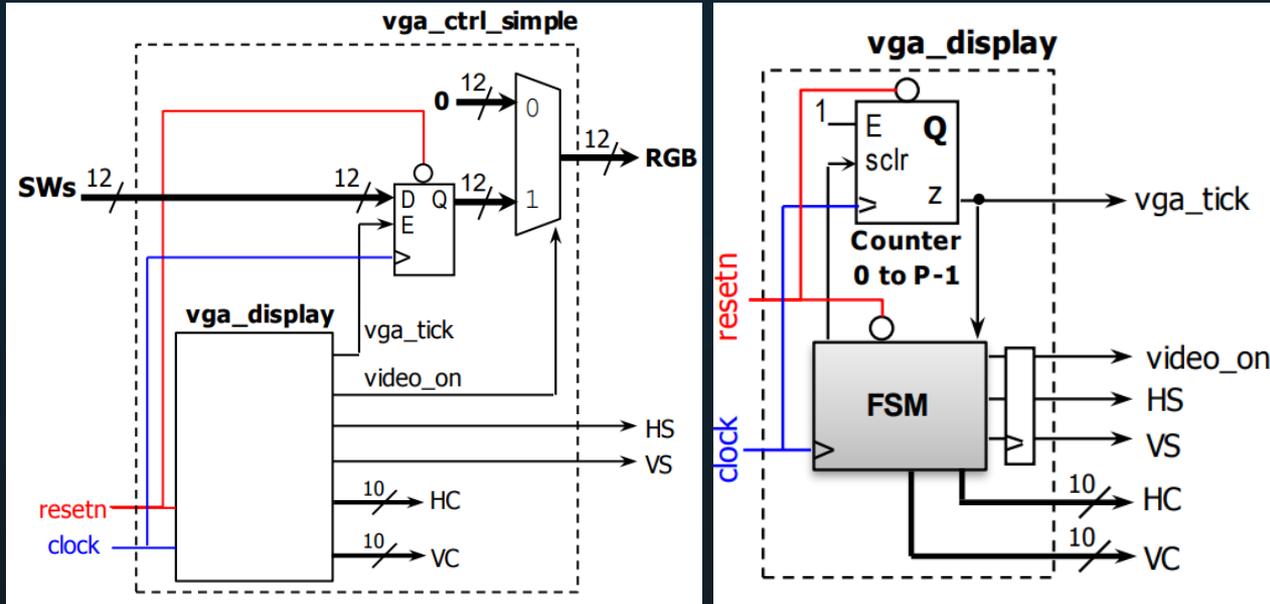


VGA Connector

VGA DISPLAY PROTOCOL

Video Graphics Array

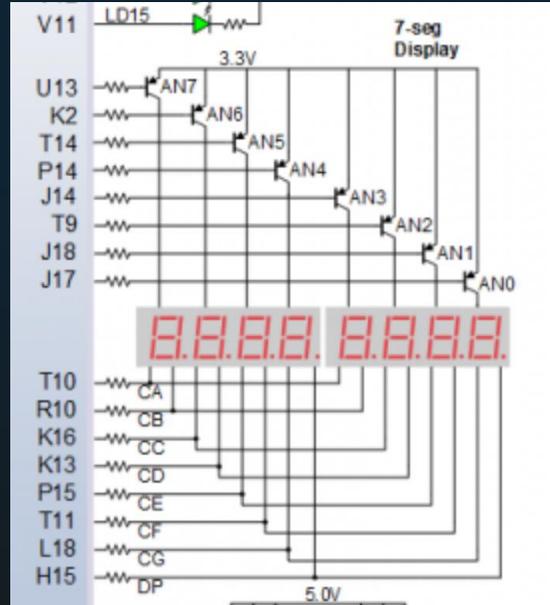
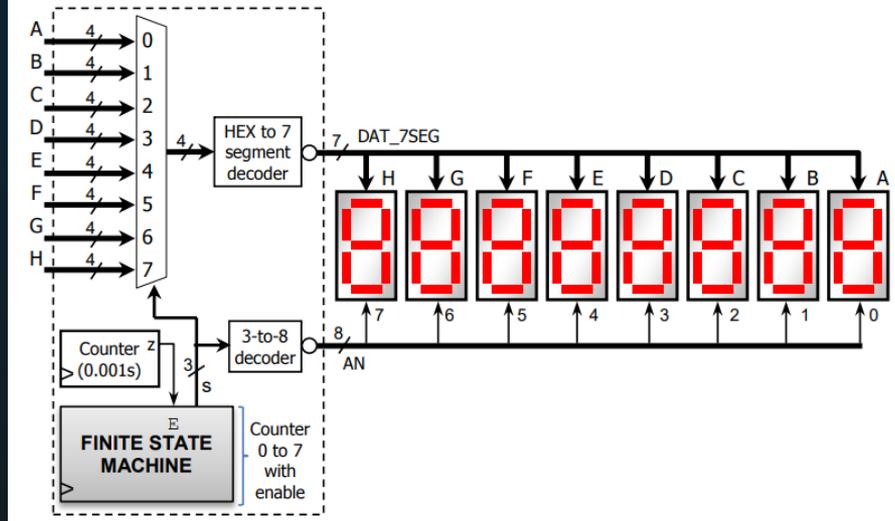
- Use HC,VC,HS, and VS to select pixel location
- RGB signal = color output for selected signal
- Use logic to dictate which pixel is displayed where



7-SEGMENT DISPLAY

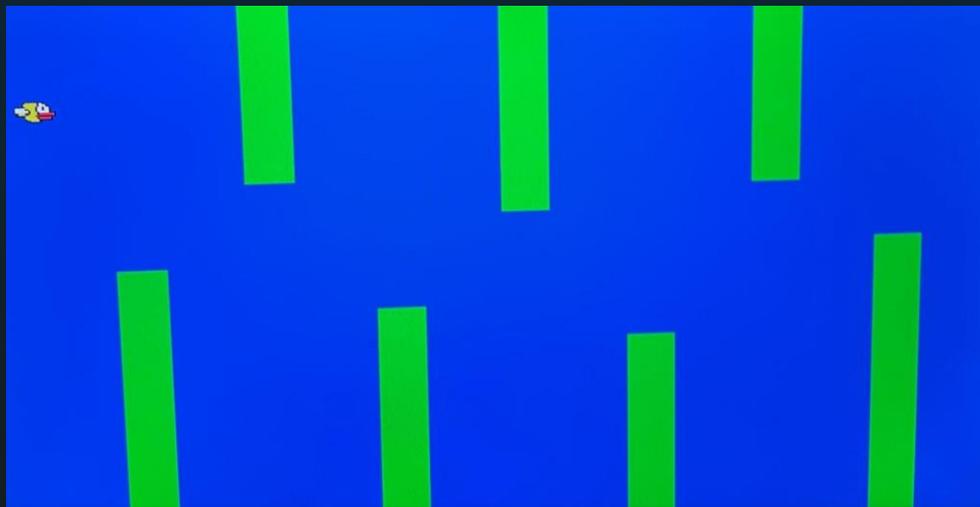
- On-board seven segment display
- Depicts game score
 - Score increments when bird passes obstacle

8-display Serializer: Eight 7-segment displays.



PROGRAM PERFORMANCE

- Quick response time
- Large sprite step
 - Simpler implementation
- Basic graphics
- Small playing field



PROGRAM DEMO

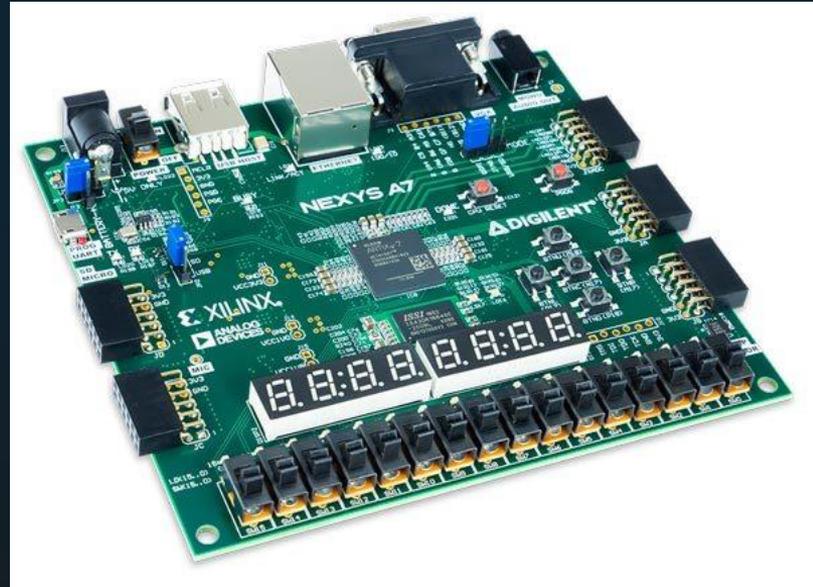
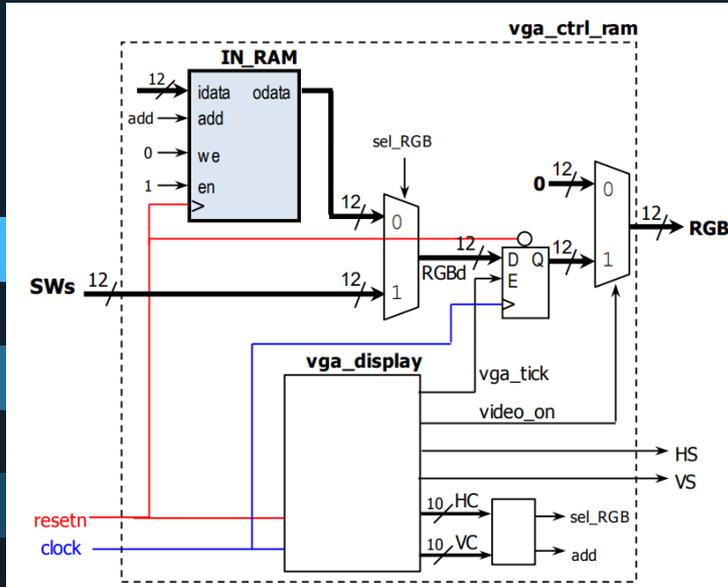
<https://youtube.com/shorts/JBdozbKbibE>

Another version of it:

<https://streamable.com/6ecfd2>

LESSONS LEARNED

- Initial plan: import graphics to FPGA
 - Nexys A7-50T RAM cannot handle extensive graphics
- Simple VGA control without using RAM has better performance



FUTURE IMPROVEMENTS

- Precise movement control of sprite
 - Bird movements confined to about 10 pixels either direction
- Variable level difficulty
- Use different board with larger RAM to have
 - Increase image quality
- Variable pipe size
 - Currently using pre-set pattern





THANK YOU!
ANY QUESTIONS?

We'd also like to give a special thank you to
Professor Llamocca for all of his help

WORKS CITED

- U. Zoltán, "Nexys-A7-50T-OOB" *GitHub*, 2006. [Online]. Available: <https://github.com/Digilent/Nexys-A7-50T-OOB/blob/master/src/hdl/Ps2Interface.vhd>. [Accessed: 01-Apr-2022].
- D. Llamocca, "VHDL Coding for FPGAs," *Reconfigurable Computing Research Laboratory*. [Online]. Available: <http://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html>. [Accessed: 1-Apr-2022].
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- A. Brown, "Nexys A7 Reference Manual," *Digilent Reference*. [Online]. Available: <https://digilent.com/reference/programmable-logic/nexys-a7/reference-manual>. [Accessed: 1-Apr-2022].