CAN Controller

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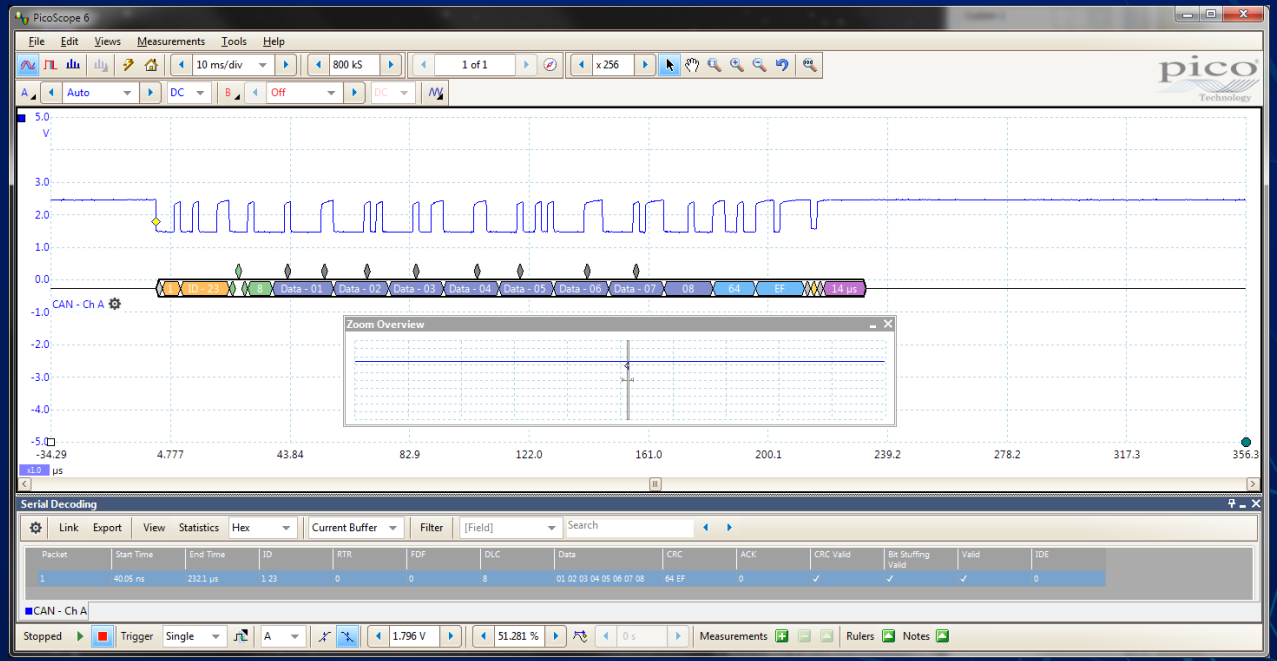
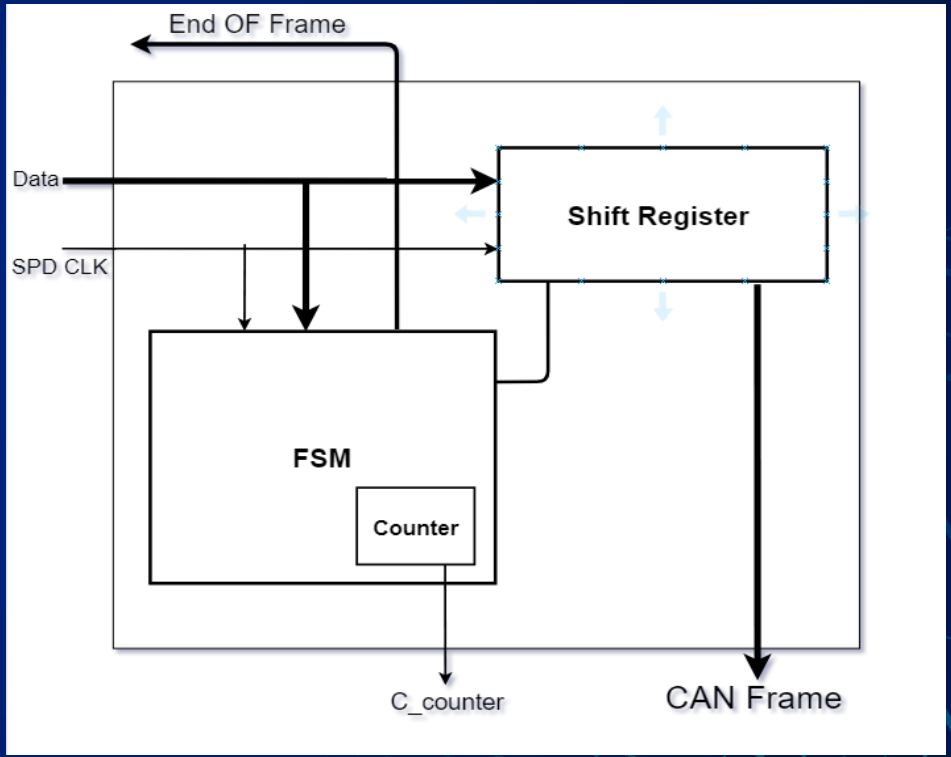
SERIAL DATA PROCESSOR

- Samples bits on the CAN bus.
- Synchronizes on rising / falling edges.



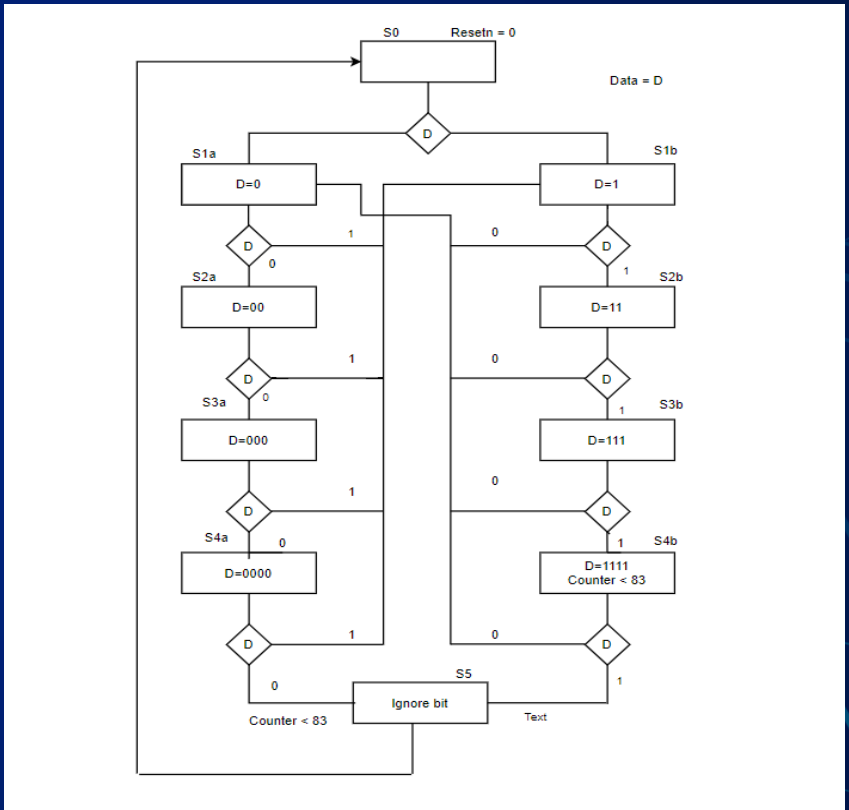
DESTUFFER

Using Shift register, counter, and the FSM, the destuffer's
main task is to filter the main data layout the actual CAN Frame
Also, the destuffer provides the bit count signal for the rest of the system.



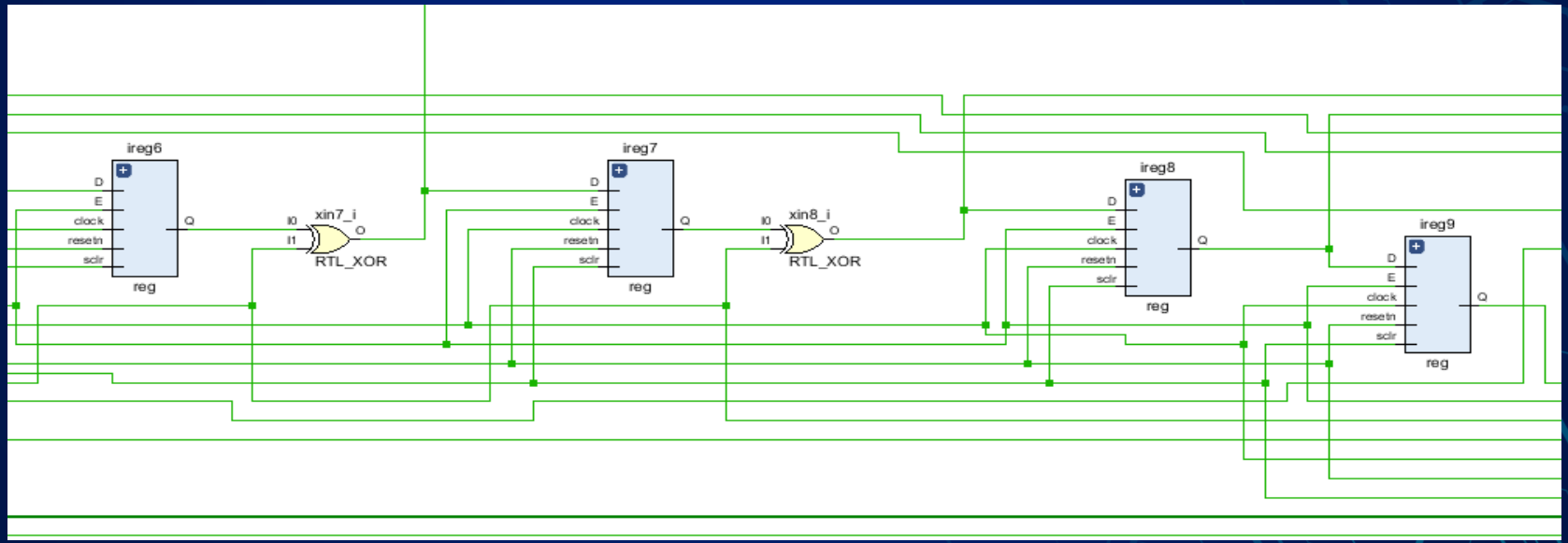
DESTUFFER FSM

FSM designed by containing ten states. Simple and efficient design.
Finally, The Destuffer sends EOF signal at the End of CAN Frame and wait for some time then Clear the counter and register.



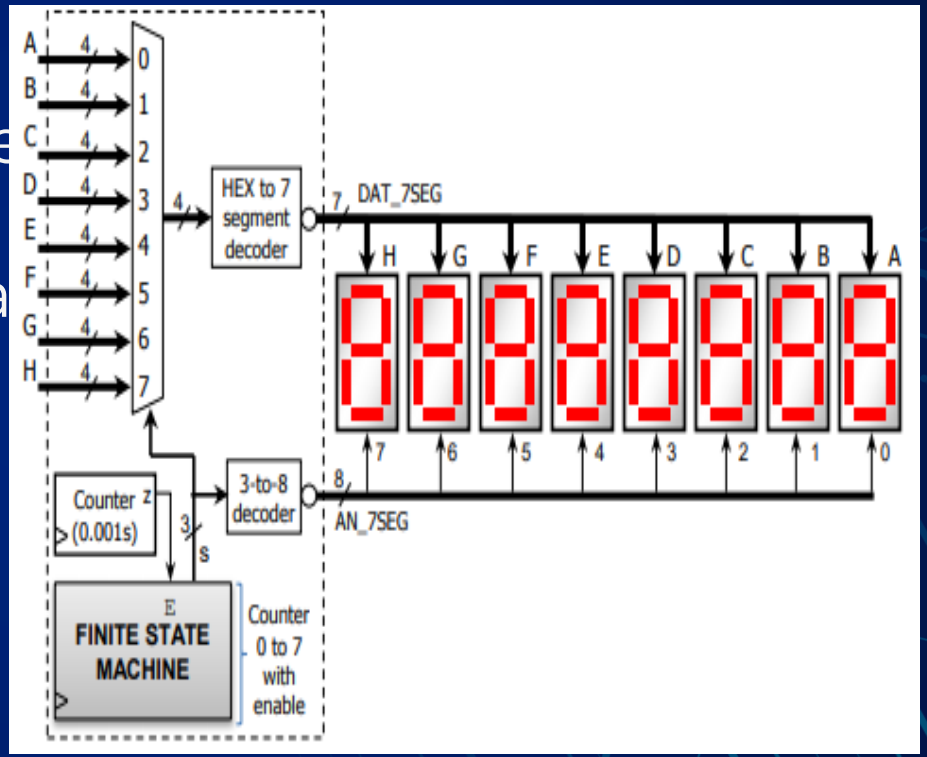
CYCLIC REDUNDANCY CHECK (CRC)

- Polynomial = $X^{15} + X^{14} + X^{10} + X^{8} + X^{7} + X^{4} + X^{3} + 1$
- Registers and XOR gates

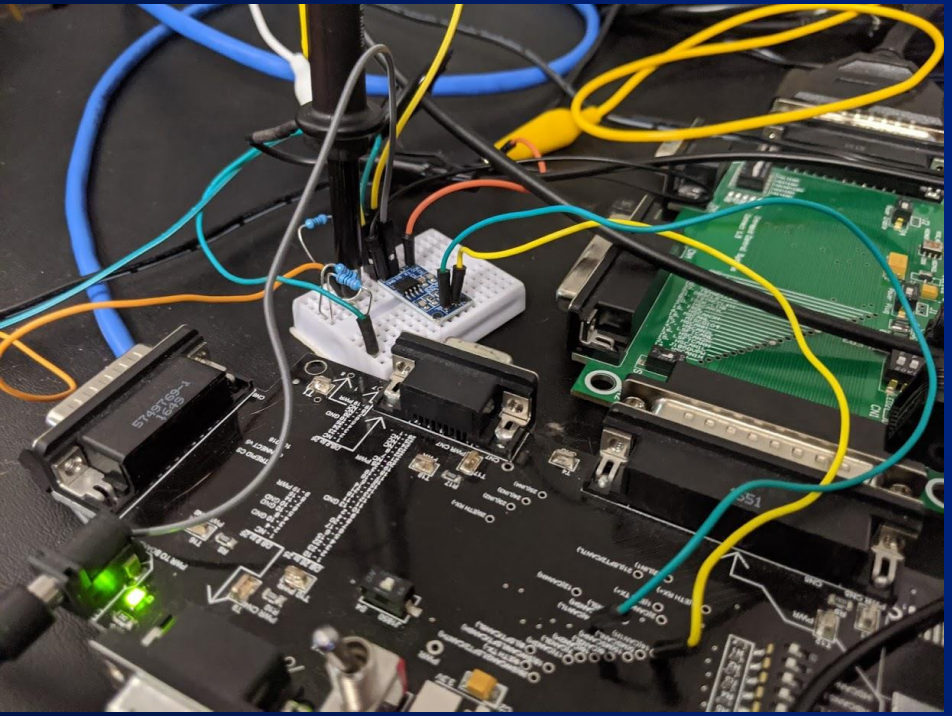


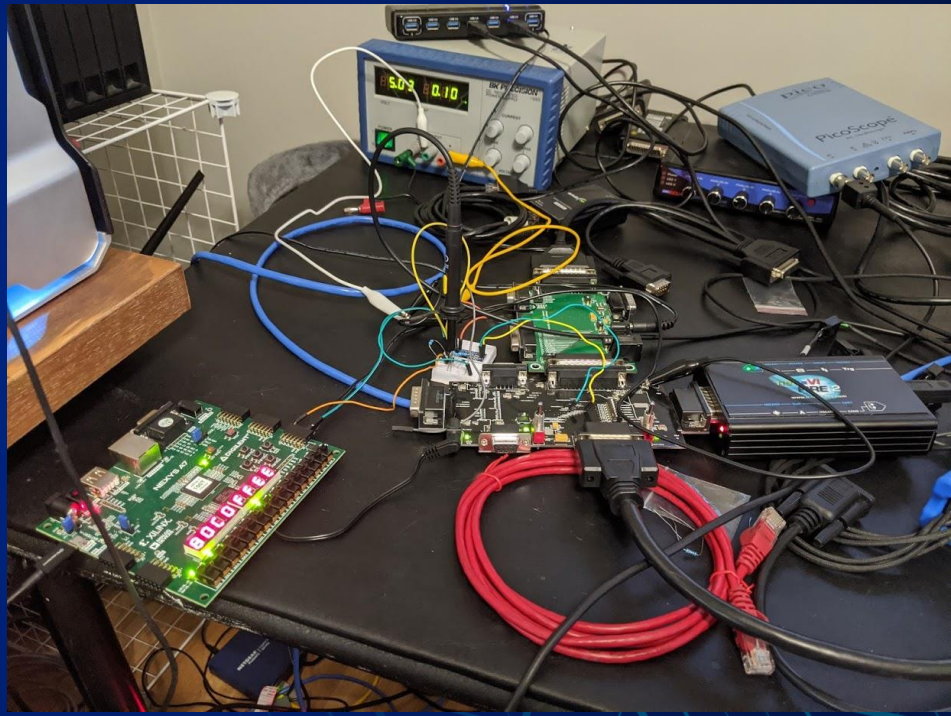
DATA EXTRACTION AND OUTPUT

- ARB_ID and ACK
  enabled Re
- Seven-Segment
  Seria

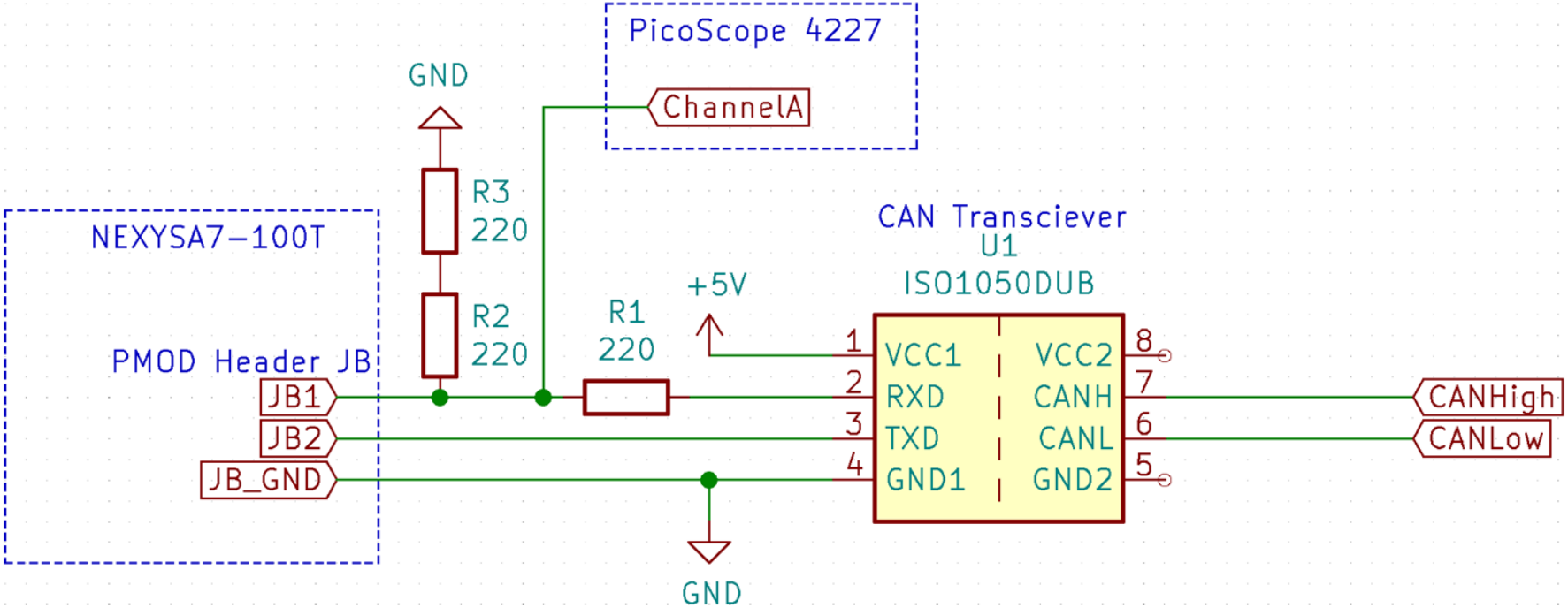


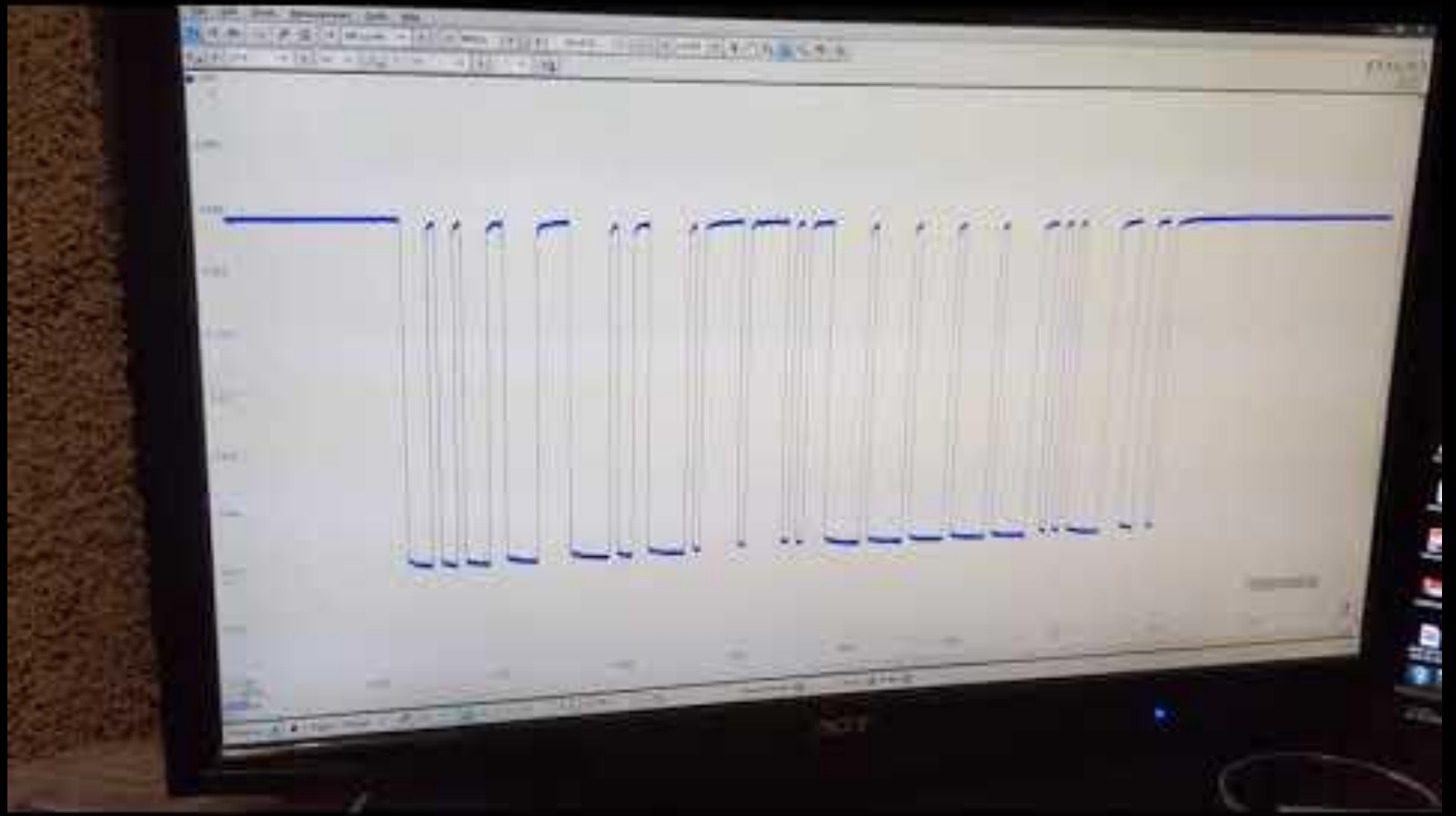
Electrical Assembly





Electrical Assembly





CONCLUSION AND SUMMARY

1. Fully functional in behavioural simulation
2. Physical implementation mostly functional
3. Generates CAN data output to seven segment display