Course Information

INSTRUCTOR	Daniel Llamocca
CONTACT INFO	email: llamocca@oakland.edu
OFFICE HOURS	Tuesday 2:00 to 4:00 pm @ Room EC-438, or by appointment
LECTURES	Tuesday/Thursday 7:30 pm - 9:17 pm @Room SFH-373 (South Foundation Hall)
LABORATORY	002: Wednesday 7:30 pm – 10:30 pm @ Room EC-562 003: Thursday 12:00 pm – 2:59 pm @ Room EC-562 TA: David Stern destern@oakland.edu

COURSE CATALOG DESCRIPTION: ECE 3710 – Computer Hardware Design (4 credits)

Development of components and techniques needed to design digital circuits and systems for controllers, computers, communication and related applications. Design and analysis of combinational and sequential logic circuits using a hardware description language such as VHDL, timing simulations, test benches, embedded cores. Design of special-purpose processors and their implementation in an FPGA. With Laboratory. Offered fall, winter, summer.
Prerequisite(s): ECE2700 or ECE 278 and major standing.

COURSE WEBPAGE

- The course material will be hosted on Moodle (moodle.oakland.edu). Grades will be periodically posted via this system.
- As a backup resource, the material will also be posted at: www.secs.oakland.edu/~llamocca/Winter2019_ece3710.html
- VHDL for FPGAs Tutorial: Available at the following permanent link: www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

TEXTBOOK:

- There is no required textbook. Students are encouraged to use the extra references.

EXTRA REFERENCES:

- Pong P. Chu, *FPGA Prototyping by VHDL examples: Xilinx Spartan-3 version*. John Wiley & Sons, 2011.
- M. Morris, C. Kime, T. Martin, *Logic and Computer Design Fundamentals*, Pearson Education , 5th edition, 2015
- S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, 3rd ed., McGraw Hill, 2009.
- Bryan J. Mealy, James T. Mealy, *Digital McLogic Design*, Free Range Factory, 2012.
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- Bryan Mealy, Fabrizio Tappero, Free Range VHDL, Free Range Factory, 2013
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- Peter J. Ashenden, The Designer's Guide to VHDL, 3rd ed., Elsevier, 2008.

COURSE OBJECTIVES

1. Design combinational and sequential components in VHDL. (1)
2. Describe how combinational and sequential components can be used to design a datapath and control unit for implementing digital systems. (1, 4)
3. Design custom architectures to interact with external peripherals. (2)
4. Design dedicated special-purpose processors using VHDL and synthesize them to an FPGA. (1,2,4)
5. Build a testbench for a digital system. (6)
6. Perform functional and timing simulation of a digital circuit described in VHDL. (1,2,4)
7. Work in a team environment to design a digital system and communicate the results in a written report and an oral presentation. (1,2,3,4,5,7)

ABET Course Outcomes:

1	2	3	4	5	6	7

GRADING SCHEME:

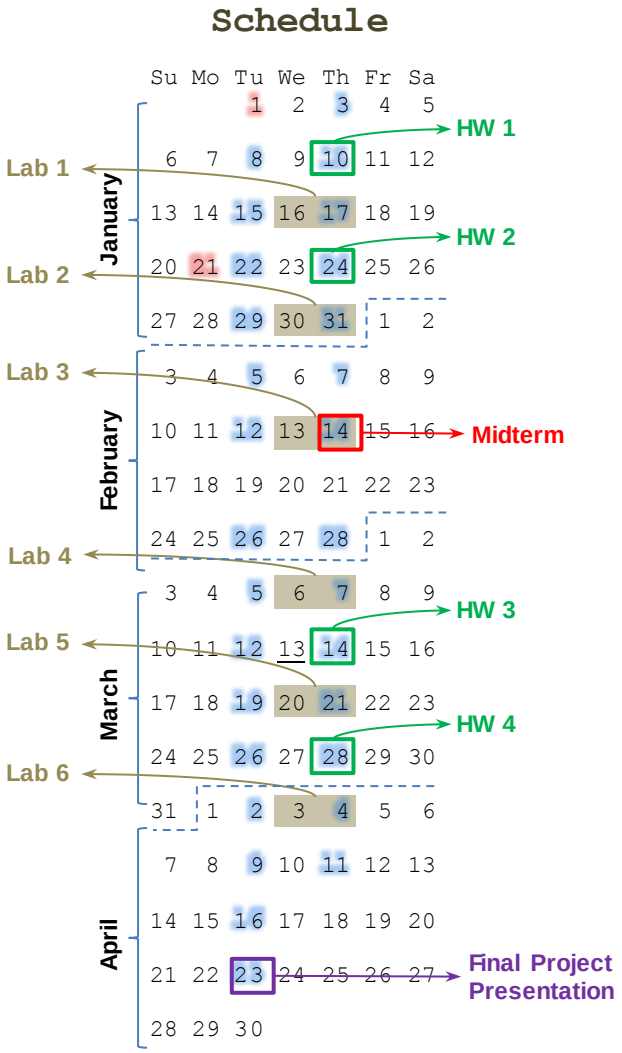
Homeworks:	20%	**Midterm Exam**:	25% (February 14th, 7:30-9:17 pm)
Laboratory:	30%	**Final Project**:	25% (April 23rd, 7:00-10:00 pm)

- **Homeworks:** Homework assignments are meant to strengthen your conceptual understanding of the topics. Completing homework assignments is a key component of this course as it will help students master the course material and prepare them for the exams.
  Homeworks will be posted according to the schedule (green rectangles). Students have one week to turn in the completed assignments in class. Late submissions are NOT accepted.

- **Midterm Exam:** Closed-books, closed-notes, in-class exams. Students are not allowed to take the exams neither before nor after the exam date. Make-up exams are given *only* under extreme circumstances (e.g.: medical emergency, jury duty).

- **Laboratory:** This important component of the class will reinforce your understanding of the topics. There will be six (6) labs throughout the semester.
  TAs will be present every week during the regularly scheduled laboratory times. Students can work during those times or at any other time and place.
  Students have one week to complete the lab assignments and have them checked off by the TA.

- **Final Project:** Students will work in groups (up to 4) in a Final Project. Each group will prepare an oral presentation and submit a final report. Presentations will take place on April 23th.



GRADE ASSIGNMENT:

96-100	A	4.0
90-95	A-	3.7
85-89	B+	3.3
80-84	B	3.0
72-79	B-	2.7
66-71	C+	2.3
60-65	C	2.0
56-59	C-	1.7
53-55	D+	1.3
50-52	D	1.0
49 and below	F	0.0

LABORATORY MATERIALS

- **Hardware**: Nexys™ A7 FPGA Trainer Board - Option: A7-50T (you can also use the Nexys™-4 DDR Artix-7 FPGA Board)
  - ✓ To order: https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
    Go to: Get Academic Pricing ($171.75)

- **Software**:
  - ✓ MATLAB® or Octave (open-source version of MATLAB).
  - ✓ Vivado HL Webpack Edition
    To download: http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

OUTLINE OF TOPICS

Digital System Design	▪ Components: Datapath circuit, Control circuit. ▪ Design examples: Simple processor, Debouncer, Banner on 7-seg displays, Binary to BCD algorithm. ▪ Extra Topics: ✓ Counter Design. ✓ Linear Feedback Shift Registers (Example: CRC), Memory Decoding. ✓ Practical aspects: flip flop timing parameters, reducing output rate.	
Computer Arithmetic	Unsigned/signed integer numbers	▪ Addition/subtraction, multiplication, division ▪ Arithmetic units for integers. Comparators, Arithmetic Logic Unit (ALU), Barrel Shifter.
	Fixed-point (FX) arithmetic	▪ Addition/subtraction, multiplication, division. ▪ FX arithmetic units. ▪ Truncation/Rounding/Saturation.
	Floating-point (FP) arithmetic	▪ Addition/subtraction, multiplication, division. ▪ FP Arithmetic units
External Peripherals: Interfacing	▪ Serial Comm.: UART, PS/2 (Keyboard/mouse), SPI (accelerometer), I^2C (Temp. Sensor) ▪ PWM: Tri-color LEDs, Audio output. ▪ PDM: Microphone: ADMP421. ▪ Display: VGA, HDMI ▪ SRAM/DDRRAM, LCD, SD card.	
Special-Purpose Circuits and Techniques	▪ CORDIC: Computation of trigonometric and hyperbolic functions ▪ Square Root, BCD Adder, CSA: Adder and Multiplier. ▪ Look-Up Table method: Pixel processor for gamma correction, contrast stretching, etc. ▪ Multiply-and-accumulate (MAC) circuit, Wallace multipliers, Booth recording. ▪ FPGA Resources: CLBs, FIFOs, BlockRAMs, DSPs, Clock Managers, XADCs.	
Pipelining and unfolding	▪ Iterative, array, and pipelined array designs ▪ Multi-operand addition: iterative (accumulator) vs. pipelined array (adder tree) ▪ Multiplier and Divider: iterative vs. pipelined array ▪ CORDIC: iterative vs. pipelined array	
Microprocessor Design	▪ Computer Hardware Organization: Single/Multiple-Cycle Hardwired Control, Instruction Set ▪ Memory technology: RAM/ROM, FIFOs. SRAMs, DDRRAM, Flash.	

VHDL: These are the aspects of VHDL description and coding techniques that will be covered in this course.

Introduction	▪ Design Flow: Design Entry, Behavioral/Timing Simulation, Mapping, Implementation ▪ Data Types and Description of Logic Gates ▪ VHDL Testbench Generation
Concurrent Description	▪ Concurrent statements: 'with-select', 'when-else' ▪ Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux.
Behavioral Description	▪ Asynchronous processes. ▪ Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux. ▪ Sequential statements: 'if-else', 'case', 'for-loop'
Structural Description	▪ Hierarchical design: Use of port-map, for-generate ▪ Examples: Adder, Multiplier, Arithmetic Logic Unit, Look-up Table
Sequential Circuits	▪ Synchronous processes: flip-flops, counters, registers ▪ Description of Finite State Machines (FSMs) ▪ Testbench: generating clock stimulus
Parameterization	▪ Use of for-generate, if-generate in VHDL. ▪ Custom-defined data types, arrays (e.g.: std_logic_2d), packages, functions, procedures. ▪ Generic testbenches
I/O Text files	▪ Synthesis: Reading input text files ▪ Simulation: Reading input text files and writing output text files.
Miscellaneous Topics	▪ Embedding counters and registers inside ASM diagrams. ▪ Using Xilinx primitives: BRAMs, FIFOs, etc.

CLASS POLICIES

- **No Credit Policy**: A grade of 0.0 will be given to students not receiving 60% in the Laboratory category and to students not participating in the Final Project, regardless of their performance in other parts of the course.

- **Laboratory**: Students must be aware of their Laboratory section: 002, 003. This will be used to determine whether a student is late in their laboratory submission. Students are advised to attend on the day of their respective Laboratory Section. However, students can attend any other Laboratory Section if there is space available. Students will be able to complete a TA evaluation form at the end of the semester.

- **Academic conduct policy**: All members of the academic community at Oakland University are expected to practice and uphold standards of academic integrity and honesty. Academic integrity means representing oneself and one's work honestly. Misrepresentation is cheating since it means students are claiming credit for ideas or work not actually theirs and are thereby seeking a grade that is not actually learned. Academic dishonesty will be dealt with seriously and appropriately. Academic dishonesty includes, but it is not limited to cheating on examinations, plagiarizing the works of others, cheating on lab reports, unauthorized collaboration in assignments, hindering the academic work of other students.

- **Special Considerations**: Students with disabilities who may require special consideration should make an appointment with campus Disability Support Services, 106 North Foundation Hall, phone 248 370-3266. Students should also bring their needs to the attention of the instructor as soon as possible. For academic help, such as study and reading skills, contact the Academic Skills/Tutoring Center, 103 North Foundation Hall, phone 248 370-4215.

- **Add/Drops**: The university policy will be explicitly followed. It is the student's responsibility to be aware of deadline dates for dropping courses.

- **Attendance**: It is assumed that the students are aware of and understand the university attendance policy. Attendance is mandatory and maybe monitored. Students are responsible for all material covered in classes that they miss. There will no excuses for being late to quizzes/exams.

- **Athlete Excused Absences**: Students shall inform the instructor of dates they will miss class due to an excused absence prior to the date of that anticipated absence. For activities such as athletic competitions whose schedules are known prior to the start of a term, students must provide their instructors during the first week of each term a written schedule showing days they expect to miss classes. For other university excused absences, students must provide the instructor at the earliest possible the dates that they will miss.

- **Special Circumstances:** The instructor should be notified as early as possible regarding any special conditions or circumstances which may affect a student's performance during the course timeframe (e.g., medical emergencies, family circumstances).

- **Cellphones**: A ringing cellphone going off during a lecture is disruptive to other students as well as the instructor. Students are strongly advised to set their cellphones to vibrate (not ringing) and leave the classroom discretely to answer the phone.