Midterm Exam

(October 21st @ 5:30 pm)
Clarity is very important! Show your procedure!

PROBLEM 1 (20 PTS)

- (5 pts) Complete the following table. The numbers are unsigned integers.

Decimal	BCD (bits)	Binary	Hexadecimal
			B5
59		00111011	
86		01010110	
	0001 0001 0100		72

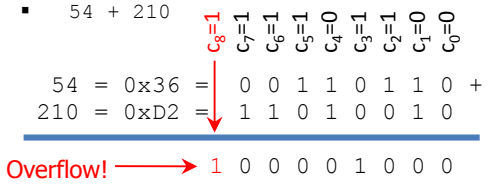
- (5 pts) Complete the following table. The numbers are represented with 8 bits.

	REPRESENTATION	
Decimal	**1's complement**	**2's complement**
		11001110
	10010010	
		01001101
-86		

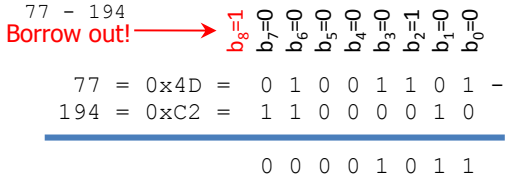
- (5 pts) Perform the following addition and subtraction of 8-bit unsigned integers. Indicate (every carry) or borrow from c_0 to c_8 (or b_0 to b_8). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte.

Example:

- 54 + 210



- 77 - 194



- 86 + 181

- 86 - 181

- (5 pts) Perform the following operations using the <u>2's complement representation</u> with 8 bits. Determine whether the operations result in an overflow.
  - -59 - 114
  - -86 + 114

PROBLEM 2 (10 PTS)

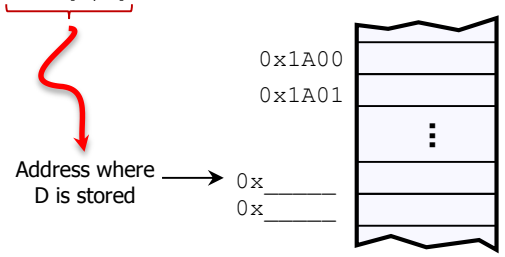
- A microprocessor has a 16-bit address line, where each address contains 8 bits. An SRAM device is connected to the microprocessor. The microprocessor has assigned the addresses `0xD800` to `0xDFFF` to this SRAM to this SRAM.
  - What is the size (in KB, or MB) of this SRAM?
  - What is the minimum number of bits required to represent the addresses only for this SRAM?

PROBLEM 3 (20 PTS)

Given the following set of instructions, complete the following:

- Register values (in hexadecimal format) as the instructions are executed.
- The state of the memory contents (in hexadecimal format) after the last instruction has been executed. Also, specify the memory address at which the contents of `D` are stored (last instruction).
- The addressing mode of each instruction. Be specific, if for example the addressing mode is indexed, indicate which one in particular. Note that the `movw` instruction uses two addressing modes.

Addressing Mode					
Inherent	`clra`				
	`clrb`				
Immediate	`ldx #$FADE`				
	`ldy #$1A00`				
		A $00	**B** $00	**X** $FADE	**Y** $1A00
	`movw #$1E20,1,Y+`				
		A	**B**	**X**	**Y**
	`ldab #$81`				
		A	**B**	**X**	**Y**
	`sex b,d`				
		A	**B**	**X**	**Y**
	`addd 1,-Y`				
		A	**B**	**X**	**Y**
	`exg x,y`				
		A	**B**	**X**	**Y**
	`std [0,X]`				



PROBLEM 4 (10 PTS)

- Mark the correct option:
  - ✓ The Interrupt Vector Table contains the list of: Vector Addresses / Interrupt Vectors
  - ✓ The Software Interrupt (`swi`) is a: Maskable Interrupt / Non-maskable Interrupt

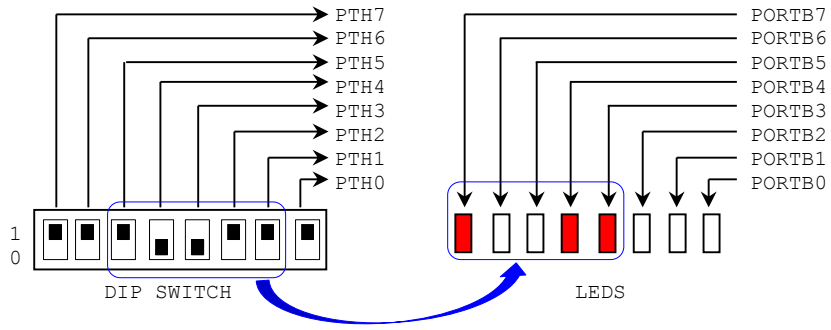
- Determine whether the following statements are True or False. If the statement is false, explain why.
  - ✓ For an Interrupt, the Interrupt Service Routine pushes the values of the PC and CPU registers in the Stack.
  - ✓ An Interrupt Vector is the starting address of an Interrupt Service Routine.
  - ✓ When servicing a Reset, the values of the PC and CPU Registers are pushed in the Stack.

- Complete:
  - ✓ To enable/disable all maskable Interrupts, we configure the bit ____ of CCR.
  - ✓ The `/XIRQ` Interrupt is enabled by setting the bit ___ of CCR to 0.

PROBLEM 5 (20 PTS)

- (5 pts) Complete the Assembly Program below so that the state of bits 5 down to 1 on the DIP Switch are displayed only on the 5 leftmost bits on the LEDs (`PORT B`). The figure shows an example on the Dragon12-Light Board: the number `10011` is shown on the five leftmost LEDs, while the other LEDs are off.

```
ROMStart    EQU  $4000

; code section
            ORG   ROMStart

Entry:
_Startup:
            LDS   #$4000

            movb #$FF, DDRB
            movb #$00, DDRH


showDIPSW:  ldaa PTH

            ; /* Write instructions here */
```




```
            ; /* End of your instructions */
            staa PORTB     ; Contents of register A are written on PORTB
            bra showDIPSW
```

- (5 pts) What is the time delay (in ms) that the following loop generates? Assume a 25 MHz bus clock. Consider that `pusha` takes 2 cycles, `pula` 3 cycles, `nop` one cycle and `dbne` 3 cycles.

```
ldx #56000
loop:  nop
       nop
       psha
       pula
       psha
       pula
       dbne X, loop
```

- (10 pts) After the `addd $10A0` instruction, what is the state of `D` and the following CCR flags: Z, C, V, and N? Does the `bcs next` instruction branches to '`next`'? Yes or no? Why?

```
      movw #$41AC, $10A0
      ldd #$730B
      addd $10A0
      bcs next
      ...
next: ...
```

D [ ]

	S	X	H	I	N	Z	V	C
CCR								

PROBLEM 6 (20 PTS)

- Given the following Assembly code, specify the `SP` and the Stack Contents at the given times (right after the colored instruction has been executed). `SP` and the Stack Contents (empty) are specified for the first instruction (`LDS #$4000`).
- Specify a value in the instruction `adda` that would make the branch instruction `bvs` branch to `myloop`.