ECE 2700 Final Project Presentation

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Design Objective: Simple Unsigned Calculator

Inputs: via keyboard

- Two 8 bit unsigned numbers
- One of four functions (+, -, *, /)

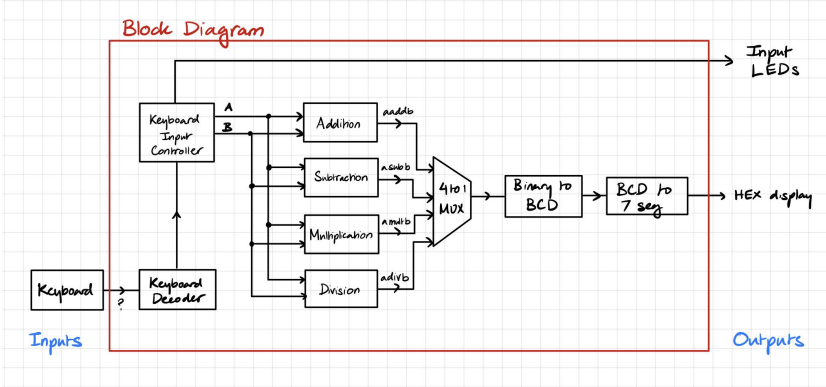
Outputs: NEXYS A7 Board

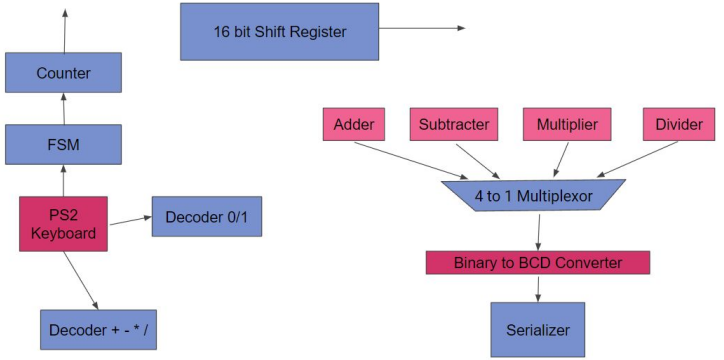
- BCD displayed on seven segment displays
- Function as an RGB LED
- Input values on the LEDs

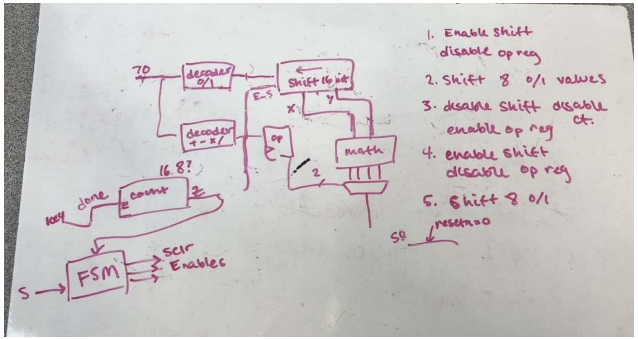
Keyboard

NEXYS A7 Board

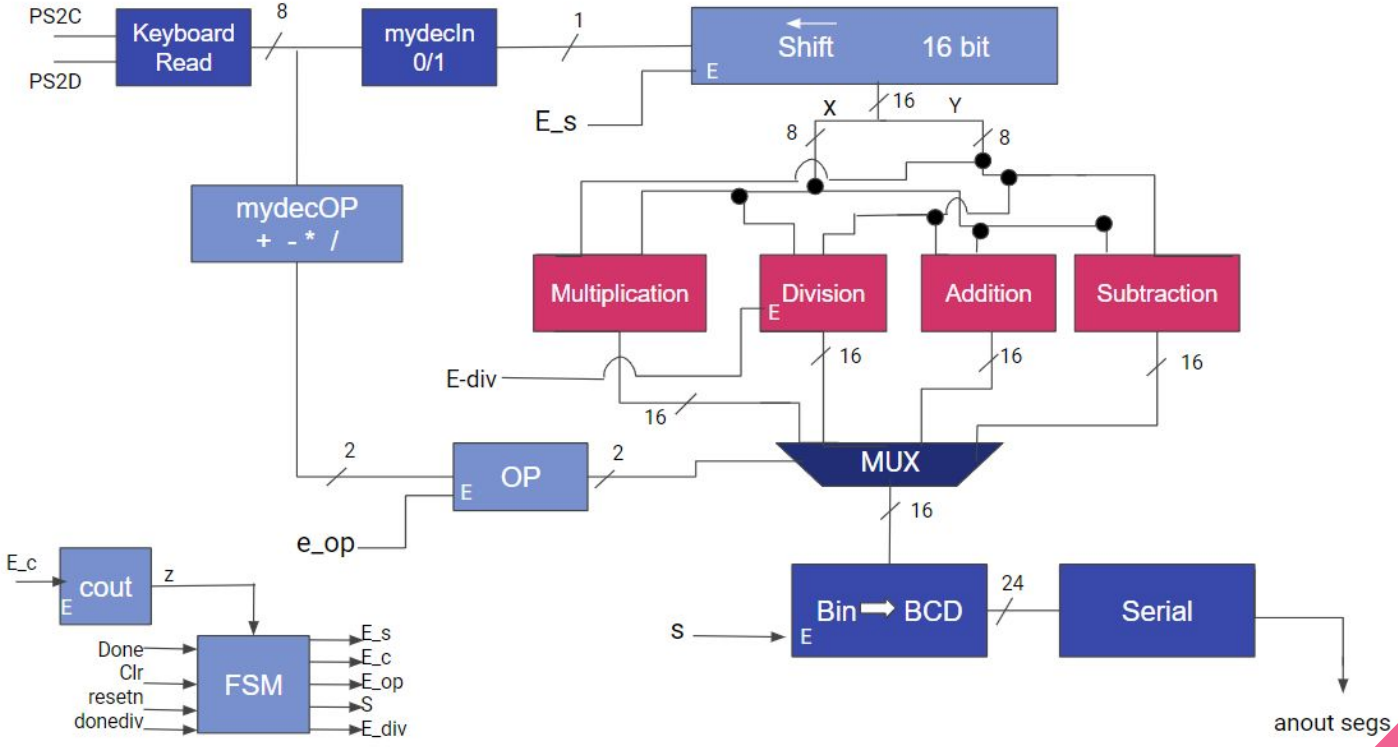
Previous Block Diagrams

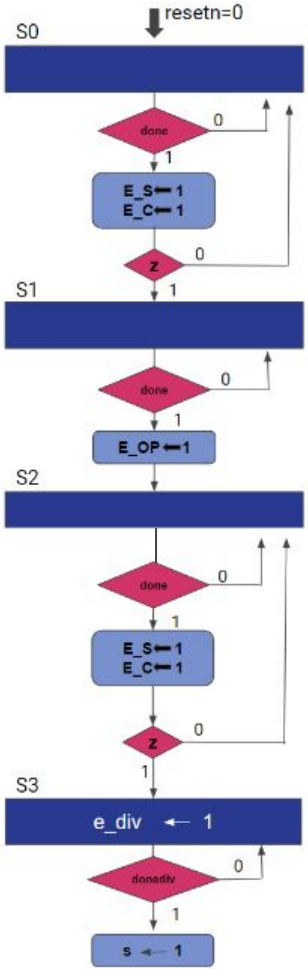






Final Block Diagram





Finite State Machine (FSM)

- Reset button is used to clear registers and restart
- **S0** - Record the first input (8 bits)
- **S1** - Record the operation (2 bits)
- **S2** - Record the second input (8 bits)
- **S3** - Enable the divider, when the divider finishes enable the binary to BCD converter

PS/2 Keyboard Controller, Decoders

Key	Scan Code make (break)
1	69 (F069)
0	70 (F070)
/	E04A (E0F04A)
*	7C (F07C)
-	7B (F07B)
+	79 (F079)

0 / 1

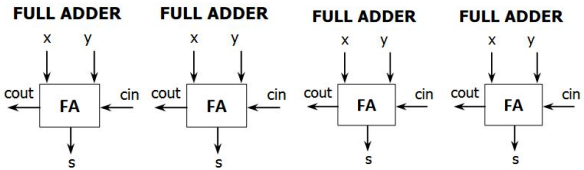
- Receives the 8 bit scan code
- Outputs a 1 bit binary value to be shifted into the 16 bit shift register
- Default input is a ‘1’

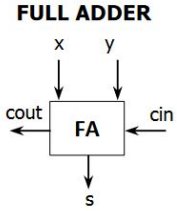
(+ - * /)

- Receives the 8 bit scan code
- Outputs a 2 bit selector for the MUX, stored in a 2 bit register
- Default operator is +

Math Operations Blocks (+ - * /)

Adder/Subtractor



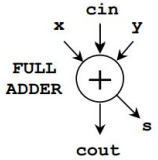


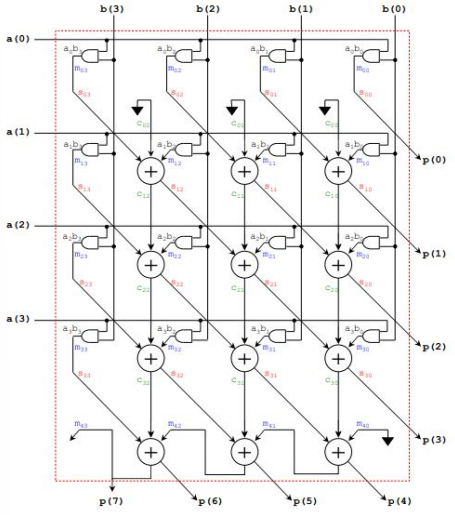
Divider

- Iterative restoring divider
- FSM
- Left Shift register for X input and quotient
- Register for Y input
- Subtractor
- Left Shift register for remainder

Multiplier

- Array Multiplier





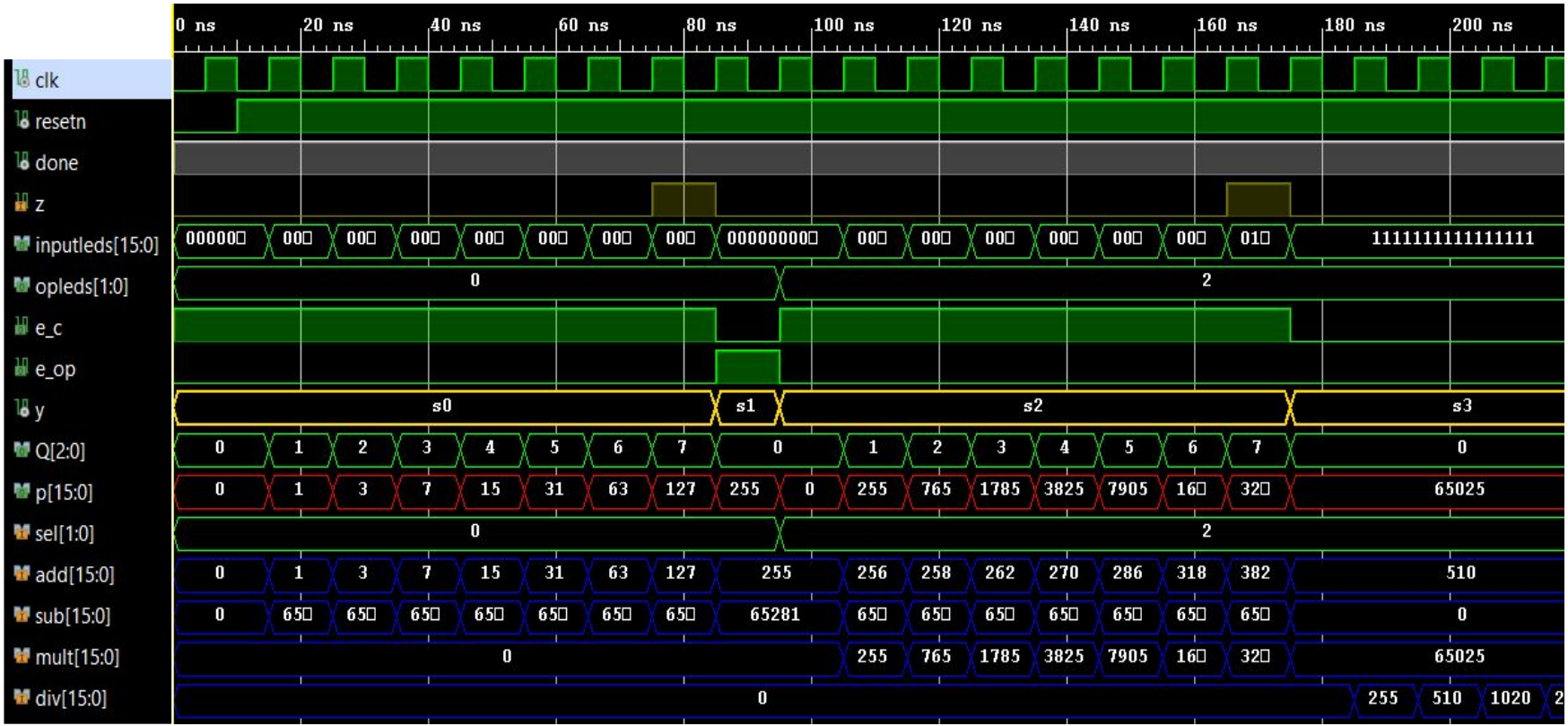
Binary to BCD, 7-Segment Serializer

Binary to BCD: Converts the binary output from the MUX into a BCD value to be displayed on the 7-segment display

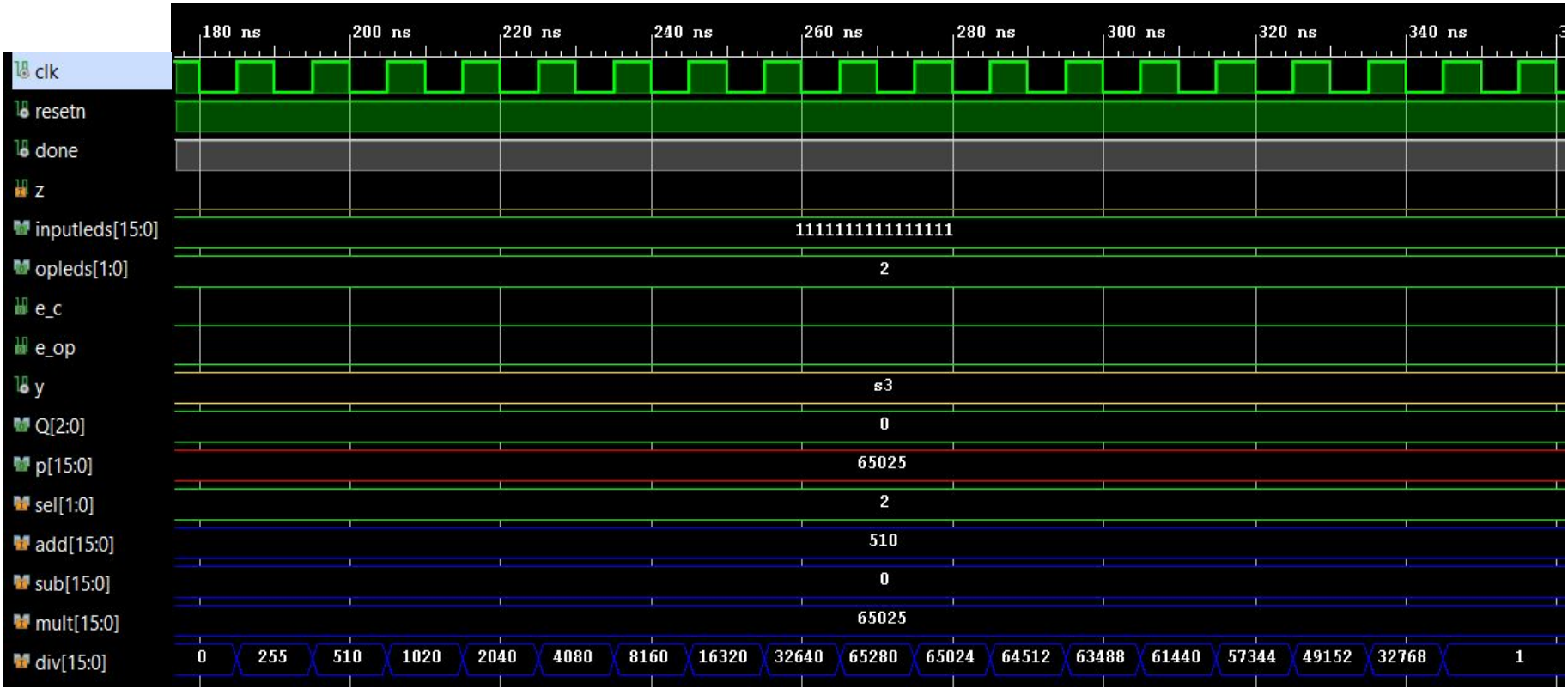
Serializer: Necessary to display several unique values on the seven segment displays

- Multiplexer
- Counter 1ms
- Hex to 7 segment decoder (active low)
- Decoder to AN for each display

Timing Diagram



Timing Diagram



Demo

- $1111\_1111_{(255)} / 1111\_1111_{(255)} = 1$
- $1010\_0000_{(160)} * 1110\_1110_{(238)} = 38080$
- $0011\_1111_{(63)} - 0011\_0000_{(48)} = 15$
- $0101\_0101_{(85)} + 1010\_1010_{(170)} = 255$

Video link: https://youtu.be/Fa8NBjneTu0

Thank you!!!!!!!

References

[1] Llamoca, D. (2013). VHDL coding for fpgas. Retrieved April 12, 2023, from https://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

[2] Master XDC file for Vivado Designs. (n.d.). Retrieved April 12, 2023, from https://moodle.oakland.edu/pluginfile.php/8345475/mod_page/content/6/Nexys-A7-100T-Master.xdc

[3] Divider Implementation. (n.d.). Retrieved April 17, 2023, from https://www.secs.oakland.edu/~llamocca/dig_library/arith/Divider%20Implementation.pdf