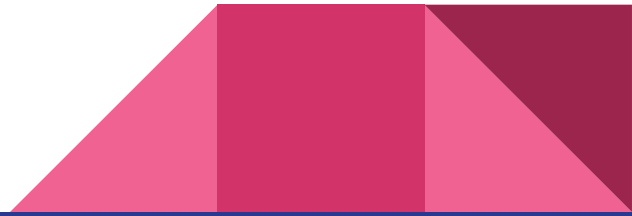
FPGA Sound Synthesizer

Armela Gjokaj | Forrest Mason | Mehvi Mehvi | Tyler Waddell
e-mails: armelagjokaj@oakland.edu, forrestmason@oakland.edu, mehvi@oakland.edu, waddell@oakland.edu

Introduction

The project is about the implementation through VHDL of a Sound Synthesizer. It involves the connection of an external device, which is a buzzer, to the FPGA board through the PMOD ports. The user can use SW[0] to hold the system in its current state.

Notes ascend from C4 to C5, no sharps



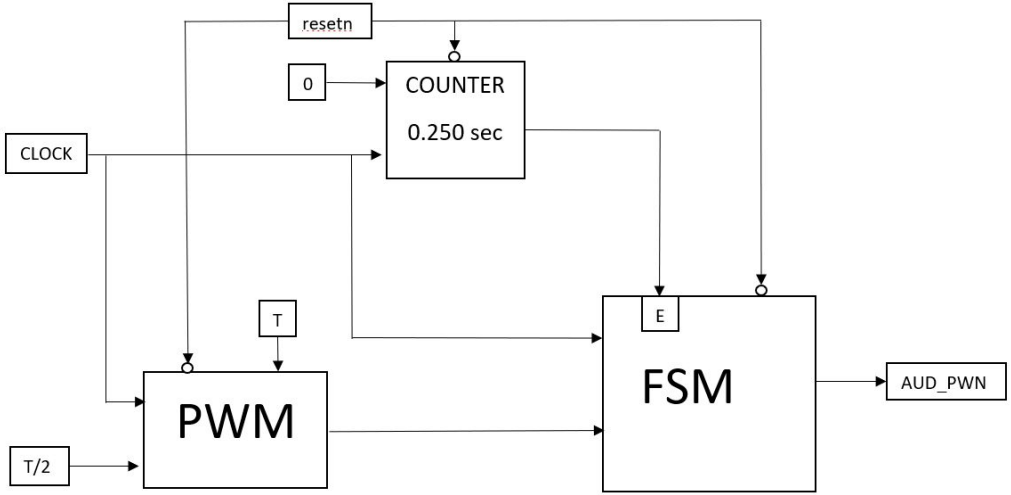
Methodology

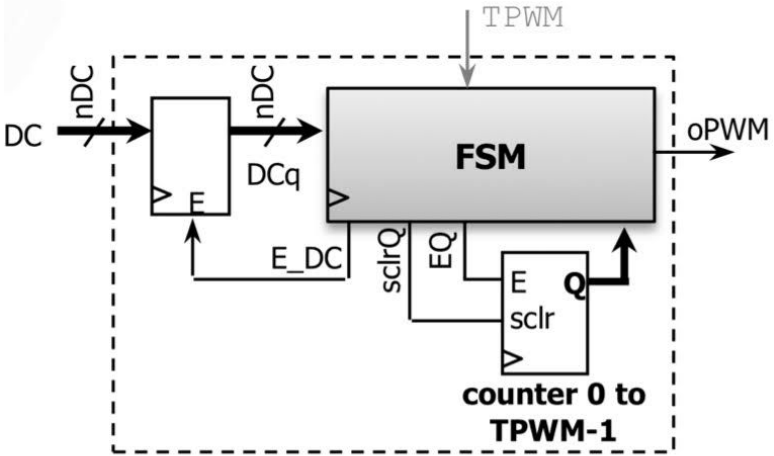
The process of building the circuit consists of two systems which are presented in diagrams. The state diagram describes the desired output based on the user input.

Math determined number constants

Clock Rate	Note	Note Frequency	TPWM Count	DC
100MHz	C	261	383142	191571
	D	293	341297	170648
	E	329	303951	151976
	F	349	286533	143266
	G	392	255102	127551
	A	440	227273	113636
	B	493	202840	101420
	C	523	191205	95602

Block Diagram





$$nDC = \lceil \log_2(TPWM + 1) \rceil$$

$$If\ DC = 0 \rightarrow oPWM = 0$$

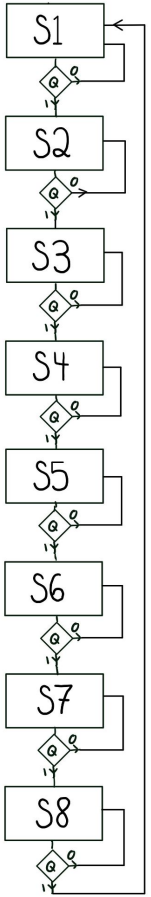
$$If\ DC = TPWM \rightarrow oPWM = 1$$

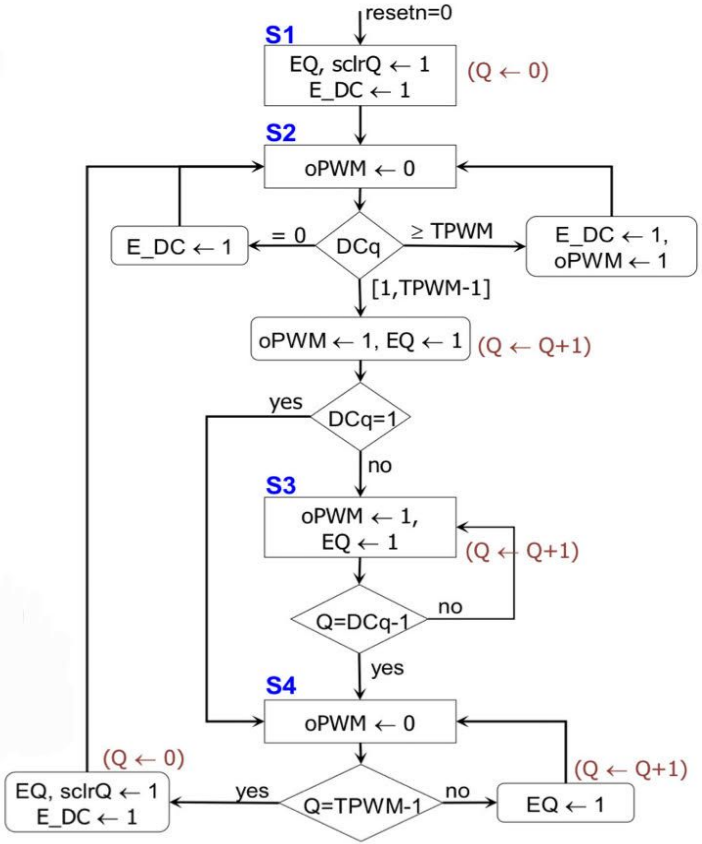
Counter counts to 25,000,000

System State Diagram

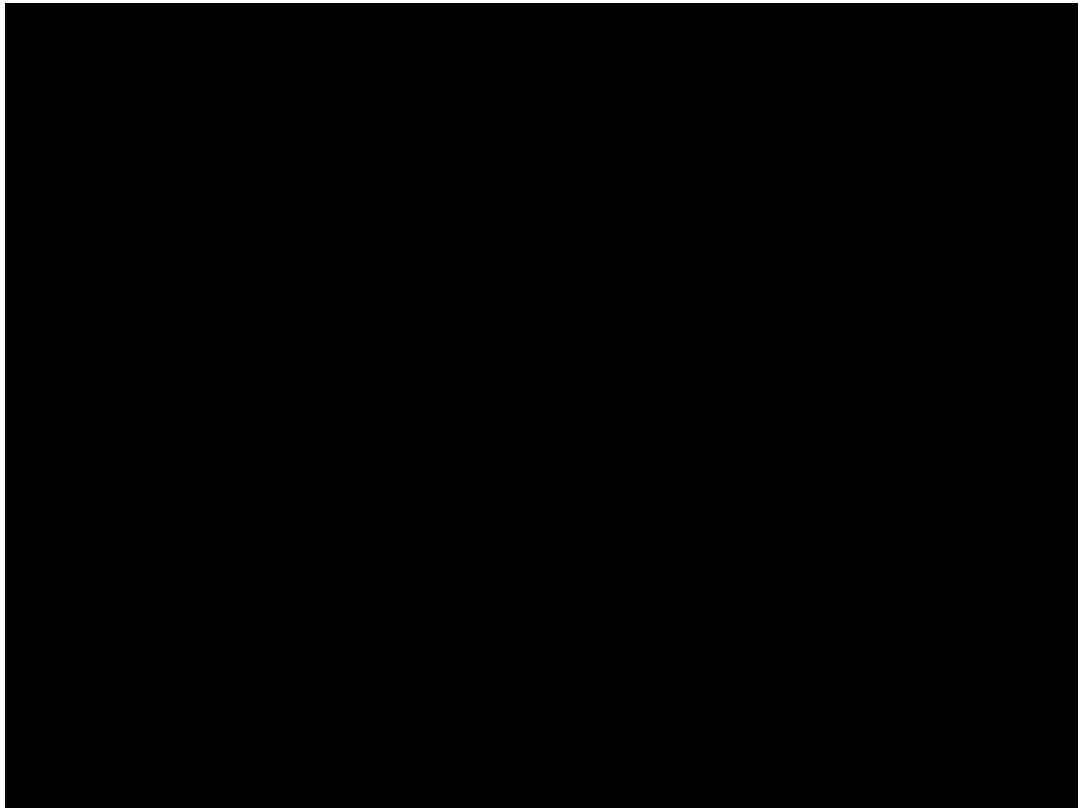
Each non-PWM state (S1-S8) sets the output to a unique frequency

A enable-type input ‘Q’ acts as a hold on the current state and prevents progression





Demo



Future Improvement and Conclusions

States can be expanded to accommodate a larger musical register

Current thought process on implementing measures involves a counter to determine which note is played next/for what duration