Digital Stopwatch

ECE-2700 FINAL PROJECT

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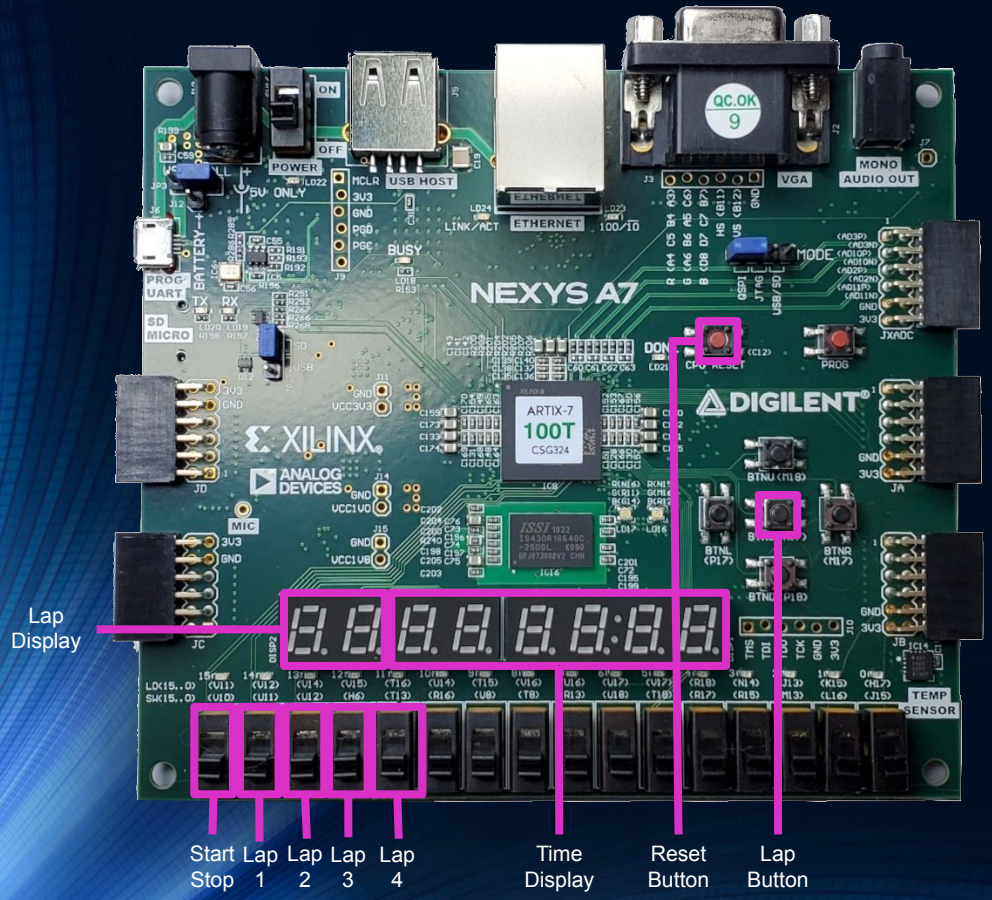
Design Objective

Using the Nexys A7 FPGA Development Board, design and develop a functional digital stopwatch.

- The stopwatch will display different units of time such as:
  i. Minutes
  ii. Seconds
  iii. Deciseconds (tenths of a second)
  iv. Centiseconds (hundredths of a second)

- Stopwatch will have multiple functions such as:
  i. Start
  ii. Lap
  iii. Pause
  iv. Reset

Logic Board Controls

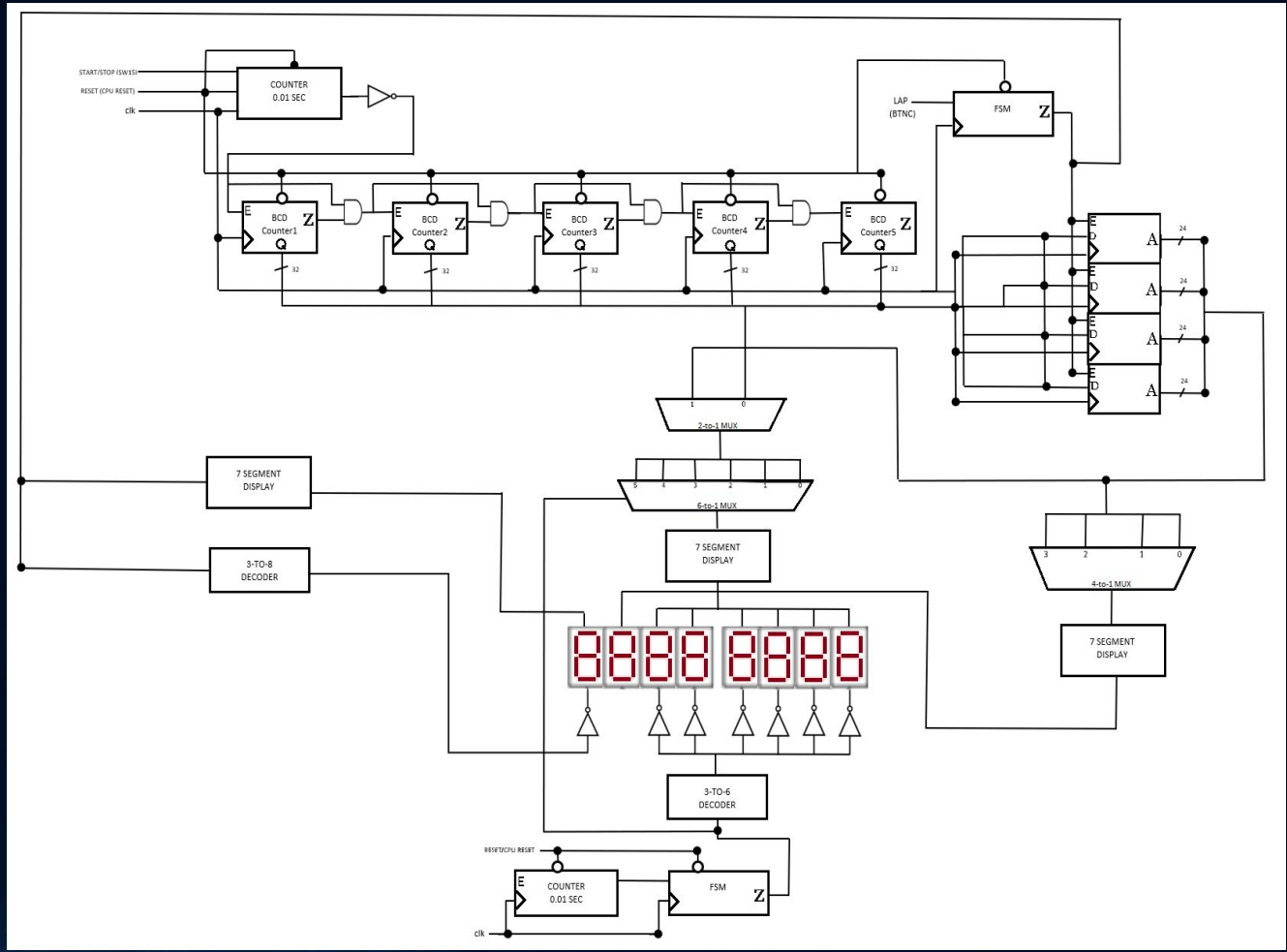


- Center Button BTNC is used to set lap times.
- Switches 14 to 11 are used to toggle between lap times 1-4.
- CPU Reset button is used to reset the stopwatch.
- Switch 15 is used as a start/stop toggle switch for the stopwatch.
- All 7-segment displays will be used and will turn on automatically with the stopwatch.

Digilent Nexys A7-100T

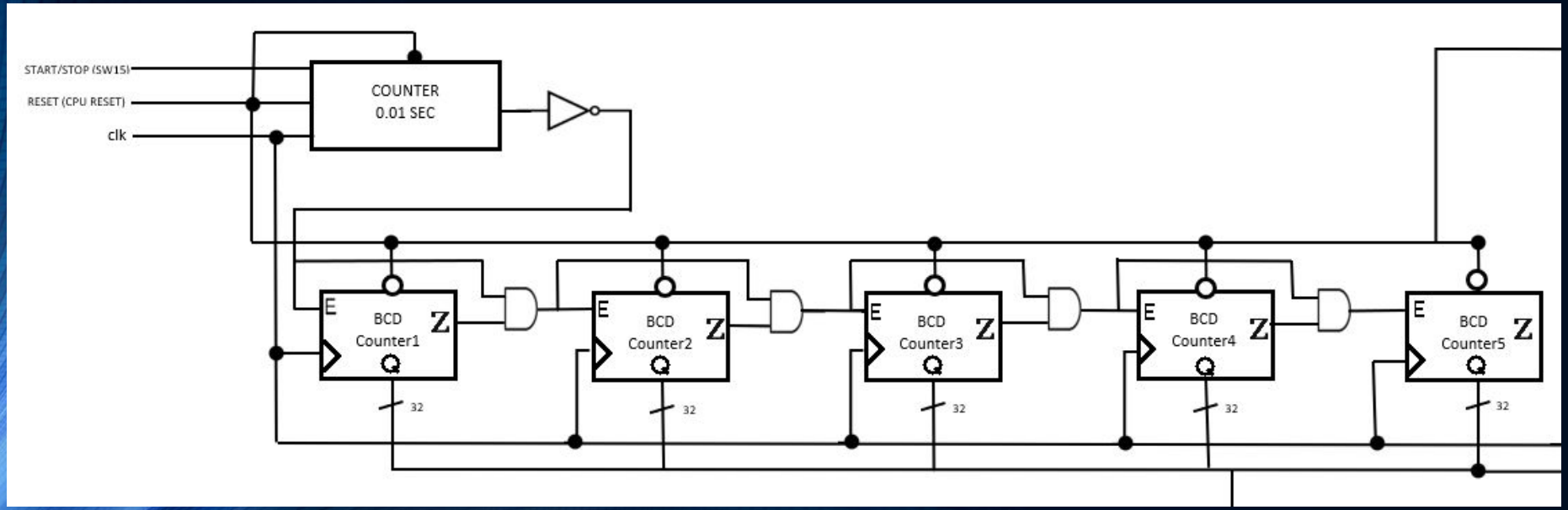
Wiring Diagram

- Design has:
  - i. BCD counters and FSM counters
  - ii. Finite State Machines
  - iii. Multiplexors
  - iv. Seven-Segment Displays
  - v. Encoders
  - vi. Decoders



Counters

- Stopwatch has 6 counters for time unit tick rate and a counter for incrementing tick rate to the hundredth of a second, or centisecond.
- Top counter enables centi second counter for every 10^6ns which then enables the centi second counter and so forth.



7-Segment Displays

Display Information

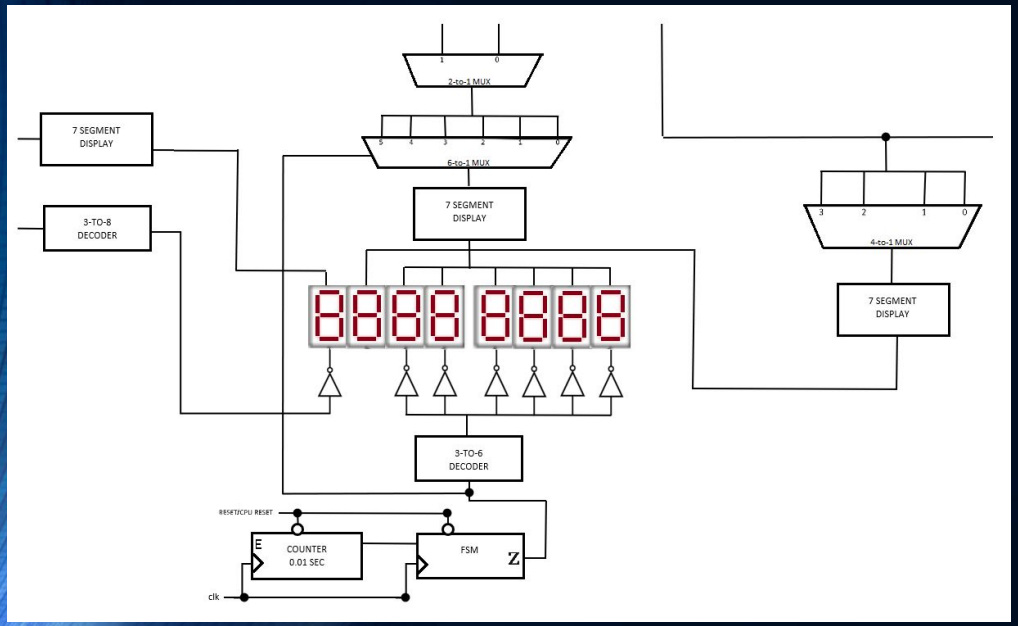
Lap Number

Minutes

Seconds

Centisecond

Decisecond

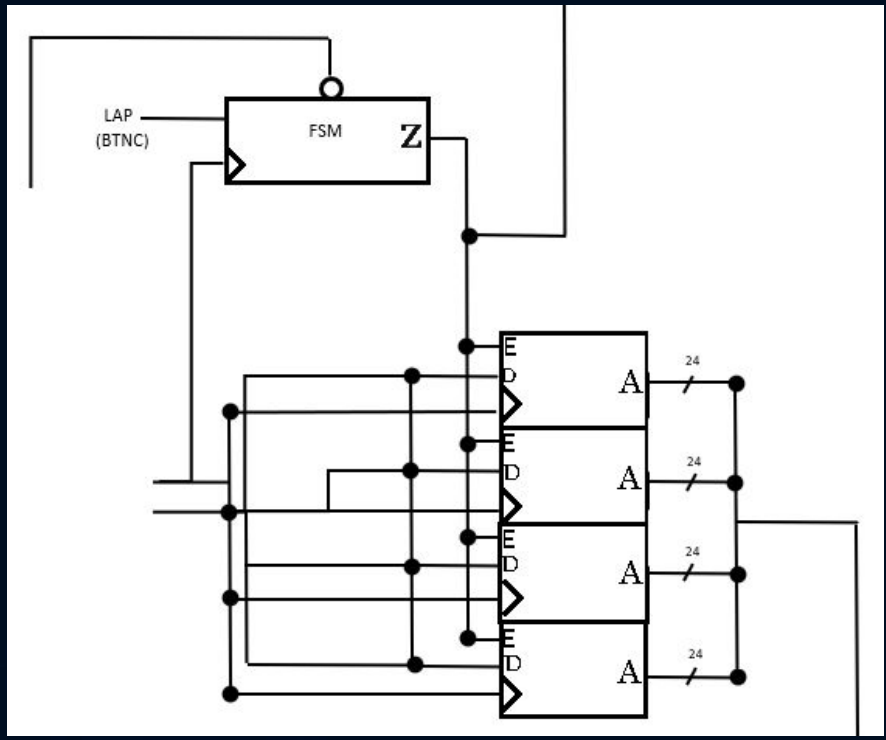


- In the above diagram, all 7-segment displays but the first two are used to display the time. They are combined to work together.
- By using a 2-to-1 Mux, the stopwatch can toggle between showing lap times or watch time.
- Used a 6-to-1 Mux for the 7-segment displays connected to a 7-segment decoder.

Project Extra Feature

Lap Memory

- Created 4 registers for 4 different lap times using a lap encoder with 2 bits to differentiate states of lap.
- Each lap belongs to a switch when toggled to show different lap times.
- Registers are connected to BCD Counters and outputs are 24 bit with shared connection which feed to the 2-to-1 Mux.
- FSM redirects data from the first register to the next register.



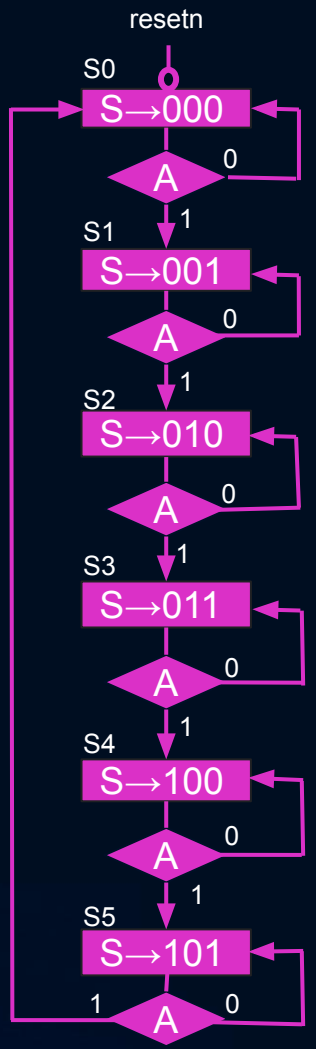
Finite State Machine

- There are 6 different states for the FSM. Each state is connected to a 7-segment display.

  S0: Centisecond Display
  S1: Decisecond Display
  S2: Second Display
  S3: Tens Second Display
  S4: Minute Display
  S5: Tens Minute Display

- Finite State Machine has a counter to tick between different states.

- Max Time Display: 59:59.99



Thank You!

Demonstration Video

https://drive.google.com/file/d/12X9szibKPFOjxEwfYlRO_UEvrL2FZXeN/view?usp=sharing

References

http://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

https://kcmedicine.org/healthminute/stopwatch/#