Course Information

INSTRUCTOR	Daniel Llamocca
CONTACT INFO	email: llamocca@oakland.edu
OFFICE HOURS	Tuesday 2:00 to 4:00 pm (Moodle → Virtual Office hours via Zoom, or by appointment)
LECTURES	Tuesday/Thursday 5:30 pm - 7:17 pm (CRN: 12671 – online). ▪ Synchronous sessions (Zoom) on Thursdays. ▪ Asynchronous sessions (Panopto) on Tuesdays.
TAS	▪ Sandeep Kumar keshwapanthula@oakland.edu ▪ Moath Algharibeh algharibeh@oakland.edu ▪ Ala'aldin Hijaz ahijaz@oakland.edu

LABORATORY

Section	CRN	Time	TAs	
002	12672	Monday 7:30 pm – 10:30 pm @ Room EC-562	Ala'aldin	Moath
003	12673	Monday 12:00 pm -2:59 pm @ Room EC-562	Ala'aldin	Moath
004	12674	Tuesday 12:00 pm -2:59 pm @ Room EC-562	Sandeep	Moath
006	14548	Wednesday 12:00 pm -2:59 pm @ Room EC-562	Sandeep	
007	15699	Monday 4:00 pm – 7:00 pm @ Virtual Section (online)	Sandeep	
008	15752	Wednesday 4:00 pm – 7:00 pm @ Room EC-562	Sandeep	
010	15754	Monday 8:00 am – 11:00 am @ Virtual Section (online)	Sandeep	
011	15775	Friday 12:00 pm – 3:00 pm @ Room EC-562	Sandeep	Moath

COURSE CATALOG DESCRIPTION: ECE 2700 – Digital Logic Design (4 credits)

Boolean algebra; number systems and arithmetic, combinational logic circuits; synchronous sequential circuits; asynchronous sequential circuits; introduction to a hardware description language (HDL). With Laboratory. (Formerly ECE 278).
Prerequisite(s): EGR 240 or EGR 2400.

COURSE MATERIALS

- The course material will be hosted on Moodle (moodle.oakland.edu). Grades will be periodically posted via this system.
- As a backup resource, the material will also be posted at: www.secs.oakland.edu/~llamocca/Winter2021_ece2700.html
- VHDL for FPGAs Tutorial: Available at the following permanent link: www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

TEXTBOOK

- A textbook is not required. Class notes will be provided for every unit. Students are encouraged to use the extra references.

EXTRA REFERENCES:

- Bryan J. Mealy, James T. Mealy, *Digital McLogic Design*, Free Range Factory, 2012 (free download).
- Bryan Mealy, Fabrizio Tappero, Free Range VHDL, Free Range Factory, 2013 (free download).
- S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, 3rd ed., McGraw Hill, 2009. (suggested)
- Peter J. Ashenden, The Student's Guide to VHDL, 2nd ed., Elsevier, 2008.

COURSE OBJECTIVES

1. Design and analyze combinational and sequential logic circuits. (1)
2. Design and analyze finite state machines. (1)
3. Perform addition, subtraction, and multiplication in binary arithmetic. (1)
4. Describe memory operation and memory addressing. (1)
5. Describe digital circuits using VHDL and implement them on an FPGA. (1, 6)
6. Perform functional and timing simulation of a digital circuit described in VHDL. (1,6)
7. Describe how combinational and sequential components can be used to design a datapath and control unit for implementing digital systems. (1, 2)
8. Work in a team environment to design a digital system and communicate the results in a written report and an oral presentation. (1, 2, 3, 6)

ABET Course Outcomes:

1	2	3	4	5	6	7

GRADING SCHEME:

Homeworks:	15%	**Final Project:**	15%
Quizzes:	10%	**Midterm Exam**:	20% (February 16th, 5:30-7:17 pm)
Laboratory:	20%	**Final Exam**:	20% (April 27th, 7:00 – 10:00 pm)

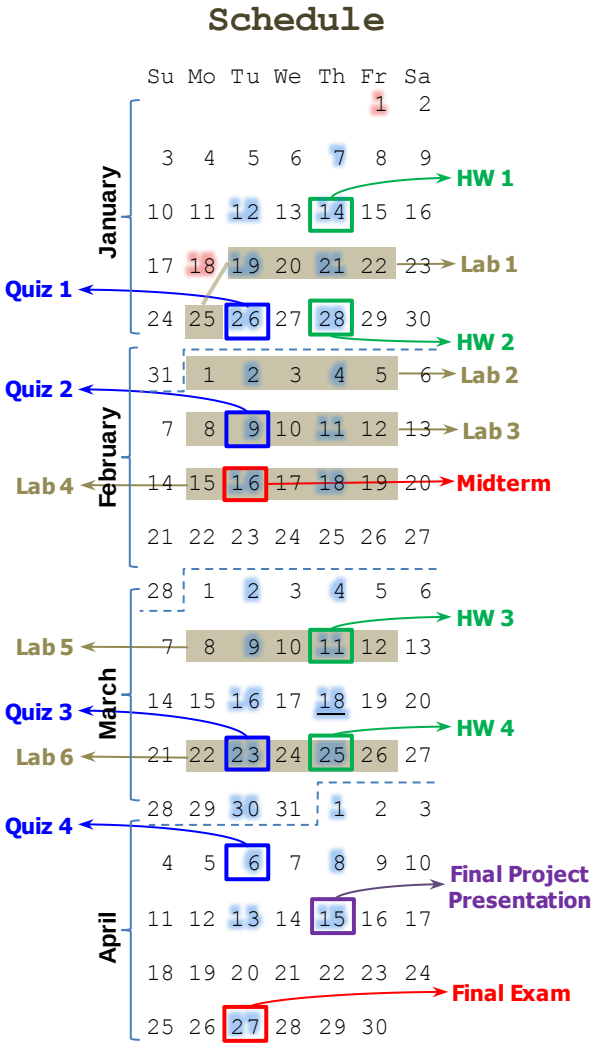
- **Homeworks:** Homework assignments are meant to strengthen your conceptual understanding of the topics. Completing homework assignments is a key component of this course as it will help students master the course material and prepare them for the exams.
  Homeworks will be posted according to the schedule (green rectangles). Students have one week to turn in the completed assignments (via Moodle). Late submissions are NOT accepted.

- **Quizzes:** They will have a duration of 45 minutes at the beginning of class.

- **Exams:** Closed-books, closed-notes, online exams. The final exam will be a comprehensive test that will cover the whole syllabus. Students are not allowed to take the exams neither before nor after the exam date. Make-up exams are given *only* under extreme circumstances (e.g.: medical emergency, jury duty).

- **Laboratory:** This important component of the class will reinforce your understanding of the topics. There will be six (6) labs throughout the semester.
  TAs will be present every week during the regularly scheduled laboratory times. Students can work during those times or at any other time and place.
  Depending on the lab assignment, students have 1 or 2 weeks to complete them and have them checked off by the TA.
  * *There is a late policy on laboratory assignments.*

- **Final Project:** Students will work in groups (up to 4) in a Final Project. Each group will prepare an oral presentation and submit a final report. Presentations will take place on April 15th.



GRADE ASSIGNMENT:

96-100	A	4.0
90-95	A-	3.7
85-89	B+	3.3
80-84	B	3.0
72-79	B-	2.7
66-71	C+	2.3
60-65	C	2.0
56-59	C-	1.7
53-55	D+	1.3
50-52	D	1.0
49 and below	F	0.0

LABORATORY MATERIALS

- **Hardware**: Nexys™ A7 FPGA Trainer Board - Option: A7-50T (you can also use the Nexys™-4 DDR Artix-7 FPGA Board)
  - ✓ To order: https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
    Go to: Get Academic Pricing ($171.75)

  If you do not plan to take ECE4710, you can use the Basys3 Trainer Board:
  - ✓ To order: https://store.digilentinc.com/basys-3-artix-7-fpga-trainer-board-recommended-for-introductory-users/
    Go to: Get Academic Pricing ($111.75)

- **Software**: Vivado HL Webpack Edition (free software)
  - ✓ To download: http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

OUTLINE OF TOPICS

Introduction to Logic Circuits	▪ Boolean Algebra ▪ Sum-of-Products and Product-of-Sums forms ▪ Logic Gates. Timing diagrams	
Optimized Implementation of Logic Functions	▪ Basic Techniques ▪ Karnaugh Maps ▪ Quine-McCluskey algorithm	
Implementation Technology	▪ Logic Levels, CMOS Logic gates ▪ Tri-state buffers, Transmission Gates ▪ Practical aspects: propagation delay, noise margin, hazards ▪ Programmable Logic Devices, Field Programmable Gate Arrays	
Number Systems and Computer Arithmetic	Unsigned integer numbers	Binary representation Octal and hexadecimal representation Addition and subtraction
	Signed integer numbers	Binary representation Addition and subtraction
	Multiplication of integer numbers	Array multiplier for unsigned numbers Multiplication of signed numbers
	▪ Binary Codes ▪ Introduction to Fixed-point arithmetic	
Combinational Circuits	Basic circuits	Multiplexers, De-multiplexers, Shannon Expansion Theorem Decoders, Encoders, Comparators Code Converters: BCD to 7-segment, Gray to BCD, etc. Parity generators and parity checkers
	Complex circuits	Look-up Tables Arithmetic Logic Unit (ALU) Design Barrel shifter
Synchronous Sequential Circuits	Basic circuits	Flip flops and latches Registers, shift registers Parallel access shift registers: parallel-to-serial/serial-to-parallel conversion Counters: synchronous, BCD, Ring, Johnson Random Access Memory
	Finite State Machines (FSMs)	Moore and Mealy state Models Design Steps: State Diagram, State Table, State assignments. Algorithmic State Machine (ASM) charts
Introduction to Digital System Design	▪ Digital system (or special-purpose processor) components: Datapath circuit, Control Circuit ▪ Design examples: Small processor, shift-and-add multiplier, sequential divider.	

VHDL: FOR EVERY TOPIC, AN ASPECT OF VHDL DESCRIPTION WILL BE EXPLORED.

Introduction	▪ Design Flow: Design Entry, Functional Simulation, Mapping, Timing Simulation, Implementation ▪ Data Types ▪ VHDL Description: Logic Gates ▪ VHDL Testbench Generation
Concurrent Description	▪ Concurrent statements: 'with-select', 'when-else' ▪ Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux.
Behavioral Description	▪ Asynchronous processes ▪ Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux. ▪ Sequential statements: 'if-else', 'case', 'for-loop'
Structural Description	▪ Hierarchical design: Use of port-map, for-generate, if-generate. ▪ Examples: Adder, multiplier, Arithmetic Logic Unit, Look-up Table
Sequential Circuits	▪ Testbench: generating clock stimulus ▪ Asynchronous processes: Latches ▪ Synchronous processes: flip-flops, counters, registers ▪ Description of Finite State Machines
Parameterization	▪ Simple techniques ▪ Use of for-generate, if-generate.

OUTLINE OF COURSE TOPICS, ASSOCIATED ASSIGNMENTS AND REFERENCE MATERIAL.

TOPICS SHADED IN GRAY: SYNCHRONOUS LECTURES (ZOOM)

TOPICS SHADED IN RED: ASYNCHRONOUS LECTURES (PANOPTO)

Week		Unit	Topics	Associated Material	Assignments
1	01/07	1	Class policies. Class structure	Syllabus	
			Boolean Algebra	Lecture Notes – Unit 1	
2	01/12	1	Canonical Forms, Logic Gates, Timing Diagram	Lecture Notes – Unit 2 VHDL for FPGAs Tutorial # 1	
		1	*VHDL*: logic gates, testbench generation. *Experiment*: First VHDL example		
	01/14	2	K-maps: 2, 3, 4 variables. "Don't care" outputs. Quine McCluskey algorithm. *VHDL*: Use of std_logic_vector	Lecture Notes – Unit 2 VHDL for FPGAs Tutorial # 1	Homework 1
3	01/19	2	*VHDL*: structural description. *Experiment*: 4-bit adder	Lecture Notes – Unit 2 VHDL for FPGAs Tutorial # 4	*Laboratory 1*
	01/21	3	Logic Levels, CMOS Logic gates. Tri-state buffers Propagation delay, hazards Programmable Logic Devices, Field Programmable Gate Arrays	Lecture Notes – Unit 3	
4	01/26	4	Binary representations Unsigned integer numbers. Addition and subtraction *Experiment*: 4-bit subtractor	Lecture Notes – Unit 4 VHDL for FPGAs Tutorial # 4	Quiz 1
	01/28	4	Signed (SM, 1C, 2C) integer numbers. Addition and subtraction Multiplication of integer numbers. Binary codes Introduction to Fixed-Point Arithmetic	Lecture Notes – Unit 4	Homework 2
5	02/02	4	Design Examples	Lecture Notes – Unit 4	*Laboratory 2*
		5	Multiplexor, Demultiplexor, Decoder, Encoder, LUT	Lecture Notes – Unit 5	
	02/04	5	Examples: Timing diagrams, 3-variable function with 4-to-1 MUX *VHDL*: Concurrent description: with-select, when-else *Experiment*: 4-to-16 decoder out of five 2-to-4 decoders	Lecture Notes – Unit 5 VHDL for FPGAs Tutorial # 2	
6	02/09	5	Shannon's Expansion *VHDL*: Asynchronous processes	Lecture Notes – Unit 5 VHDL for FPGAs Tutorial # 3	*Laboratory 3* Quiz 2
	02/11	5	ALU, Barrel Shifter. Midterm preparation	Lecture Notes – Unit 5	
7	02/16		Midterm Exam		*Laboratory 4*
	02/18	6	Latches and flip flops. Timing Diagrams. Examples. *VHDL*: flip flop description	Lecture Notes – Unit 6	
9	03/02	6	Registers, shift-registers, counters. Timing diagrams. Examples	Lecture Notes – Unit 6	
		6	*VHDL*: description of registers, counters	VHDL for FPGAs Tutorial # 5	
	03/04	6	Counter: accumulator-based design. RAM. Examples *Experiment*: 2-bit counter implementation.	VHDL for FPGAs Tutorial # 5	
10	03/09	6	Finite State Machines. Moore and Mealy FSMs. Timing Diagrams. Circuits: Sequence Detectors, Pulse Detector	Lecture Notes – Unit 6	*Laboratory 5*
	03/11	6	*VHDL*: FSM description. *Experiment*: Sequence detector implementation Algorithmic State Machine (ASM) Charts). Exercises. *Experiment*: Sequence detector implementation (ASM)	Lecture Notes – Unit 6 VHDL for FPGAs Tutorial # 6	Homework 3
11	03/16	6	Exercises with ASM charts. *Experiment*: Arbiter implementation (ASM)	Lecture Notes – Unit 6	
		7	Digital Systems: Overview. RGB LED Control. *Experiment*: RGB LED Control	Lecture Notes – Unit 7 VHDL for FPGAs Tutorial #7	
	03/18	7	Digital Systems: VHDL implementation, standard blocks, Timing Diagram.	Lecture Notes – Unit 7	
12	03/23	7	7-segment serializer. UART, PS2 Keyboard, Stopwatch. Example: Special counter: Timing Diagram.	Lecture Notes – Unit 7 VHDL for FPGAs Tutorial # 7	*Laboratory 6* Quiz 3
	03/25	7	*Experiment*: 7-segment serializer implementation. Exercises. Intro to uP.	VHDL for FPGAs Tutorial # 7	Homework 4
13	03/30	7	Timing Diagrams: Bit-counting circuit	Lecture Notes – Unit 7	
		7	*Experiment*: Bit-counting circuit implementation		
	04/01	7	*Experiment*: Special counter implementation	Lecture Notes – Unit 7	
14	04/06	7	Timing Diagrams: Sequential multiplier	Lecture Notes – Unit 7	Quiz 4
		7	*Experiment*: Sequential multiplier implementation	Lecture Notes – Unit 7	
	04/08	7	Final Exam Preparation	Lecture Notes – Unit 6 - Unit 7	
15	04/13	7	Simple Microprocessor	Lecture Notes – Unit 6 – Unit 7	
	04/15		Final Project – Presentation		
16	04/27		Final Exam		

TECHNICAL ASSISTANCE

- If you have general questions about the course (such as due dates, content, etc.) or trouble accessing any of the content in this course, please contact the instructor.
- For Moodle technical issues that you cannot resolve on your own, please contact the e-LIS (e-Learning and Instructional Support) office:
  - ✓ e-LIS Helpdesk Phone: (248) 805-1625
  - ✓ Submit a Moodle help ticket

REQUIRED TECHNOLOGY AND BACKUP PLAN

- To fully participate in this class, you will need an internet connected computer with the most updated version of your favorite web browser installed.
  - ✓ In the event that your computer crashes or internet goes down, it is essential to have a "backup plan" in place where you are able to log in using a different computer or travel another location that has working internet.
  - ✓ Students can access the SECS lab software (including Vivado) via Remote Desktop service. For assistance, contact the SECS technology office.
    - This can be helpful for code design, syntax checking, and simulation. However, for hardware verification, students need to physically connect the FPGA Board to the computer and test the circuit on the board (this step cannot be done remotely).
- Your computer should be able to run the Vivado software. Go here for a description of operating system support.
- If you plan to present your lab work remotely, you need to have a camera than can stream video via Zoom or Google Video.
- Any files you intend to use for your course should be saved to a cloud solution (Google Drive, Dropbox, etc.) and not to a local hard drive, USB stick or external disk. Saving files this way guarantees your files are not dependent on computer hardware that can fail.
- Quizzes, homeworks, and exams are posted as pdf files, and students need to post their work as pdfs. In order to do this, students need to be proficient in editing pdfs or generating pdfs out of scanned pages or pictures.

CLASS POLICIES

- **The instructor is expected to**:
  - ✓ Grade assignments within a week (or two when it comes to homeworks) of the assignment deadline.
  - ✓ The instructor will login into the course every day, at least 5 days a week.
  - ✓ Respond to emails and to Q&A forums replies within 1-2 days.

- **Students are expected to**:
  - ✓ Ensure that their computer is compatible with Moodle.
  - ✓ Follow the calendar of events and complete all assignments by their deadline. Students are responsible for ensuring the timely and correct submission of their assignments (should an issue arise with Moodle, students can email the assignment to the instructor as a last resort by the deadline).
  - ✓ Respond to emails within 2 days
  - ✓ Participate in a thoughtful manner
  - ✓ Respect rules of etiquette
    - Respect your peers and their privacy
    - Use constructive criticism
    - Refrain from engaging in inflammatory comments.

- **E-mail communication**: The instructor will only respond to emails from students that use their Oakland.edu account. Answering student emails from an email other than an Oakland.edu email is in violation of FERPA because the identity of the sender or receiver cannot be verified.

- **Course Questions & Answer Forum**: Students are encouraged to use this forum to post questions (associated with the course content) that they deem of interest to their classmates. The instructor will intervene periodically.

- **Laboratory**: Students must be aware of their Laboratory section (e.g.: 002, 003, 004, 005, …). This will be used to determine whether a student is late in their laboratory submission. Students are advised to attend on the day of their respective Laboratory Section. However, students can attend any other Laboratory Section if there is space available. Students will be able to complete a TA evaluation form at the end of the semester.
  - ✓ For every laboratory, students must demo their work to the TA. Then, they must submit their work files to Moodle. Work files submitted without demoing will not be considered.
    - The TA will sign off the lab sheet. Students must also submit the signed lab sheet to Moodle.
  - ✓ Note that the laboratory work is individual, and students are not allowed to submit their work in groups.

- **COVID-19 guidelines:** OU has instituted a mandatory mask policy on campus. Face shields alone will not serve to meet the mandatory mask policy. If a student comes to the laboratory without a mask, the TA will ask the student to put a mask or leave the laboratory. Students can only join the laboratory when they are cleared with the appropriate green banner display on the Daily Screening Form. For more info, see here. The TAs will also enforce the 10-student cap per lab section. OU takes these guidelines very seriously. Any non-compliance incident will be immediately referred to the Dean of Students' Office. The TA may cancel the laboratory session for the day.

- **Academic conduct policy**: All members of the academic community at Oakland University are expected to practice and uphold standards of academic integrity and honesty. Academic integrity means representing oneself and one's work honestly. Misrepresentation is cheating since it means students are claiming credit for ideas or work not actually theirs and are thereby seeking a grade that is not actually learned. Academic dishonesty will be dealt with seriously and appropriately. Academic dishonesty includes, but it is not limited to cheating on examinations, plagiarizing the works of others, cheating on lab reports, unauthorized collaboration in assignments, hindering the academic work of other students.

- **Special Considerations**: Students with disabilities who may require special consideration should make an appointment with campus Disability Support Services, 106 North Foundation Hall, phone 248 370-3266. Students should also bring their needs to the attention of the instructor as soon as possible. For academic help, such as study and reading skills, contact the Academic Skills/Tutoring Center, 103 North Foundation Hall, phone 248 370-4215.

- **Add/Drops**: The university policy will be explicitly followed. It is the student's responsibility to be aware of deadline dates for dropping courses.

- **Attendance**: It is assumed that the students are aware of and understand the university attendance policy. Attendance is mandatory and maybe monitored. Students are responsible for all material covered in classes that they miss. There will be no excuses for being late to quizzes/exams.

- **Athlete Excused Absences**: Students shall inform the instructor of dates they will miss class due to an excused absence prior to the date of that anticipated absence. For activities such as athletic competitions whose schedules are known prior to the start of a term, students must provide their instructors during the first week of each term a written schedule showing days they expect to miss classes. For other university excused absences, students must provide the instructor at the earliest possible the dates that they will miss.

- **Special Circumstances:** The instructor should be notified as early as possible regarding any special conditions or circumstances which may affect a student's performance during the course timeframe (e.g., medical emergencies, family circumstances).

- **Mental Health Resources**: Oakland University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of support, services are available. For help, contact the OU Counseling Center in the Human Health Building at (248) 370-3465 or the SEHS Counseling Center at 250A Pawley Hall, (248) 370-2633, https://oakland.edu/counseling/sehs-cc/. Student resources can also be found at https://www.oakland.edu/deanofstudents/student-health-safety-resources/. For immediate 24/7 services contact Common Ground at https://commongroundhelps.org/#/ via chat or call or text the word "hello" to 1-800-231-1127.

- **Cellphones**: A ringing cellphone going off during a lecture is disruptive to other students as well as the instructor. ~~Students are strongly advised to set their cellphones to vibrate (not ringing) and leave the classroom discretely to answer the phone.~~