7-Segment Banner

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Motivation

- Implement a design that will allow users to adjust switches to display different scrolling messages on 7-segment displays and select the speed at which they are scrolled
- Deepen our understanding of finite state machines
- Implement a functional digital system using an FPGA

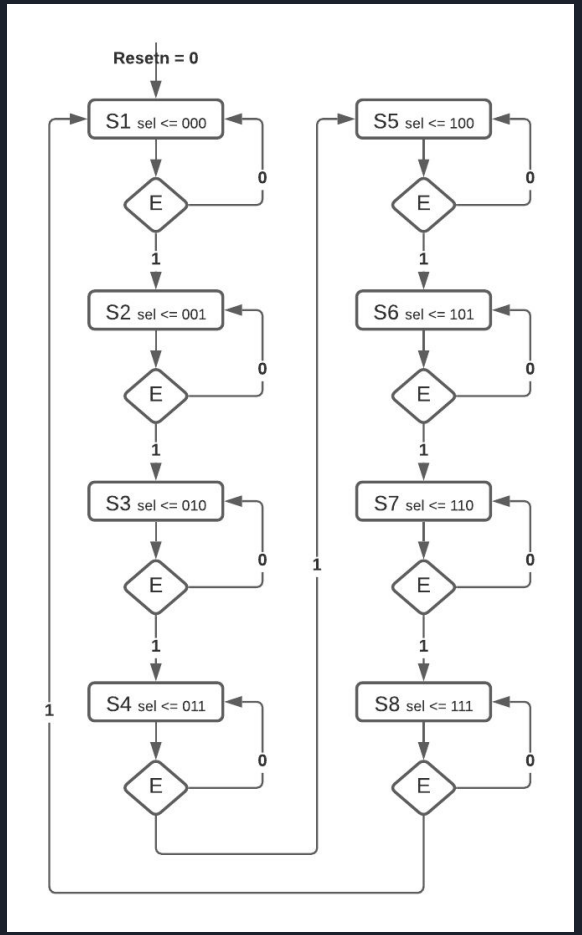
Components

- 2-to-1 MUX
- Parallel Shift Register
- 8-to-1 MUX
- Counter
- FSM
- 3-to-8 Decoder
- Hex to 7-seg Decoder

Finite State Machine

The FSM is used to control the selector for the 8-to-1 mux and is also the input for the 3-to-8 decoder

As the counter outputs a ‘1’ the state machine moves to a new state and its output changes



Counters

Two modulo-N counters are used to control the scrolling speed of the shift register. These two counters are the inputs for a 2-to-1 mux that outputs to the enable for the shift register. This allows the user to choose the scrolling speed through the select on the mux.

Another modulo-N counter is used similarly as the enable input for the finite state machine, which in turn controls which 7-seg display is on and which output is displayed. This is done so that the counter can ensure that the display is given enough time to light up and appear bright to the user before moving on to the next 7-seg display.

Shift Register

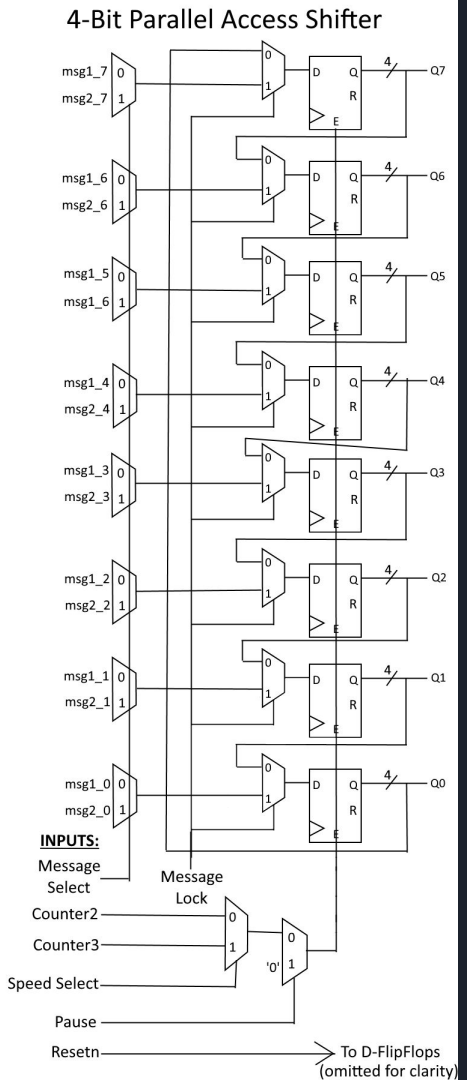
The shift register is used to shift the letters so it seems that they are scrolling across the 7 segment display.

This component is made up of d-flipflops and 2-to-1 muxes.

The 2-to-1 muxes are used to control the input to the d-flipflops in order to select between the messages to display or to allow scrolling.

They also control the input to the enable of the d-flipflops which allows for control of scroll speed as well as the ability to pause scrolling.

The eight outputs of the shift register are passed on to the 8-to-1 mux.

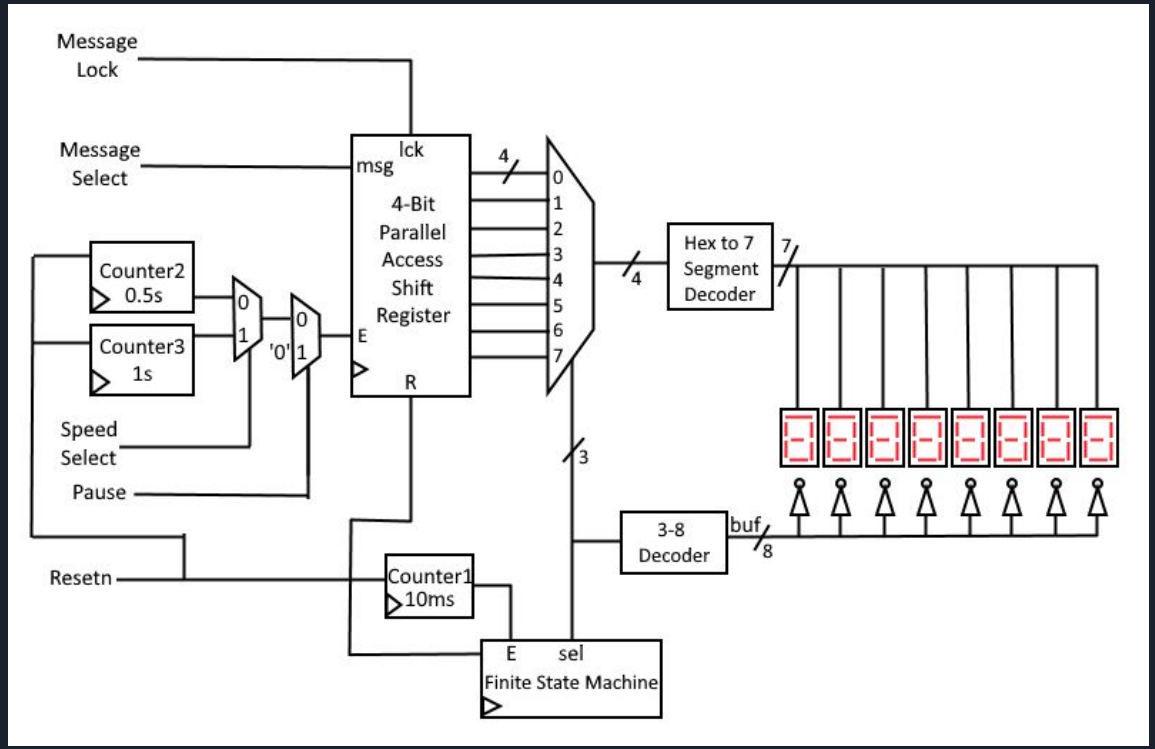


Decoders

The Hex to 7-segment display receives the output from the 8-to-1 mux and converts the 4 bit input into a 8 bit output that displays the correct pattern on the 7 segment display.

While the 3-to-8 decoder is used to choose what displays are on. The finite state machine and counter is used to control the 3-to-8 decoder and ensure that the right display is on at the right time.

Block Diagram



Challenges

- Getting correct timing so the numbers/letters don’t overlap on the seven segment displays
- Debugging the circuit, in specific our original FSM would assign the sel value when E = ‘1’ but instead it needed to assign the value once it reached a new state

Conclusion

In conclusion, using the components that we learned throughout the semester helped us build a circuit that is able to display one of two messages scrolling across a 7 segment display at varying speeds. Through this project we were also able to learn more about the use of finite state machines. This project lends credence to the fact that FPGAs and VHDL are powerful tools to create, test, and execute digital systems.

References

- *VHDL Coding for FPGAs*. [Online]. Available: http://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html. [Accessed: 14-Apr-2021].
- Counter modulo-N (generic pulse generator) with enable and synchronous clear http://www.secs.oakland.edu/~llamocca/Tutorials/VHDLFPGA/Vivado/Unit_5/my_genpulse_sclr.vhd [Accessed: 14-Apr-2021]
- 7-segment serializer (four displays) http://www.secs.oakland.edu/~llamocca/Tutorials/VHDLFPGA/Vivado/Unit_7/serializer.zip [Accessed: 14-Apr-2021]