

Battleship!

Brian Wills
Jonathan Nguyen

ECE 2700 Final Project





Introduction

Summary

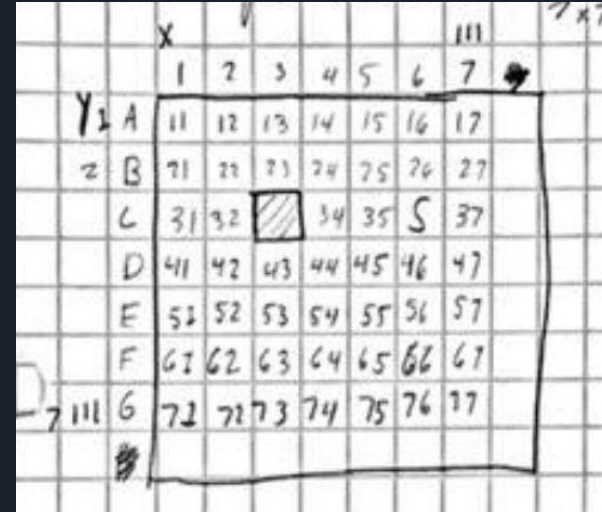
- Main project goal: implementing the classic board game *Battleship* onto an FPGA
- Battleship is a two-player game where players trade turns trying to sink the other's fleet of ships

Content List

- Base Design / Conceptual Planning
- Components
 - Registers
 - Comparator
 - Serializer
 - Multiplexers
 - Demultiplexers
 - Finite State Machine
- Project challenges/ revisions
- Final Digital System Design
- Sources

Base Design / Conceptual Planning

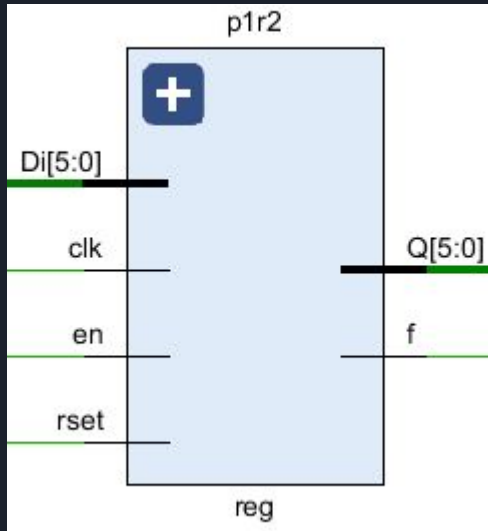
- Gameboard was chosen to be a 7x7 grid compared to typical 10x10 grid
 - Rows are designated by letters, columns by number (ex: A7, B5, etc.)
 - 7x7 grid as chosen for simplifying the bits needed to store values
- Ships only take up one square vs multiple squares in the normal game
- Code will revolve around grid coordinates and comparing coordinates vs ships and misses



A hand-drawn 7x7 grid on graph paper. The columns are labeled with numbers 1 through 7 at the top. The rows are labeled with letters A through G on the left. The grid contains numbers in each cell, representing a coordinate system. For example, the cell at row A, column 1 contains '11', and the cell at row G, column 7 contains '77'. A shaded square is located at row C, column 3. The grid is enclosed in a hand-drawn rectangular border.

	1	2	3	4	5	6	7
A	11	12	13	14	15	16	17
B	21	22	23	24	25	26	27
C	31	32	33	34	35	36	37
D	41	42	43	44	45	46	47
E	51	52	53	54	55	56	57
F	61	62	63	64	65	66	67
G	71	72	73	74	75	76	77

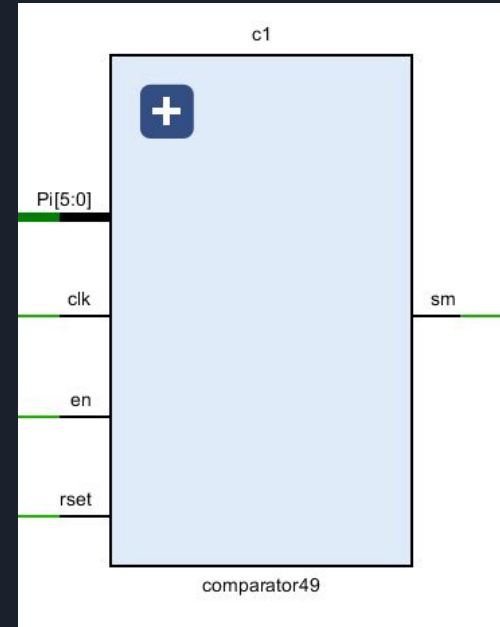
Components (Registers)



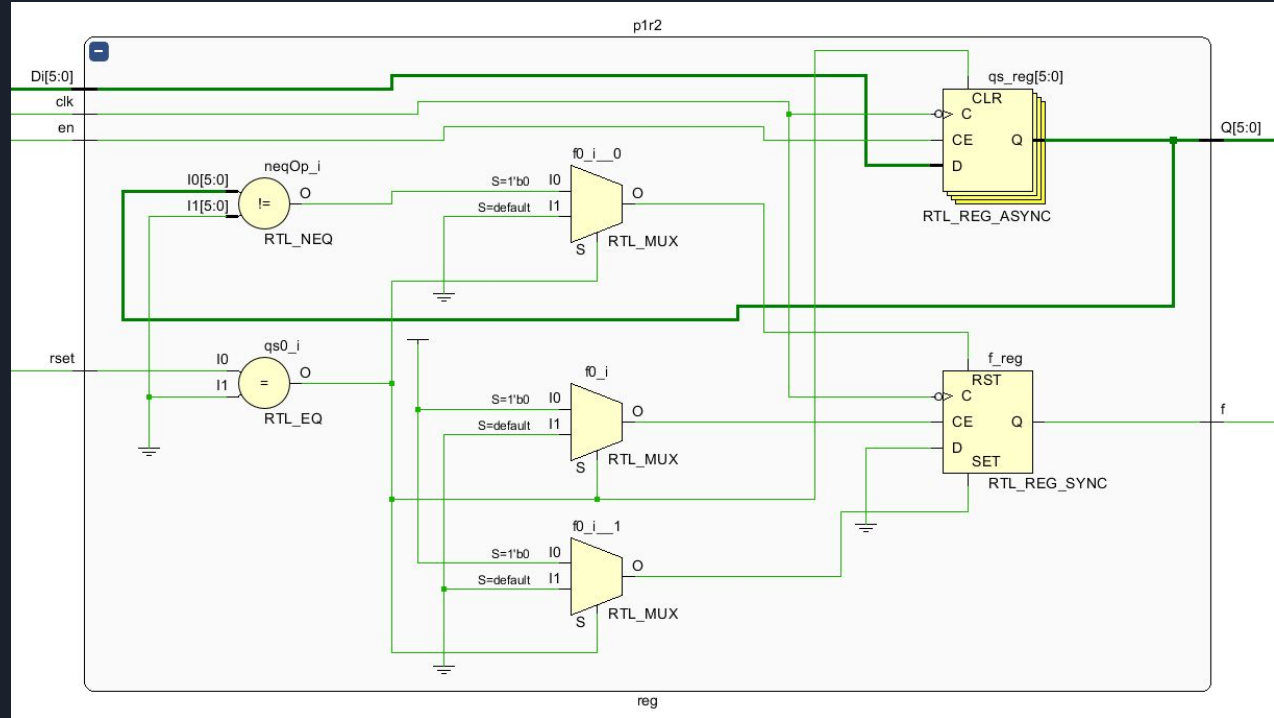
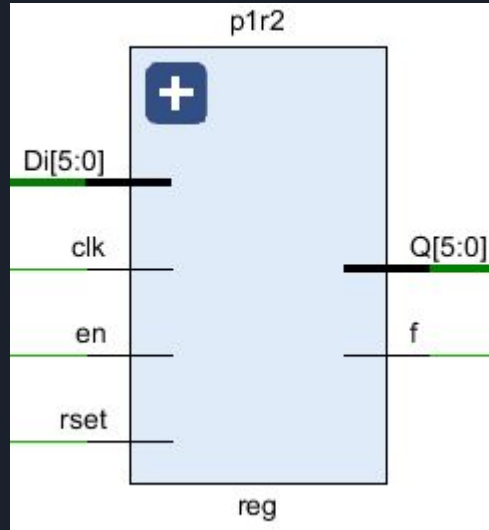
Two Types

Player Ship Location

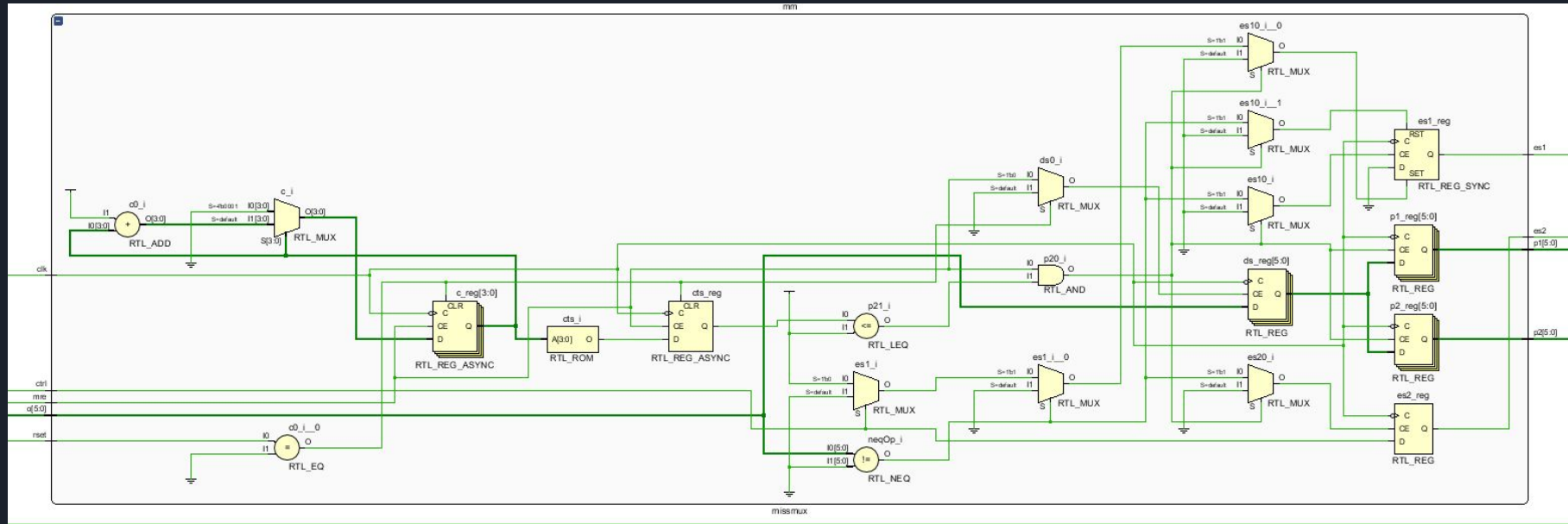
Miss Position



Register Close Up - Player Location

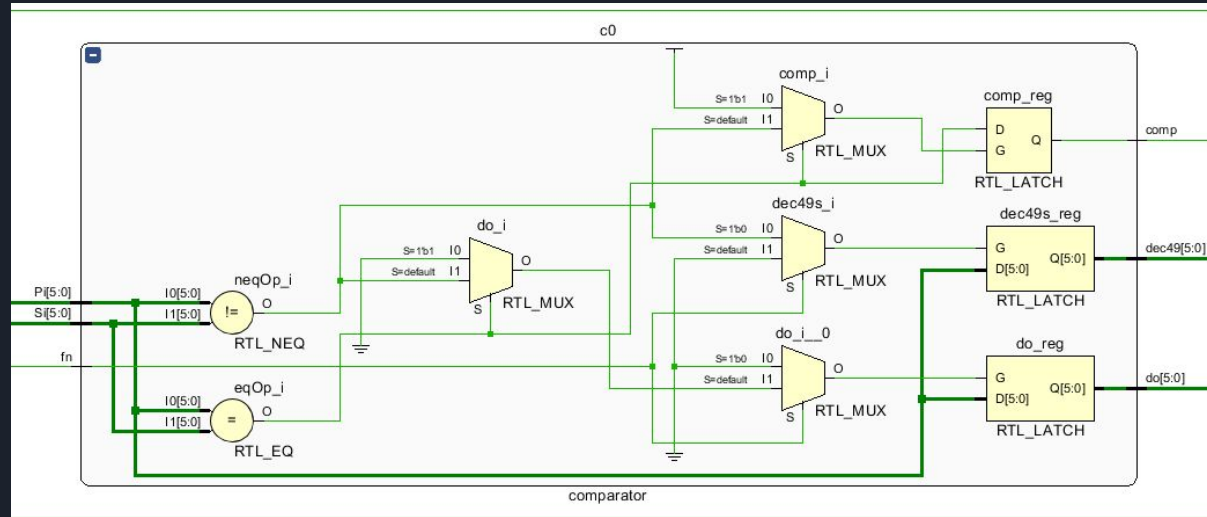
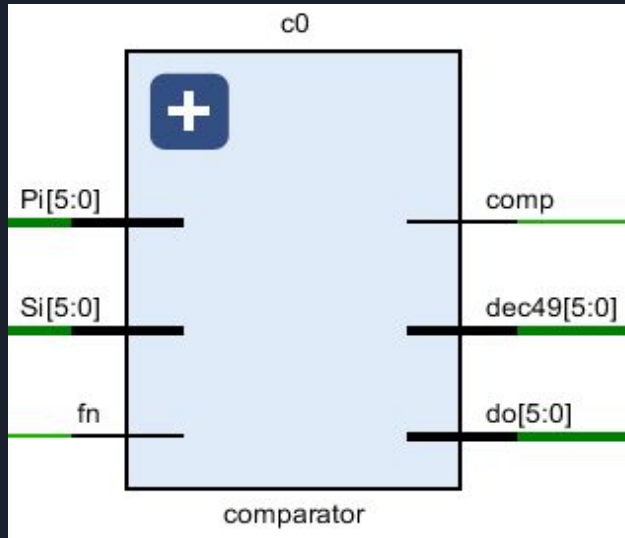


Register Close Up - Miss Position



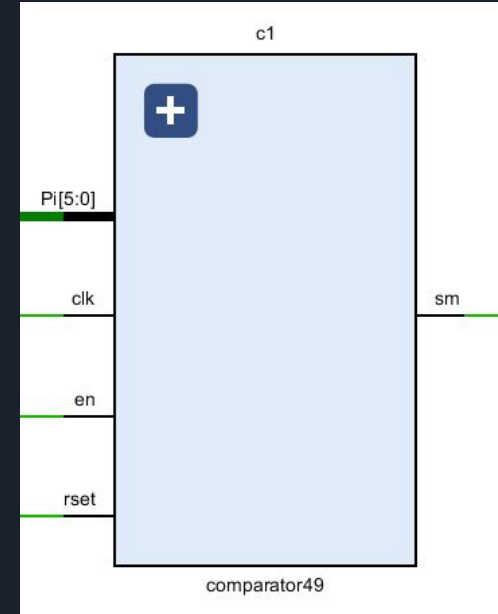
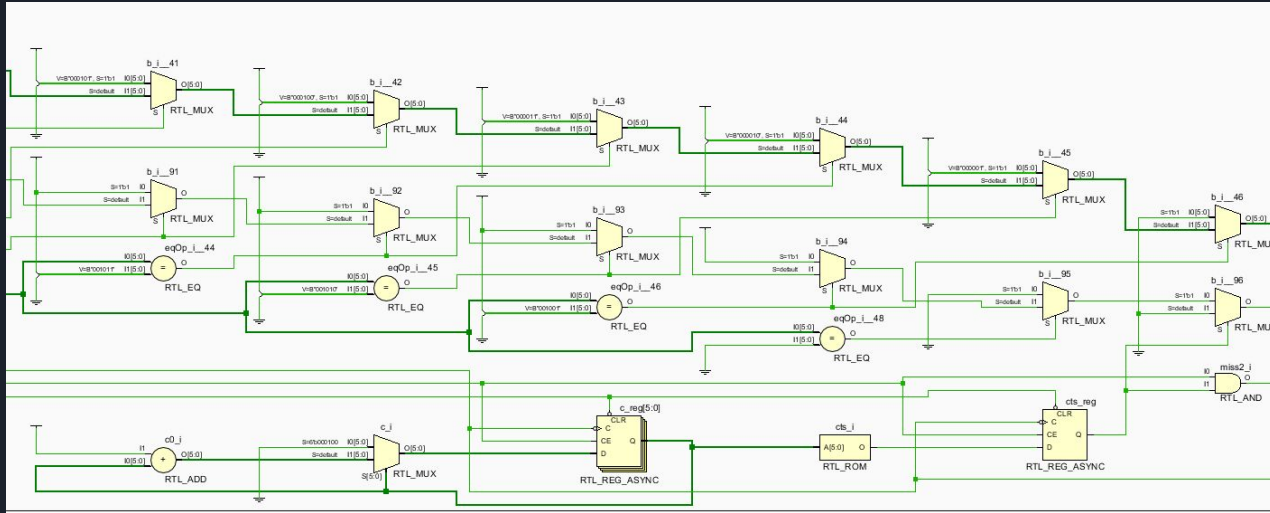
Components (Main Comparator)

- What floats and what does not?



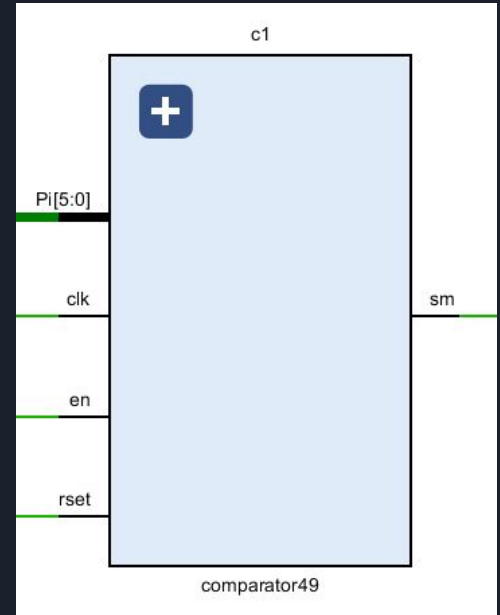
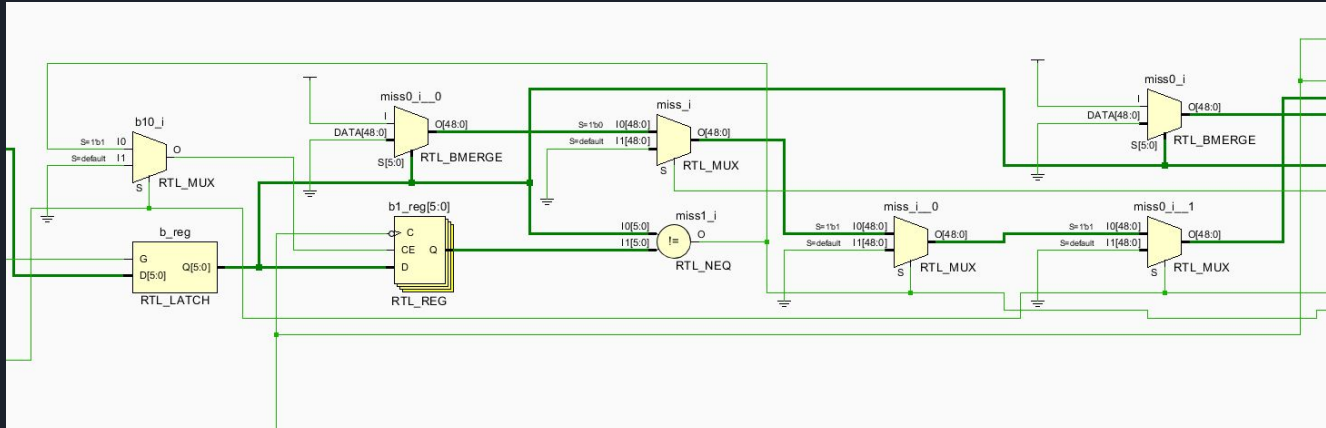
Components (Comparator, 49-bit)

- Where have you already shot?



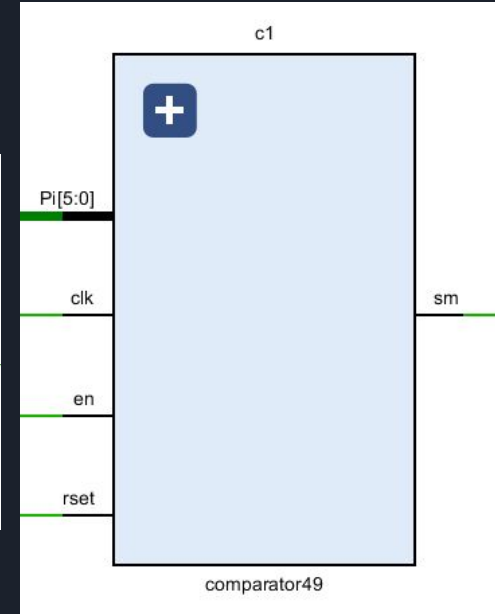
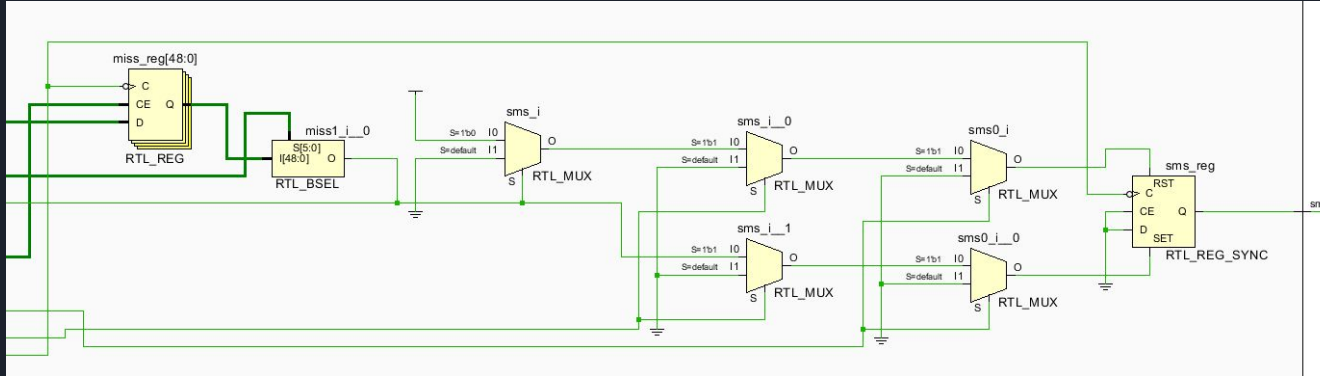
Components (Comparator, 49-bit)

- Where have you already shot?



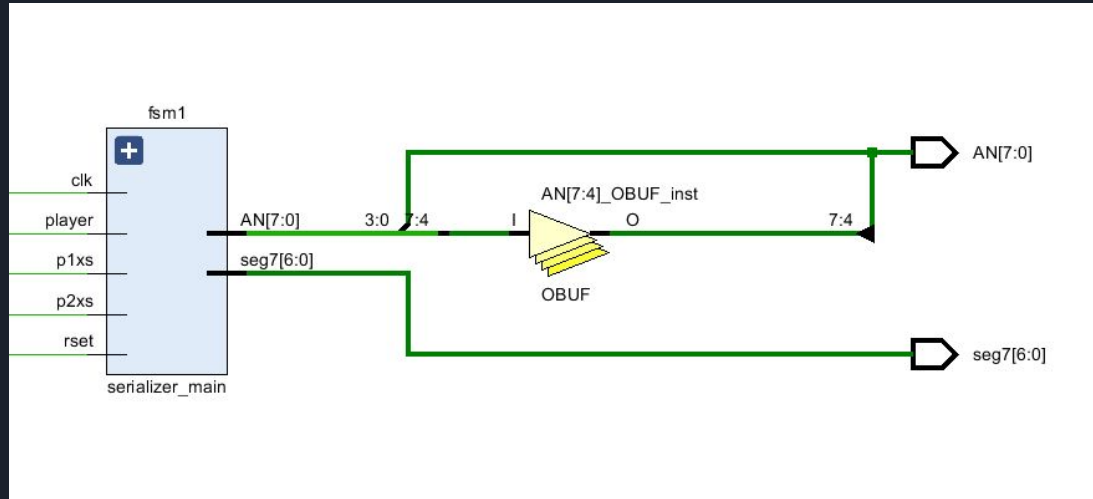
Components (Comparator, 49-bit)

- Where have you already shot?

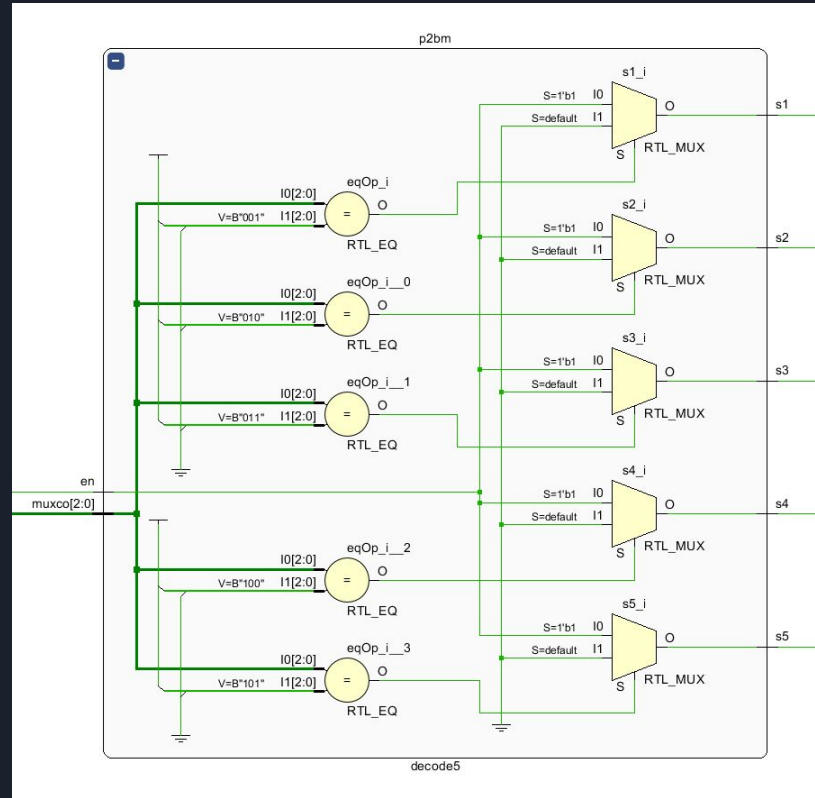
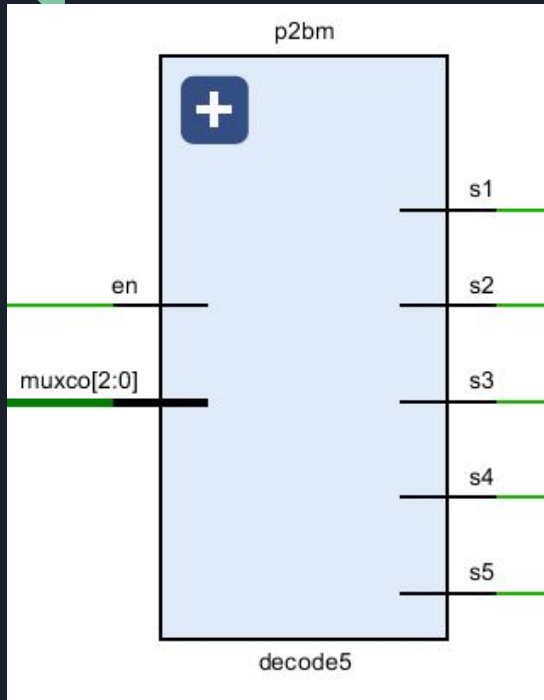


Components (Serializer)

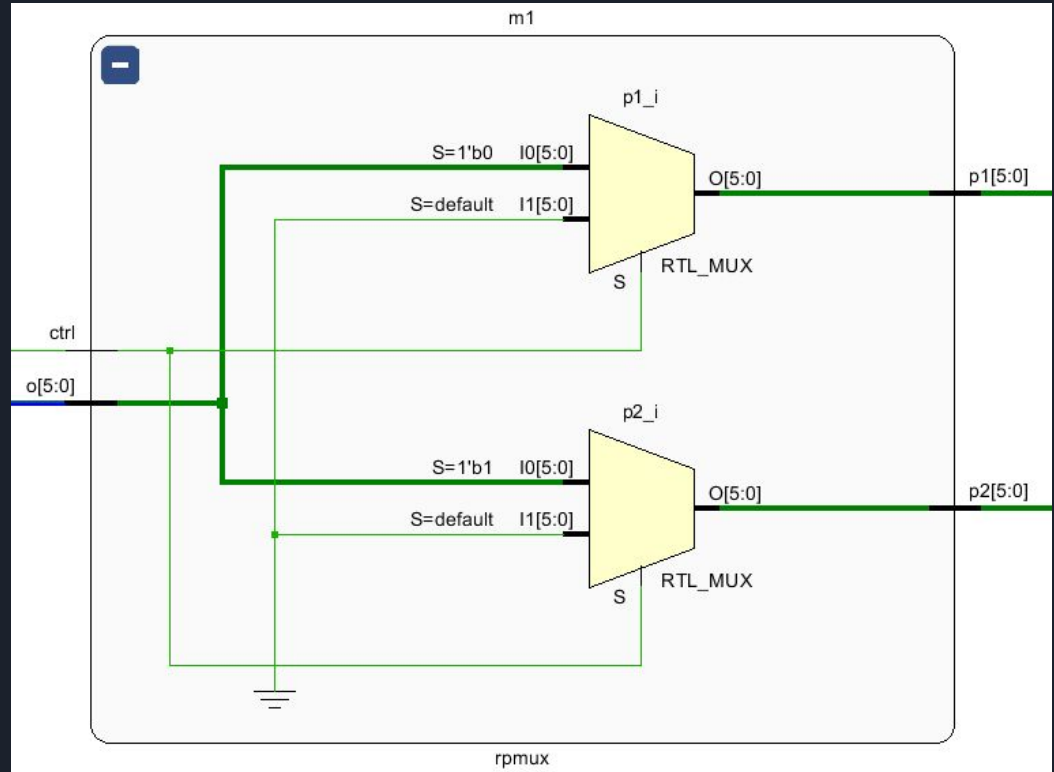
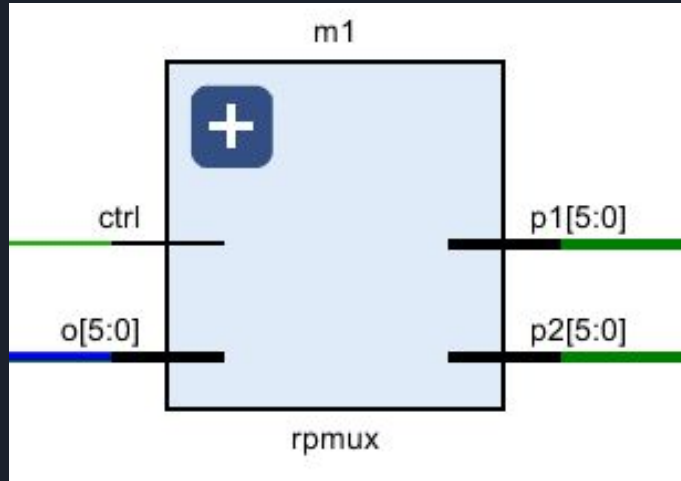
- 4x 7-segment display serializer
 - Based off code from class website/lecture notes
- Displays player turn, current grid position, and eventual player “win screen”
- Serializer is paired with a pulse counter, two decoders, and a simple FSM
 - The hex - to - 7-seg decoder has been slightly modified in terms of how certain inputs trigger specific displays



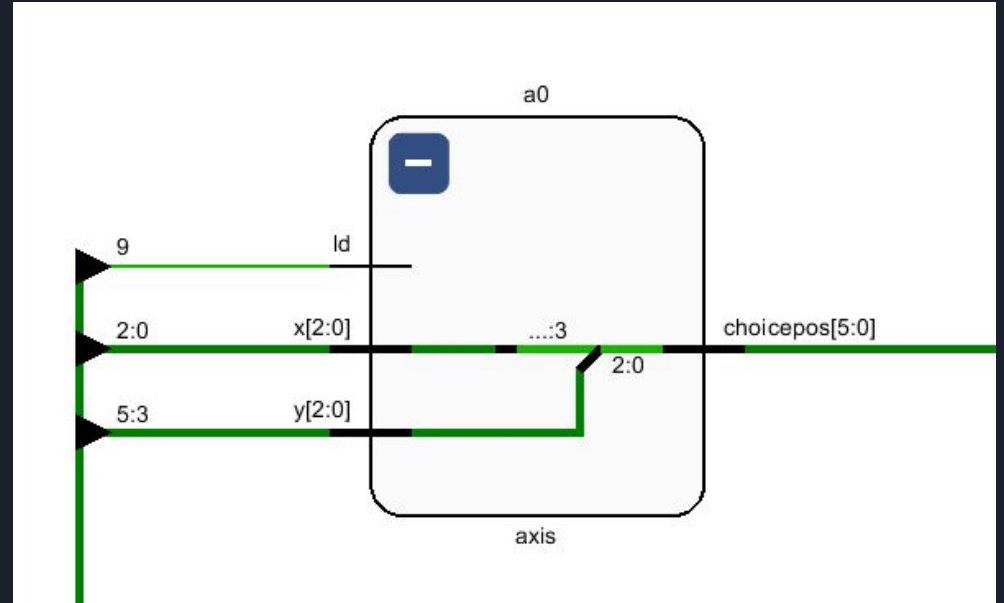
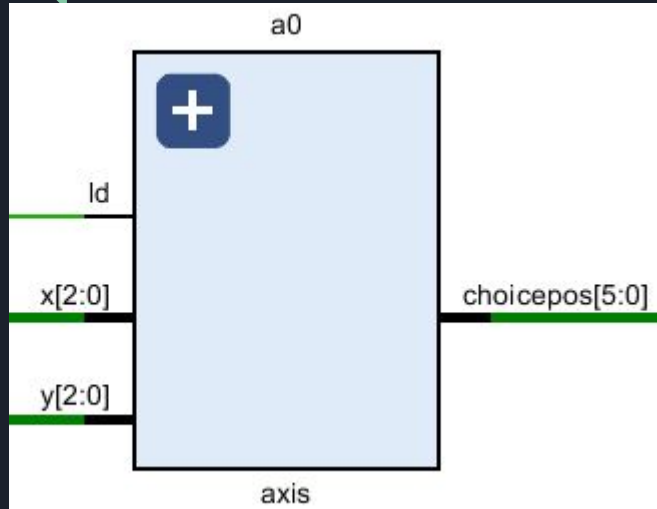
Components (Demultiplexers)



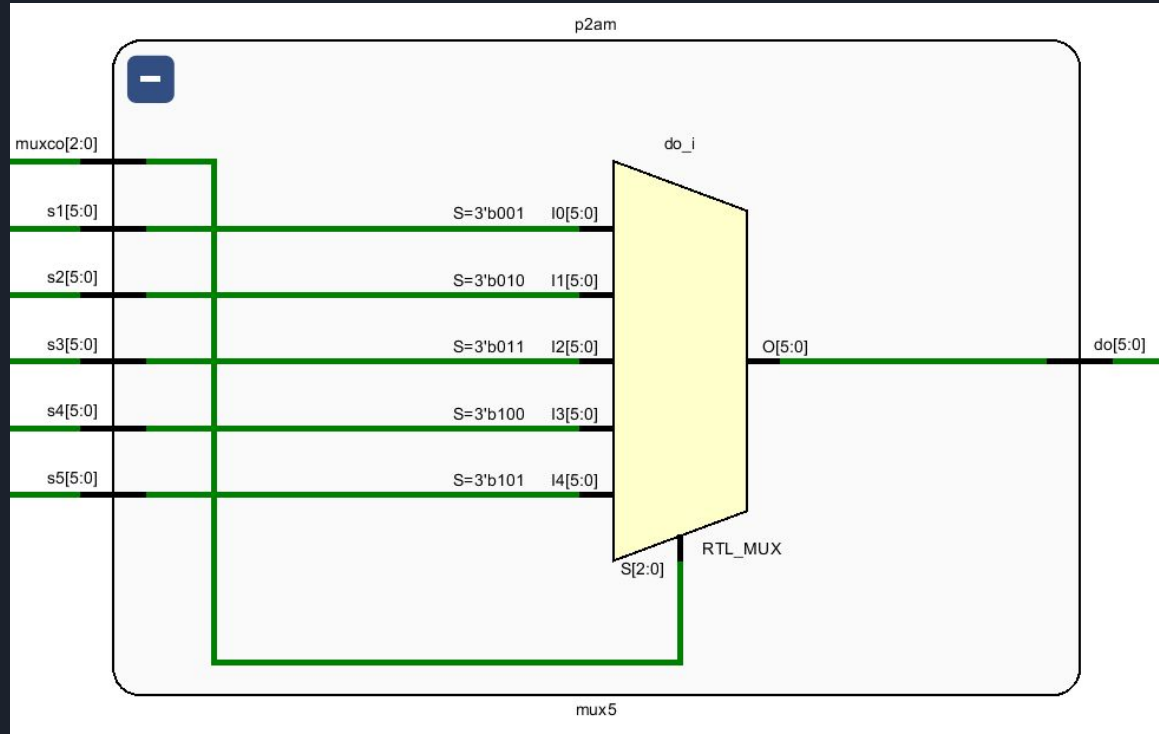
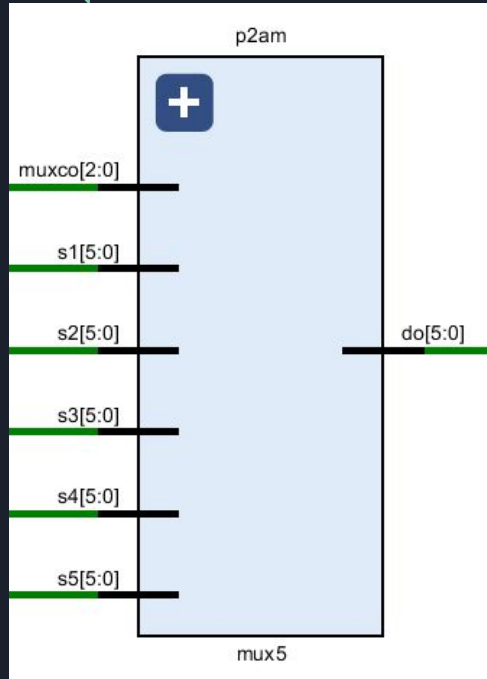
Components (Multiplexers)



Components (Integrator)

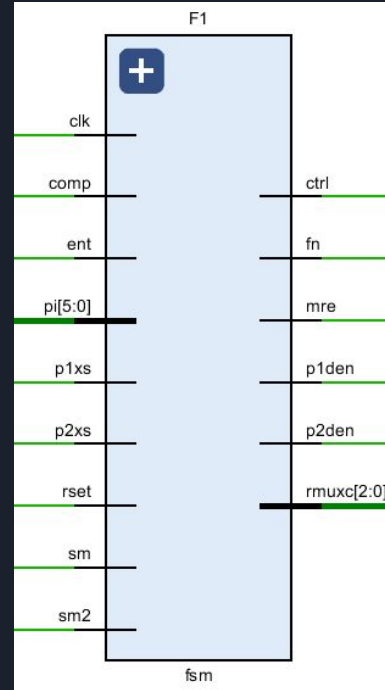


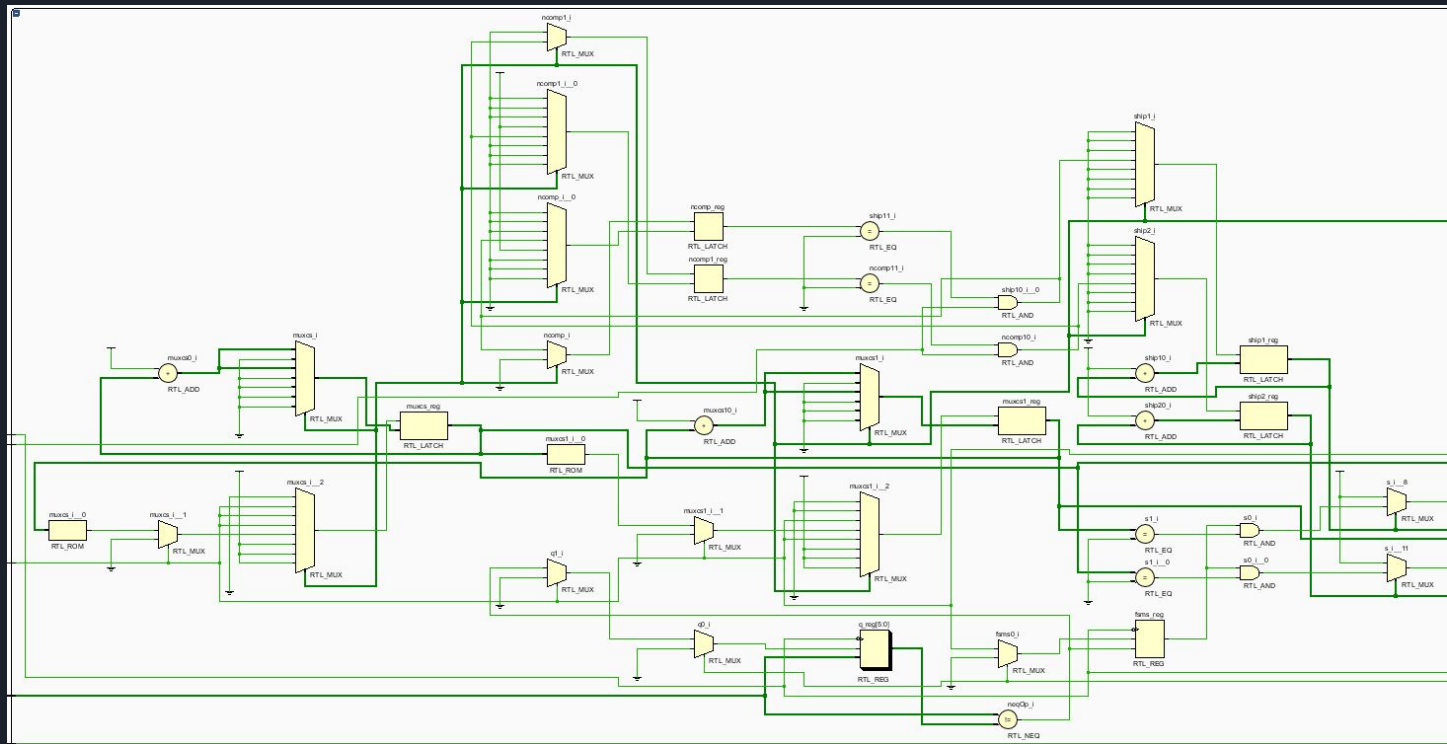
Components (Multiple Input Or)



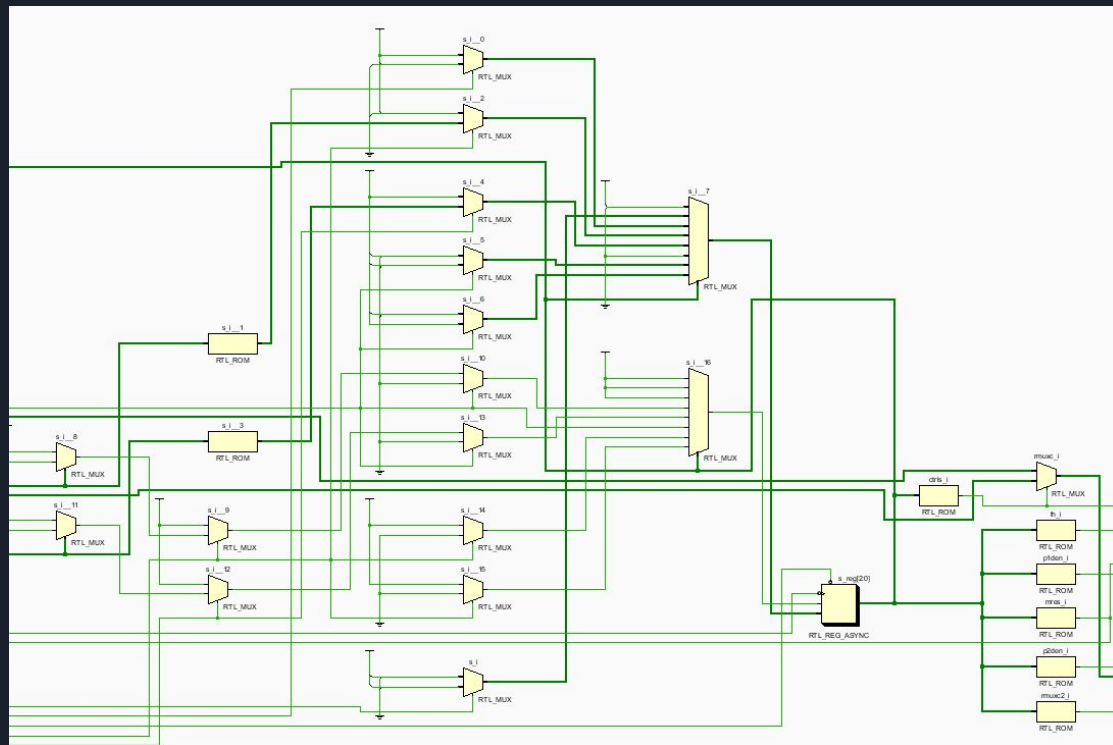
Components (Finite State Machine)

- FSM design is set to rotate between player turns
- Has built in functions to check for:
 - Ship count
 - When a player wins
 - When a hit is scored
 - Handling coordinate input
 - Handling duplicate coordinate input





Components (Finite State Machine)

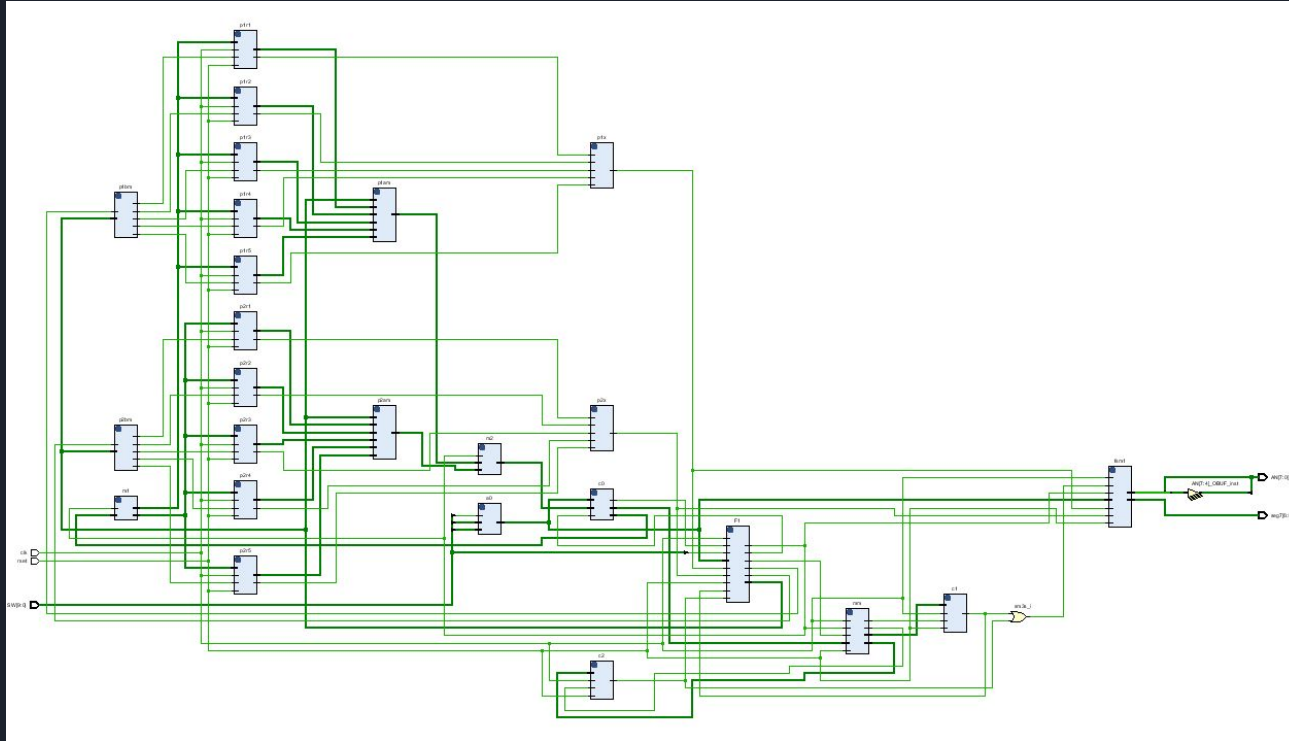




Project challenges/ revisions

- Original plans had a VGA display interface and artificial player to be added to design
 - Both were dropped due to complexity and lack of experience with combining VGA and VHDL
- 7-segment serializer was planned to be more elaborate (possibly using all 8 displays on FGPA)
 - Revised plans to incorporate four displays similar to design from lecture notes due to limitations of FGPA and handling of various inputs for displaying
- Comparator design
 - Massive amount (49-bits) to compare to keep track of ship locations as well as misses throughout entire grid
- FSM design
 - Needed to be able to cycle between player turns without overwriting opposite player components such as player input/registers/etc.
 - Synchronization issues are the main source of constant revisions to the code, aligning each signal up properly or working the code so that signals would not get crossed.
 - Circuit still contains timing bugs - crossing of synchronizing/signals miss-register signals

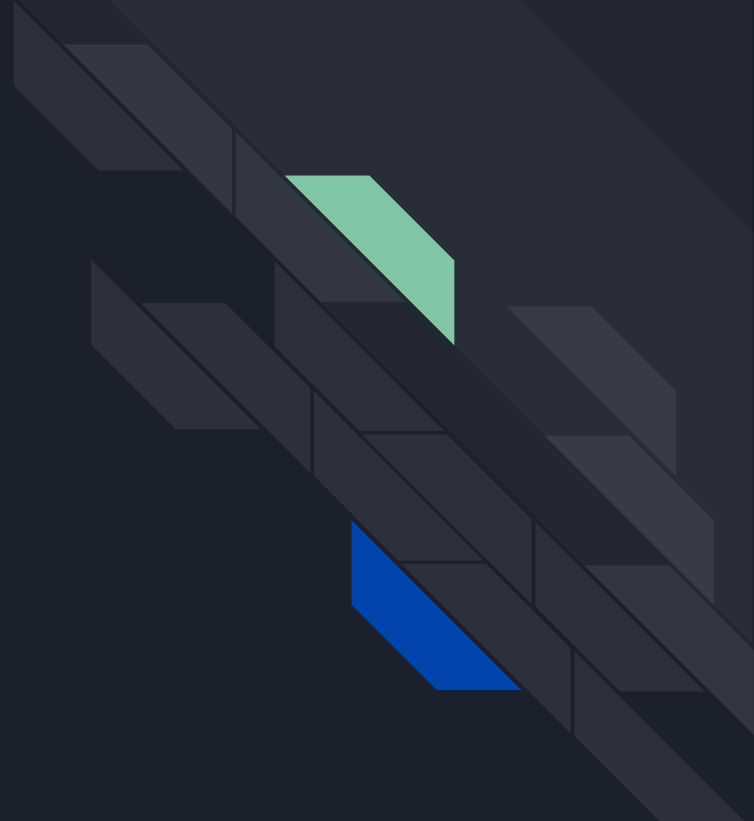
Final Digital System Design





Surrogate Demo

Thank You for your
time. Any Questions?





Sources/ Citations

- Title Picture
 - <https://www.microsoft.com/en-us/p/battleship-war-tactics/9pnnr1hvws95?activetab=pivot:overviewtab>
- VHDL Resources
 - <http://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html>
 - <https://www.ics.uci.edu/~jmoorkan/vhdlref/contents.html>
 - www.stackoverflow.com
 - Free Range VHDL Book by Bryan Mealy and Fabrizio Tappero
- Battleship Info
 - [https://en.wikipedia.org/wiki/Battleship_\(game\)](https://en.wikipedia.org/wiki/Battleship_(game))
- OU Emblem/Logo
 - <https://oakland.edu/about/ou-motto-seal-and-logo/>