Banner on a Seven Segment Display

With Various Scrolling Speeds

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***Abstract*—Our group used the Nexys A7-50T FPGA Trainer Board to design a scrolling message on a seven segment display. It used all eight of the seven segment displays and our message scrolled at various speeds, shifting letters from right to left in direction. The scrolling message combined all of the knowledge we have learned throughout the semester in ECE 2700 and incorporated many of the tools we had at our disposal in the class. The message displayed on the seven segment display was pre-coded. We utilized basic VHDL code descriptions to best implement the various elements needed for the project and interconnected them with one another to form the complete circuit.**

I. Introduction

For our project, we implemented a digital logic design using VHDL code on the Nexys A7-50T FPGA Trainer Board to display the pre-coded message, "ECE2700," onto eight seven segment displays. The message was designed to shift at various scrolling speeds, shifting the letters from right to left. We incorporated four different counters that determined the speed of the message being displayed. Many of the concepts that were introduced during the class were used in the design of this project. Additionally, the ideas that were covered and experimented on in laboratory assignments were very useful in our design for our circuit. Concepts such as the counters, the multiplexor, the finite state machine, the RAM shift register, and the seven segment serializer were covered heavily in the development of our digital circuit. An important feature to note about the serializer is it was designed to turn on and off each of the displays and shift the letters at a rate fast enough at which the human cannot detect. The motivation for the design was to share messages and affect their shift speed on the seven segment displays. Some useful applications of our project include digital clocks, clock radios, and basic calculators. Additionally, uses for our project we were unaware of are gas pumps, odometers as well as electronic billboards.

II. Methodology

A. Design

The project design was mild in complexity, but ultimately effective in achieving our objectives and utilizing our knowledge and resources learned throughout the semester. The final product of the design was a seven segment display banner, which shifts our message "ECE2700" from right to left at different speeds. A right to left shift design approach was taken to make our message easier to read. To structure the project design, our circuit had different components including four counters, a 4-to-1 multiplexor, a finite state machine, a RAM shift register, and a seven segment serializer. By first drafting a block diagram of the design, our team was able to visualize all the inputs, interconnections, and outputs in the system. With all the components divided up between the group members, we were able to effectively bring everything together to write a top file and complete the circuit. Also, having each member design a specific part prevented any overcomplication when constructing the circuit as a whole and made the debugging process more manageable.

B. Implemenation

The design was implemented using VHDL and the Nexys A7-50T FPGA Trainer Board. Since the workload between the team was divided by component, the circuit still had to be wired up in a top file. Given that each component was correctly implemented on its own, the top file was relatively painless with some minor editing having to be done to each component. For example, the RAM shifter was originally set up as a RAM emulator, but unneeded components such as the decoder and extra MUX were taken out to accommodate the final design. The scroll speed of the message was varied by the selected output from one of the 4 counters. The counters to be selected from include 2, 1, 0.5, and 0.25 second counters. Each value of the counter was calculated to be 200 x 10^6, 100 x 10^6, 50 x 10^6, and 25 x 10^6. A counter can be selected by the user toggling two switches that represent the selector of the 4-to-1 MUX in which the outputs of the counters are fed into. The output from the selected counter was used as the enable signal for the FSM and RAM shifter that controls shifting the message. The FSM had 7 states which fed each character of the message into the RAM shifter. The RAM shifter had 8 registers representing each seven segment display on the Nexys A7-50T FPGA Trainer Board and the bits that represent the LEDs on the displays. However, the outputs from the RAM shifter were only 4 bits, which is why those bits fed into a seven segment serializer with a hex to seven segment decoder to interpret them for the displays.

III. Experimental Setup

Each of the circuit components was constructed using VHDL code. This code was written and simulated in a software known as Vivado 2020, created by Xlinix. The simulation process consisted of viewing the timing diagram of each member's component under certain conditions specified in the testbench. Once the simulation steps were complete, the components were wired together in a top file to complete our final design. The circuit was downloaded to a Nexys A7-50T FPGA Trainer Board using its constraints file and binding each of the circuit's inputs and outputs to the board. Our project consisted of two switches as inputs and a seven segment display as an output. The expected results from the circuit's implementation were to view a scrolling message of "ECE2700" across all eight of the seven segment displays from right to left and adjust the speed at which the message scrolled using different combinations of the switches.

IV. Results

Originally, our results consisted of random characters scrolling across the seven segment displays in the proper right to left direction. This issue was easily corrected by changing the order of the bits representing the LEDs of the seven segment displays in the board's constraints file. The successful result after this fix was the message "ECE2700" scrolling right to left across all eight seven segment displays of the Nexsys A7-50T FPGA Trainer Board. Additionally, the speed at which the message scrolled was properly adjusted based on the switch combination the user provided. These results were as expected and apply very well with many of the topics that were learned in class. It provided experience in properly writing and simulating VHDL code, designing block diagram models of a functional circuit, debugging issues with circuit implementation, and much more. Overall, the project went as planned and there were no unexplainable results that occurred.

Circuit Demo Link : https://youtu.be/YiEVbHPW3QU

Conclusions

This project was very interesting and similar to the laboratory assignments we worked on throughout the semester. The project allowed us to collaborate as a group and put forth a solid foundation of knowledge we all obtained during the class. We incorporated a great deal of concepts and a plethora of components that were well integrated into our final project's design. Another takeaway from the project was that we were able to get more practice with debugging our code of issues with signal names and putting together the coded VHDL files of four different creators. We had a great plan heading into the code as we designed our block diagram beforehand. Additionally, we divided and conquered the work evenly and that led to an easier collaboration process. To further enhance upon our project complexity, we could have used an LCD display to create a more feasible use for the project in today's day and age.

References

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[2] "Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics." Xilinx.com, Xilinx, Inc., 13 Apr. 2017, www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_ Sheet.pdf

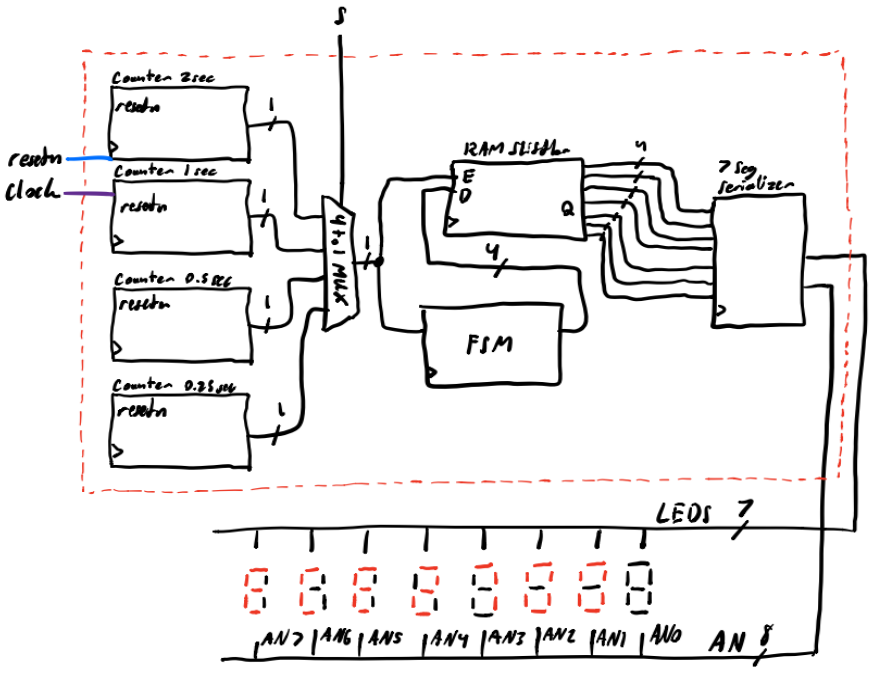

Figure 1. Top Level Block Diagram

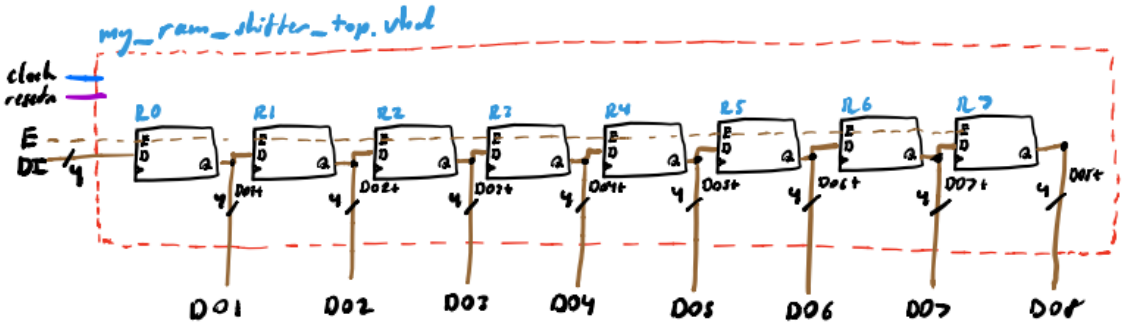

Figure 2. RAM Shift Register Block Diagram

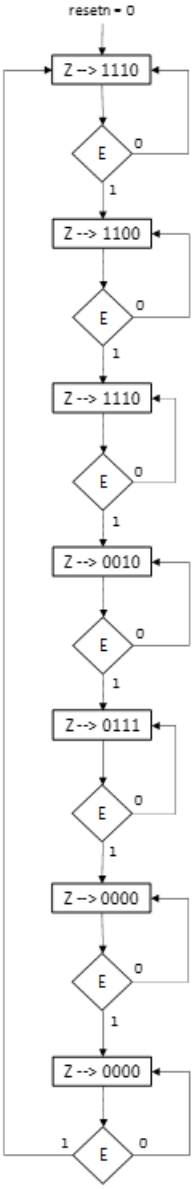

Figure 3. RAM Shift Register FSM State Diagram

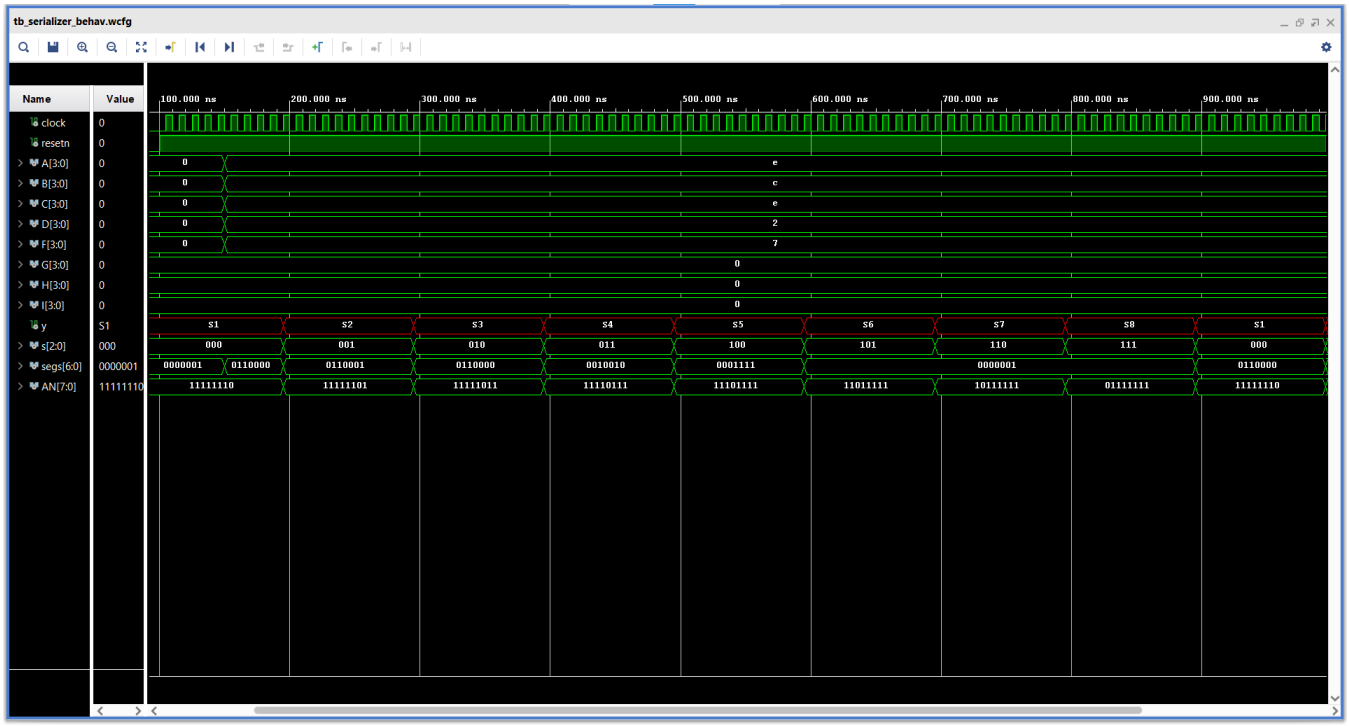

Figure 4. Seven Segment Serializer Timing Diagram