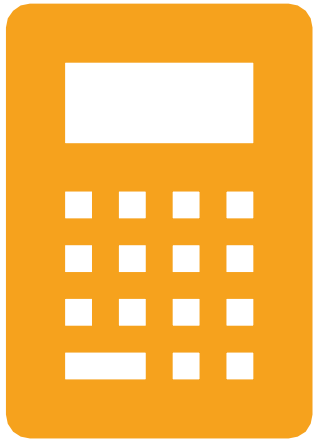


NUMBER CRUNCHER

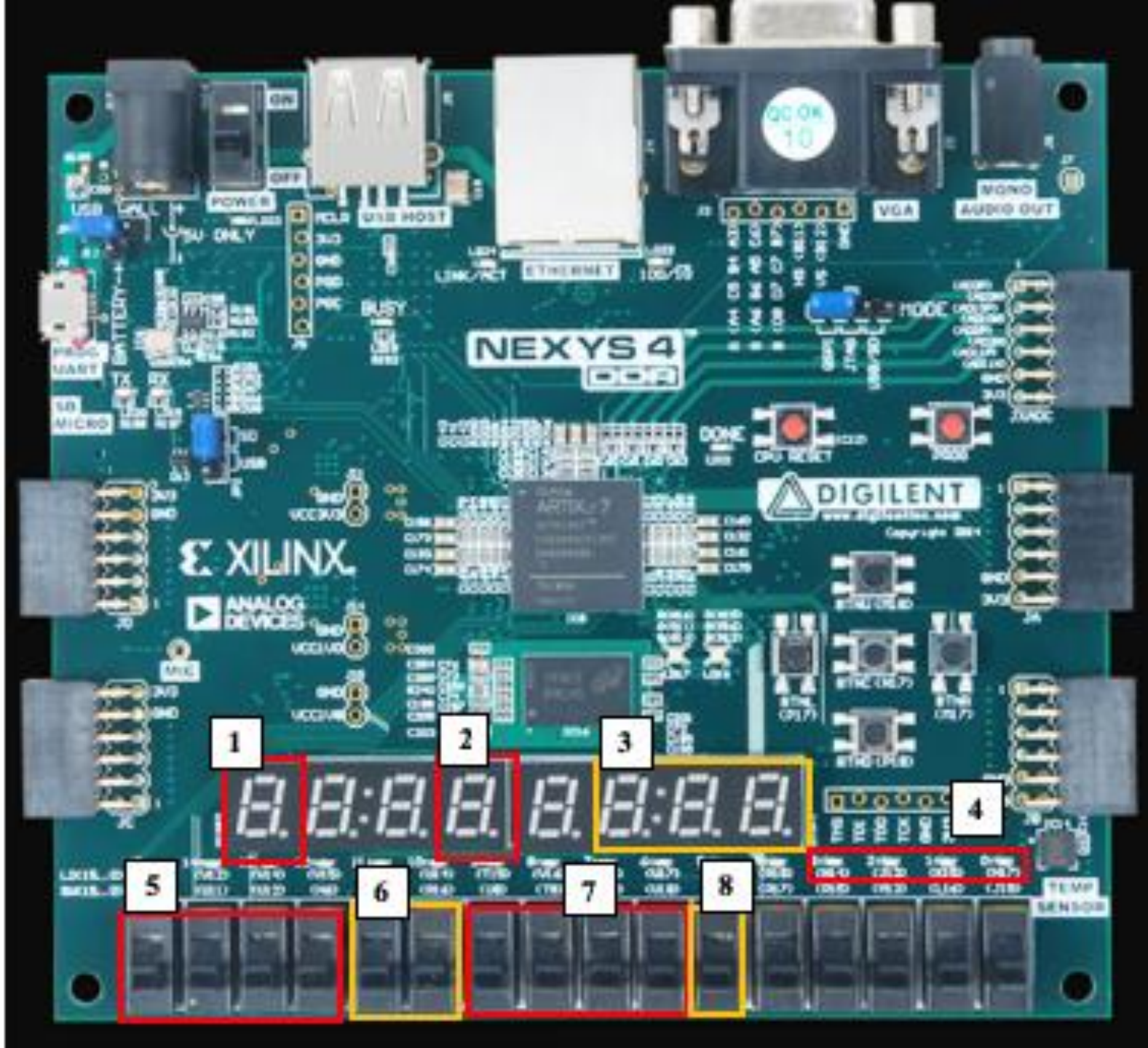
By: Mohamed Abbas, Paul Shammas, Feras Zari

INTRODUCTION

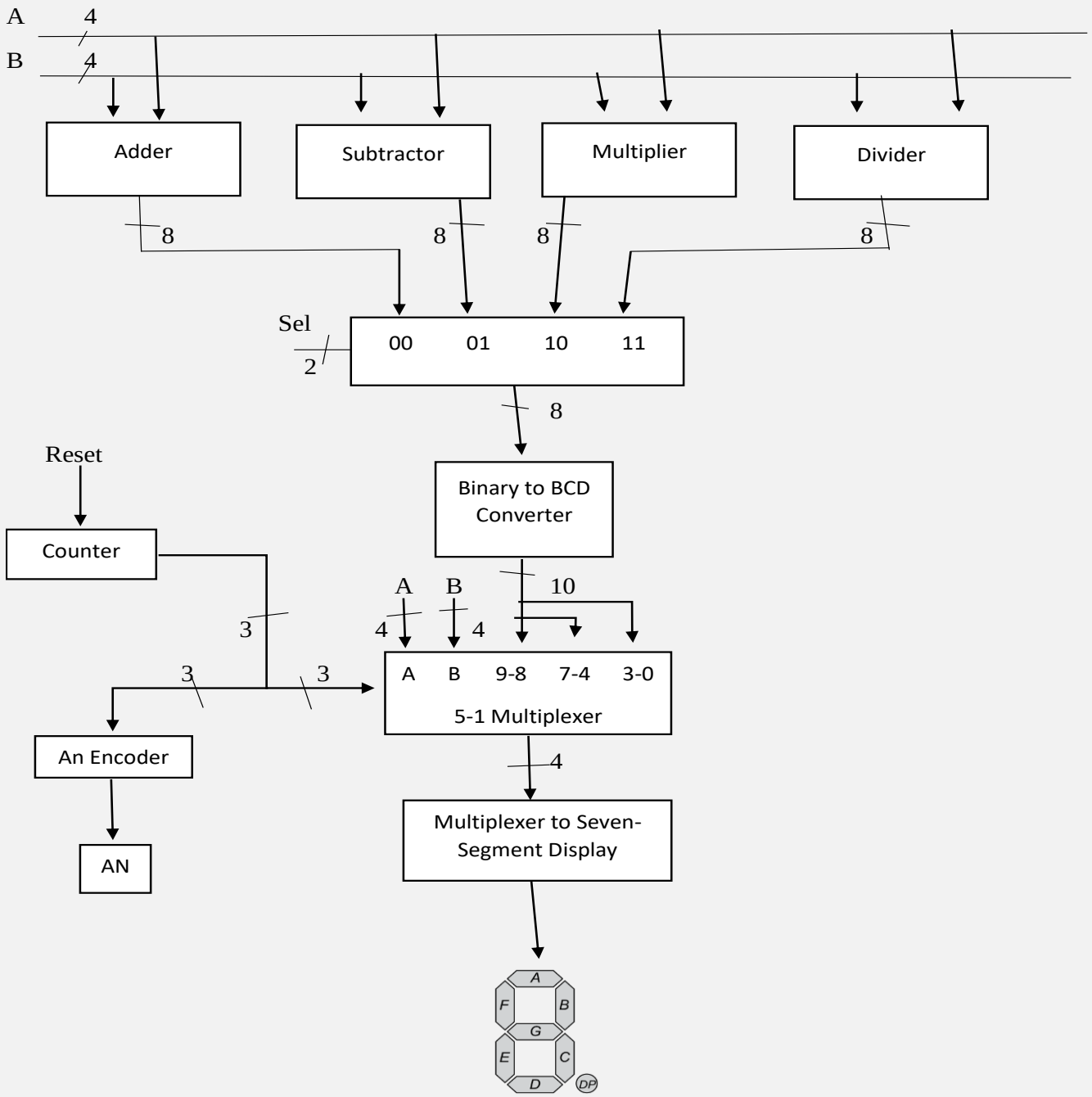
- Interactive Number Cruncher
  - Number Cruncher capable of computing 4-bit mathematical operations such as Addition, Multiplication, Subtraction, and Division inputted using unsigned binary numbers.
- Inputs
  - Switches used for an enabler, switching between mathematical operations, and inputting binary numbers.
- Outputs
  - 7 Segment Display

FPGA LAYOUT

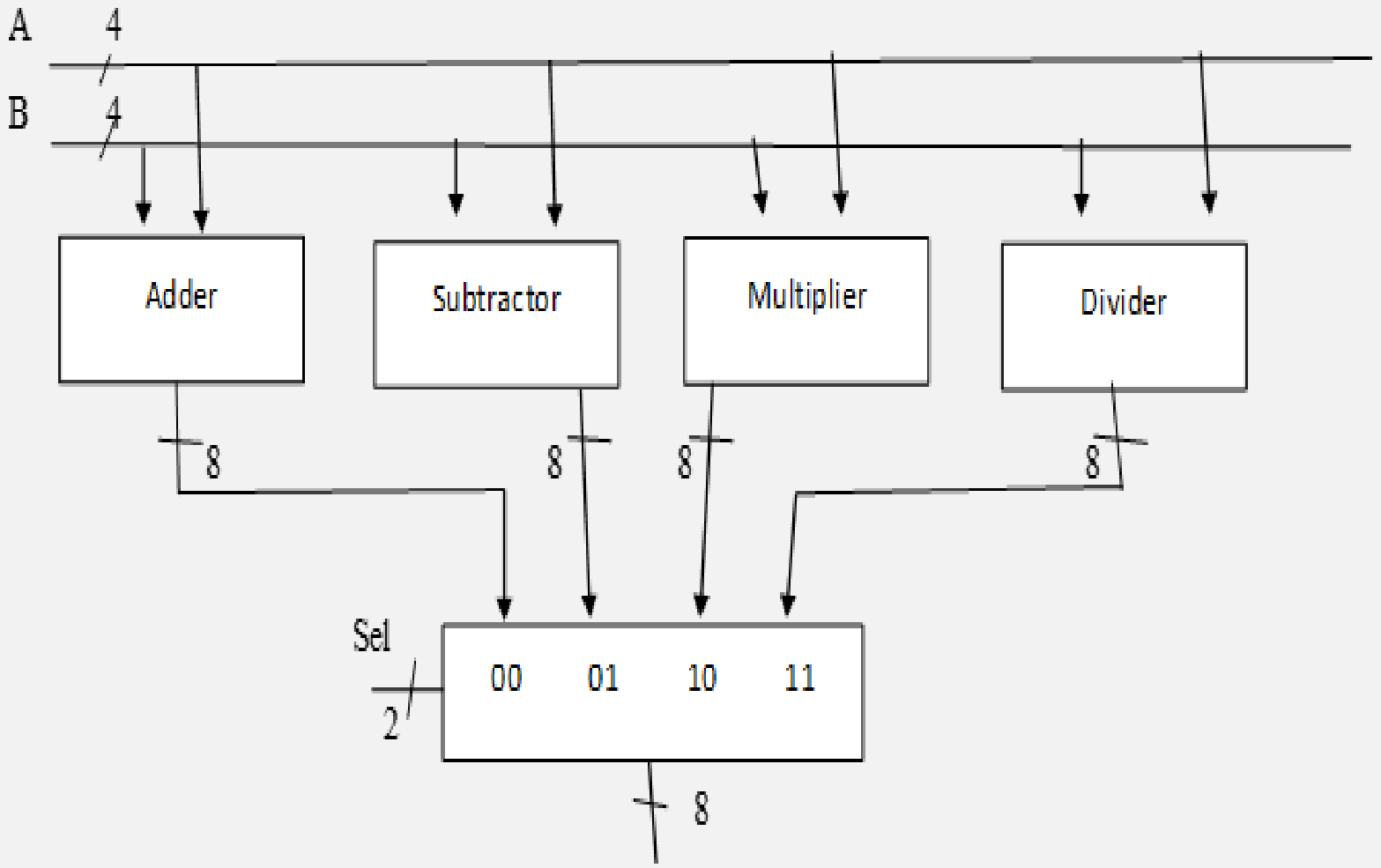
1. A Input Display
2. B Input Display
3. BCD Output Display
4. Division Remainder (LEDS)
5. Input A (SW15-S12)
6. Operations (SW11-SW10)
    a. Addition (00)
    b. Subtraction (01)
    c. Multiplication (10)
    d. Division (11)
7. Input B (SW9-SW6)
8. Enable for division (SW5)



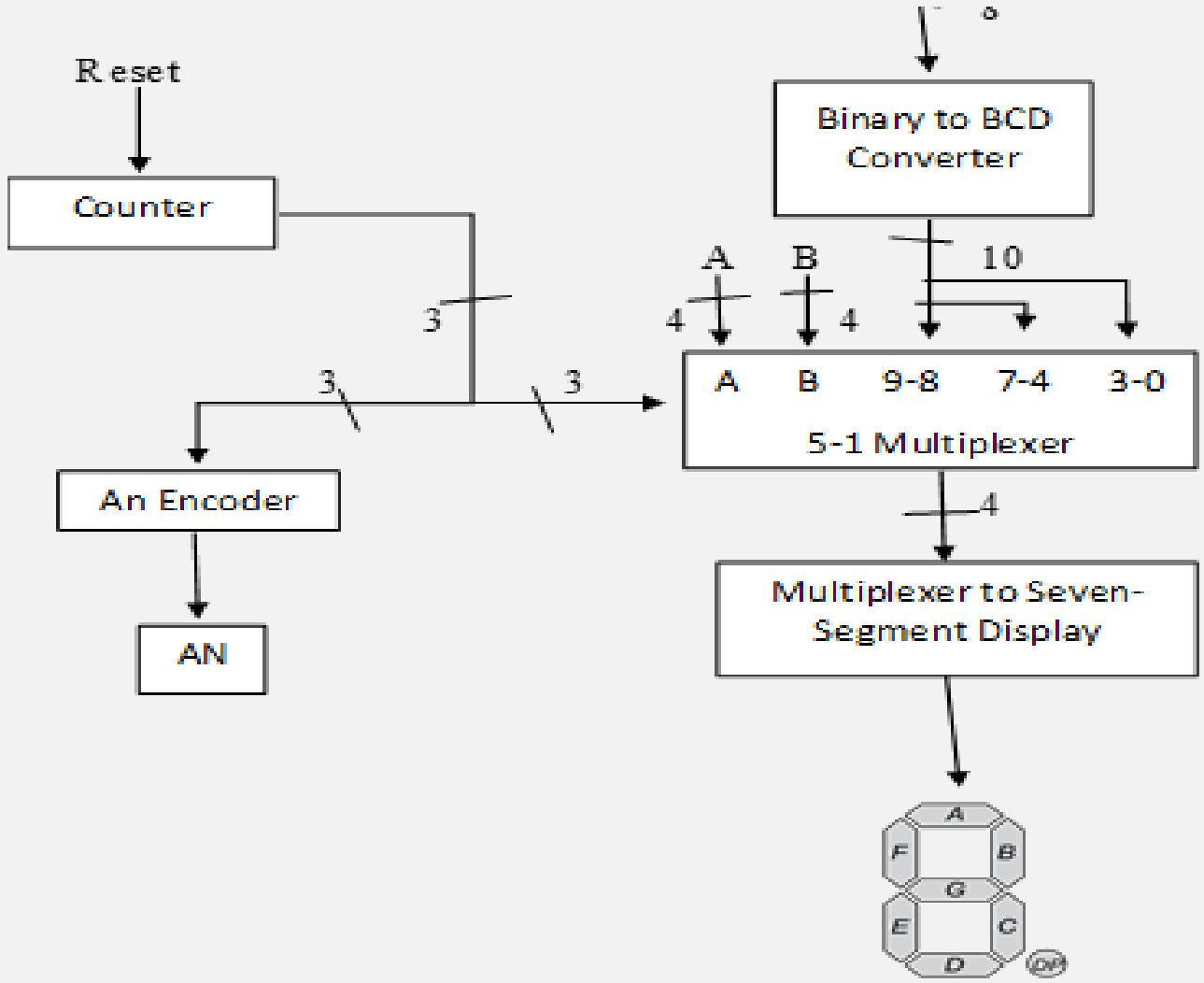
BLOCK DESIGN TOP FILE



TOP HALF OF BLOCK DIAGRAM

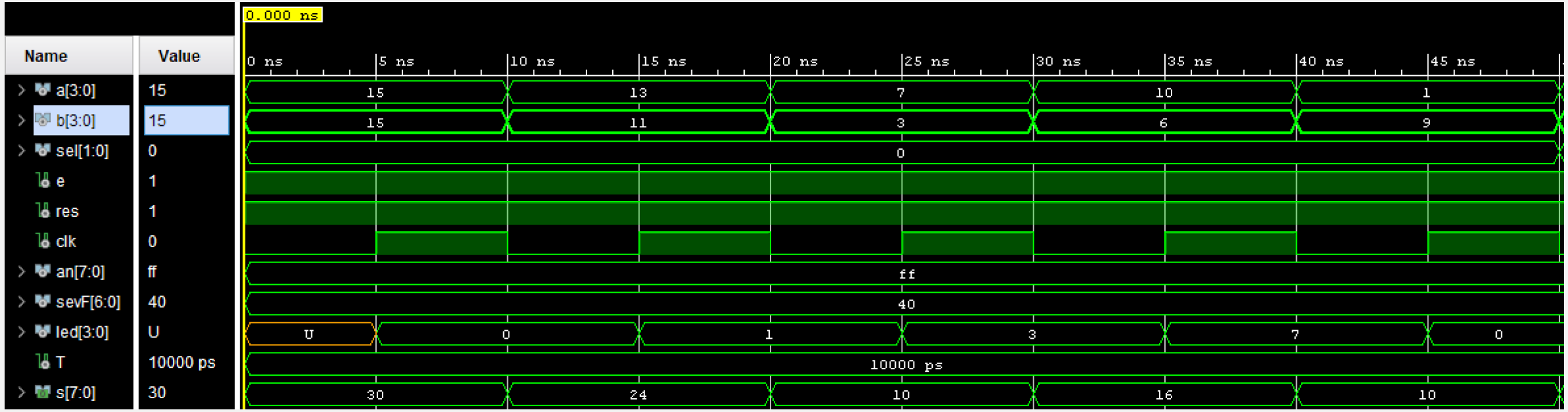


BOTTOM HALF OF BLOCK DIAGRAM



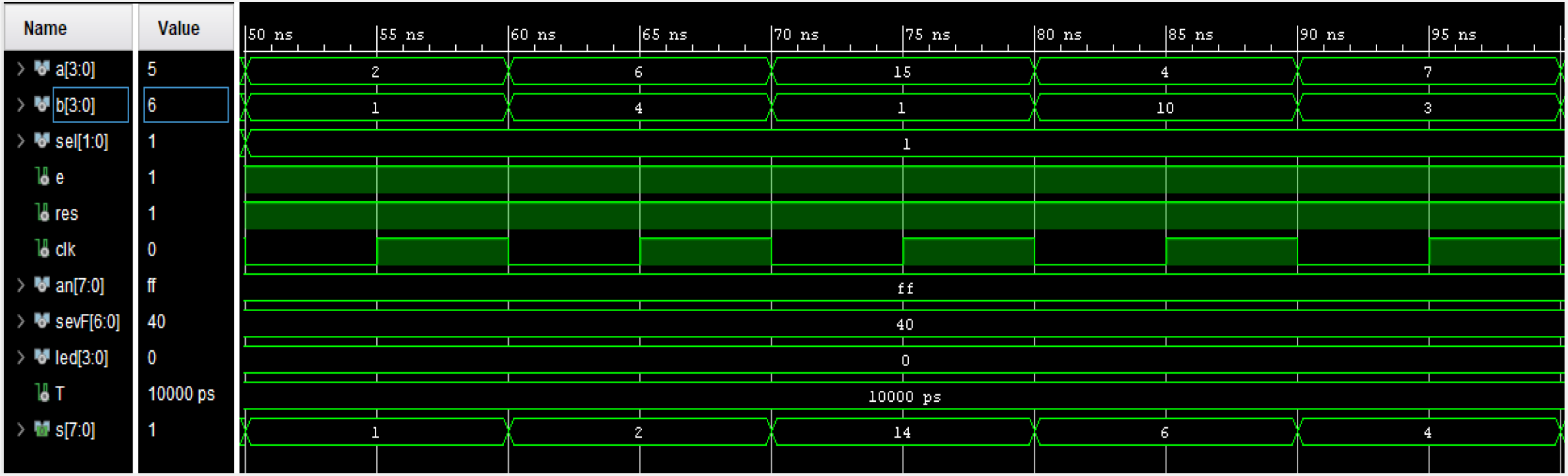
BEHAVIORAL SIMULATION

Addition



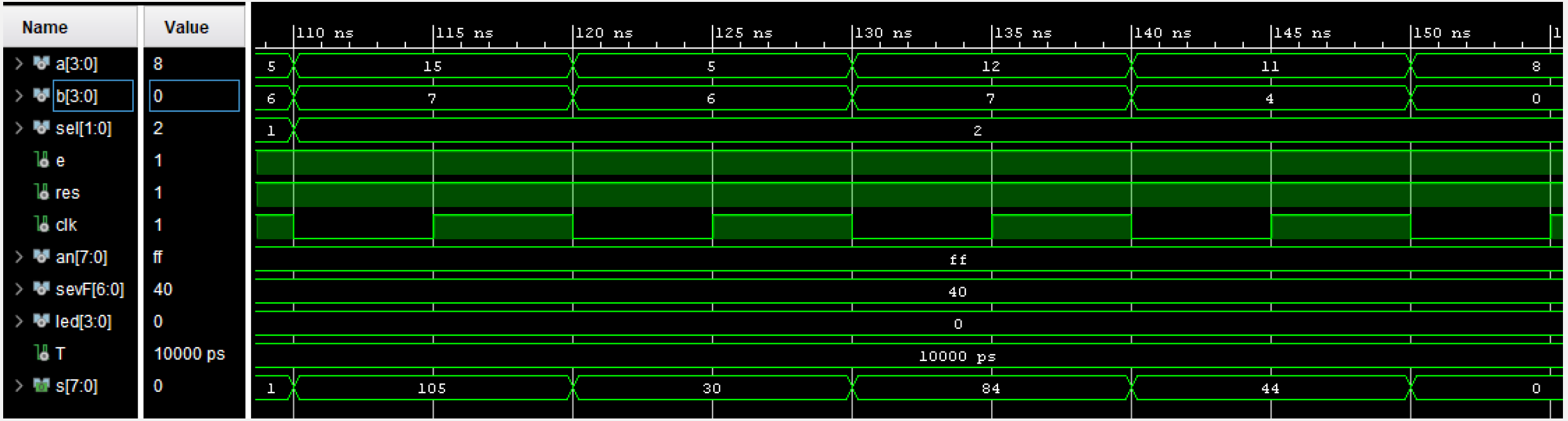
BEHAVIORAL SIMULATION

Subtraction



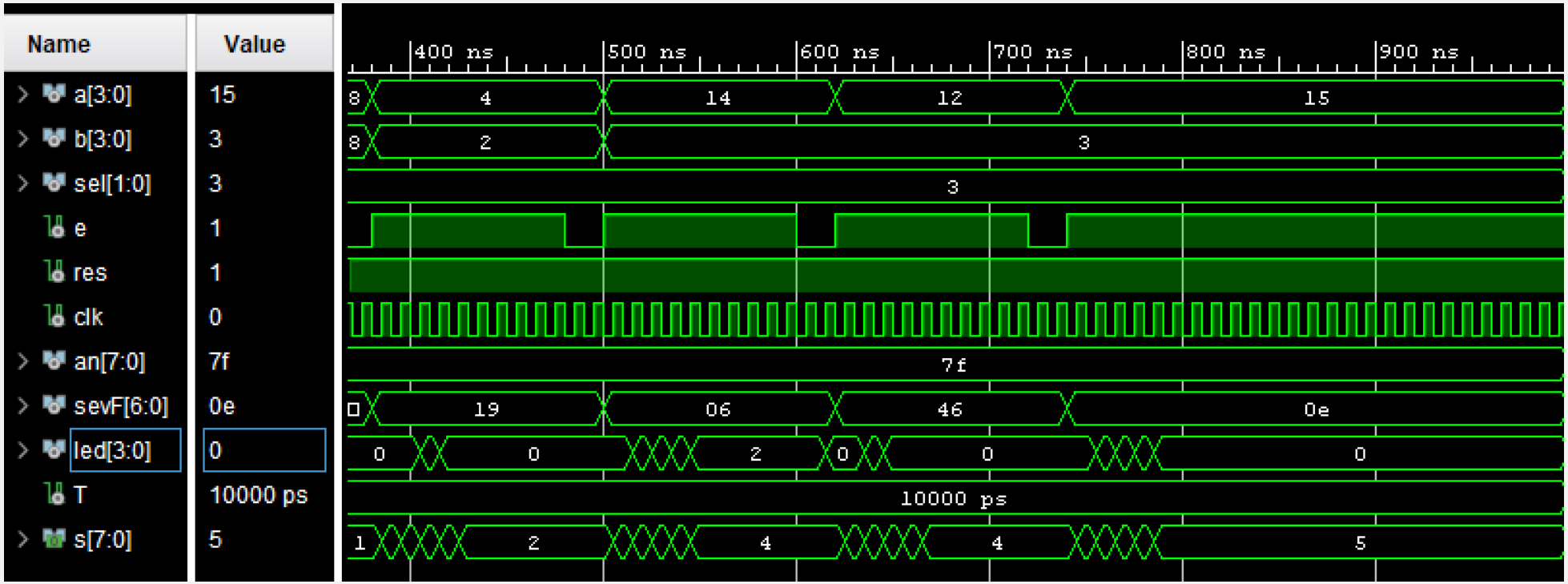
BEHAVIORAL SIMULATION

Multiplication



BEHAVIORAL SIMULATION

Division



ISSUES WHILE BUILDING PROJECT

- Division was difficult to implement however; this was solved after lab 6
- Getting the clock at the correct speed
- Having the anodes select the correct part of the seven-segment display

IMPROVEMENTS

- Incorporate multiple functions such as trig functions, square functions and exponents
- Incorporate a keyboard instead of switches
- Incorporate a LED screen or VGA screen
- Compute operations given negative inputs and results
- Have inputs larger than 4-bits

THANK YOU