BCD TO BINARY CONVERTER

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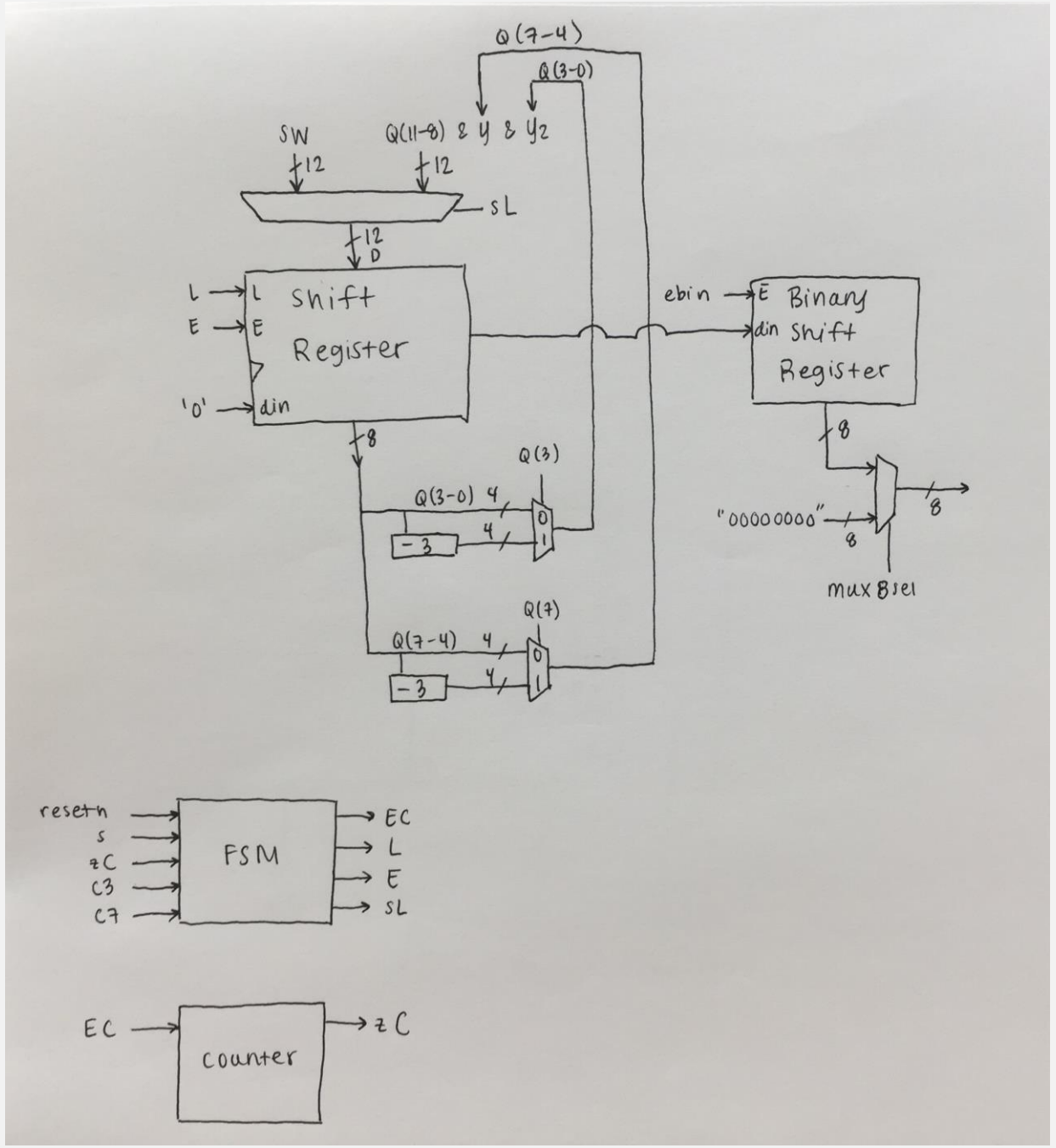
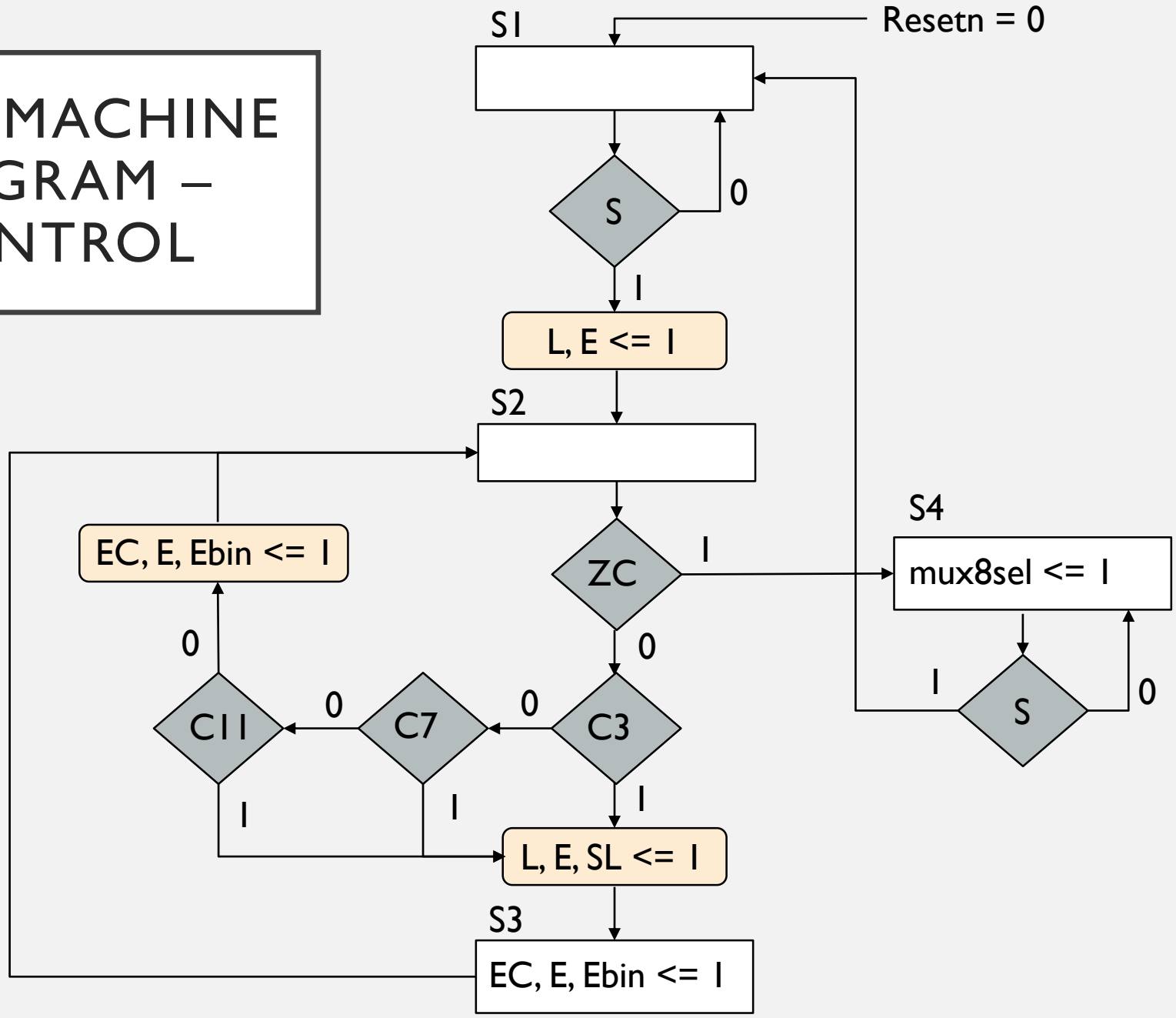
OVERVIEW

- 12 switches were used to input the BCD number into the FPGA, then we used VHDL code to convert the input to binary output which was displayed on the LEDs on the board (on = 1, off = 0).
- Our project uses a state machine, comparator, shift register, counter, subtractor and multiplexors.

BLOCK DIAGRAM- DATAPATH



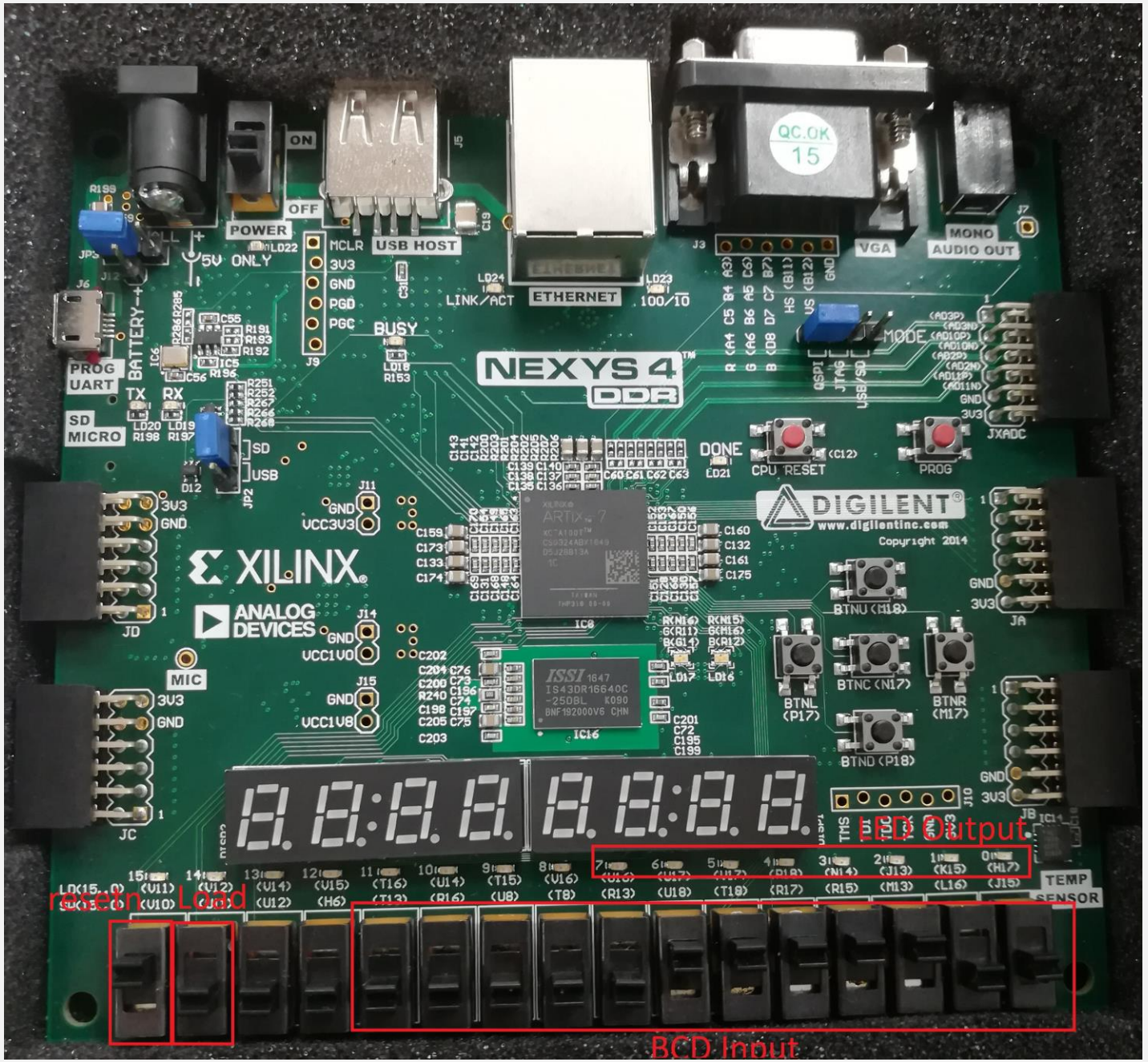
STATE MACHINE DIAGRAM – CONTROL



EXPERIMENTAL SETUP

- Least significant bit of both the output and the input are on the right

- Trial 1: 0000 0001 0111 (17 BCD)
  => 0001 0001 (Binary)
- Trial 2: 0010 0101 0101 (255 BCD)
  => 1111 1111 (Binary)
- Trial 3: 0000 0111 0110 (76 BCD)
  => 0100 1100 (Binary)
- Trial 4: 0001 0011 1001 (139 BCD)
  => 1000 1011 (Binary)
- Trial 5: 0000 0000 1000 (8 BCD)
  => 0000 1000 (Binary)



CONCLUSIONS

- Implementation of Algorithm was more difficult than expected
  - BCD → Binary algorithms seemingly less common than Binary → BCD
  - Double Dabble vs. Reversing Double Dabble
- Utilizing the FSM to control more components simplified the design process
- We would like to implement a serializer to the seven segment display to display the output.