Banner on Seven Segment Displays

With Varying Speeds and Scrolling Messages

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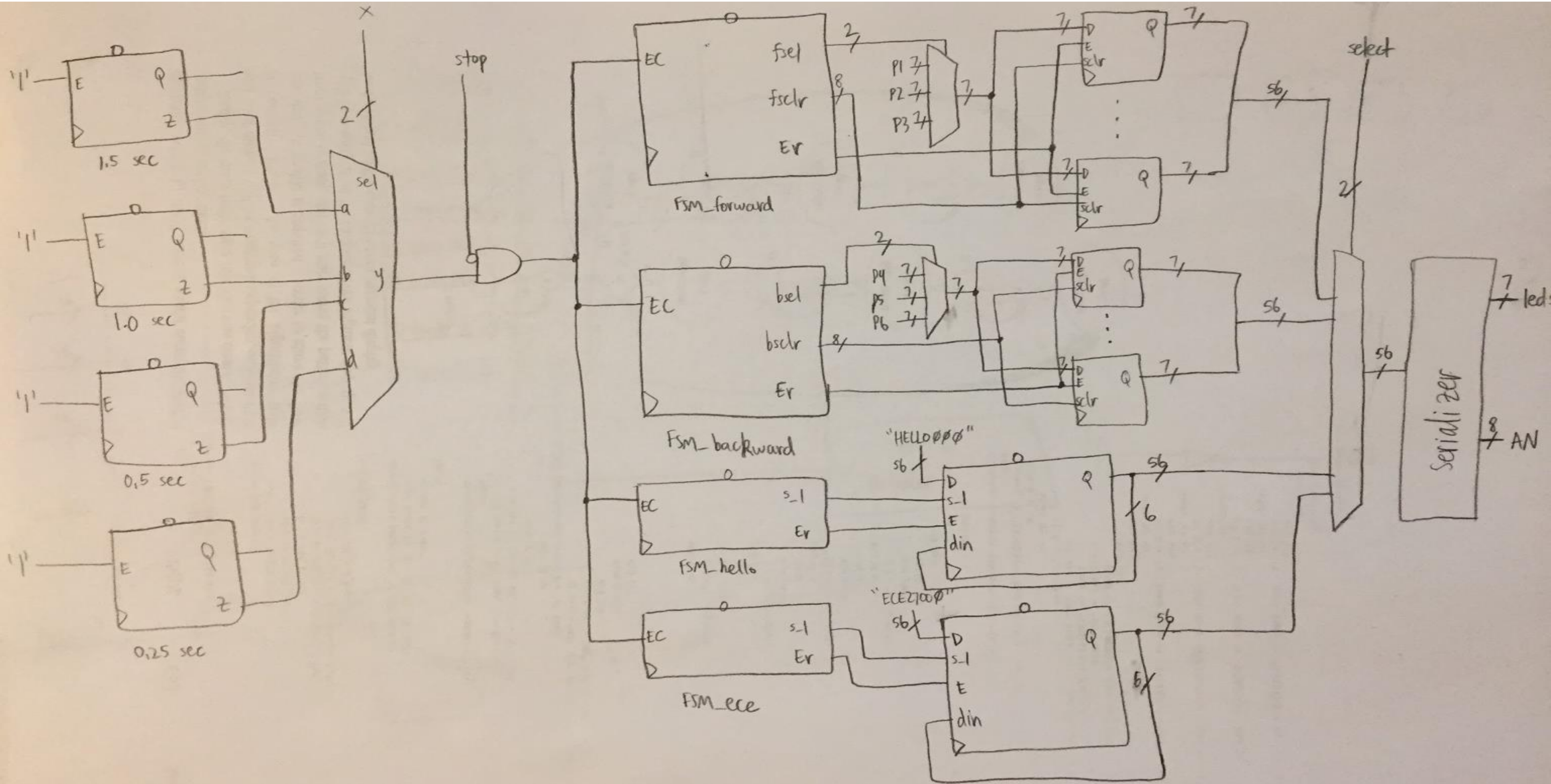
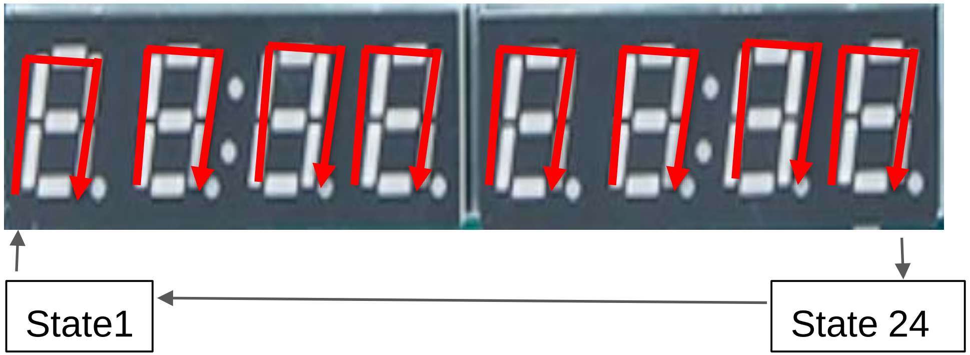
Overview

- Patterns
  - Forward pattern banner
  - Backward pattern banner
  - “HELLO” scrolling message
  - “ECE2700” scrolling message
- Switches
  - Stop
  - One of four speeds
  - One of four patterns

Circuit Overview



FSM_forward

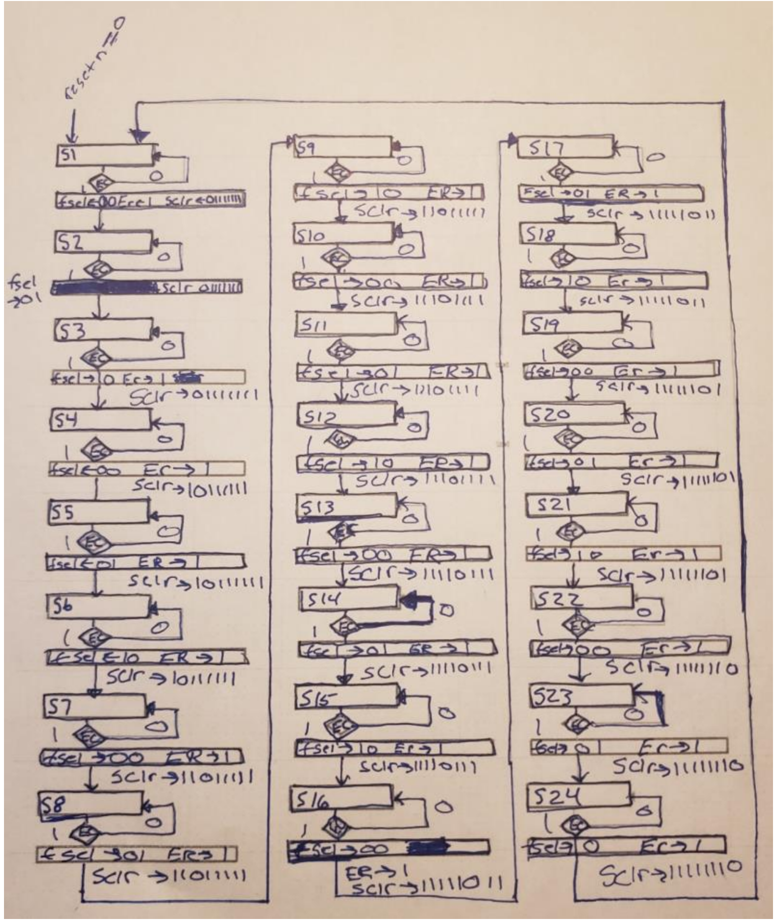


State1

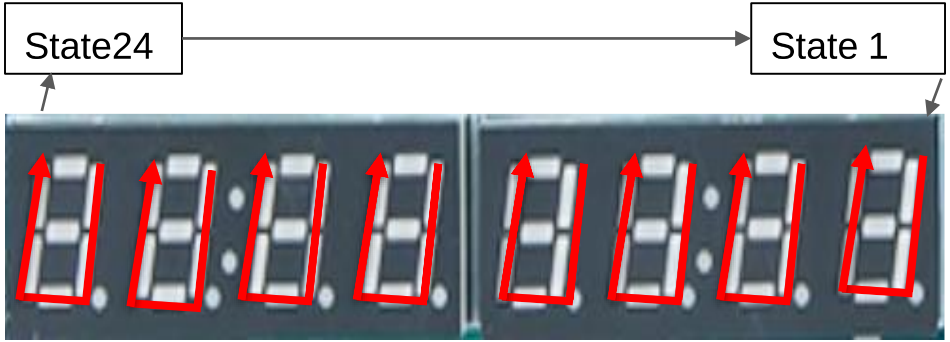
State 24

For each of the eight seven segment displays, there are three different states that illuminate on each anode (active low).

FSEL	**LEDs**
00	0111001
01	0011100
10	0001111



FSM_backward

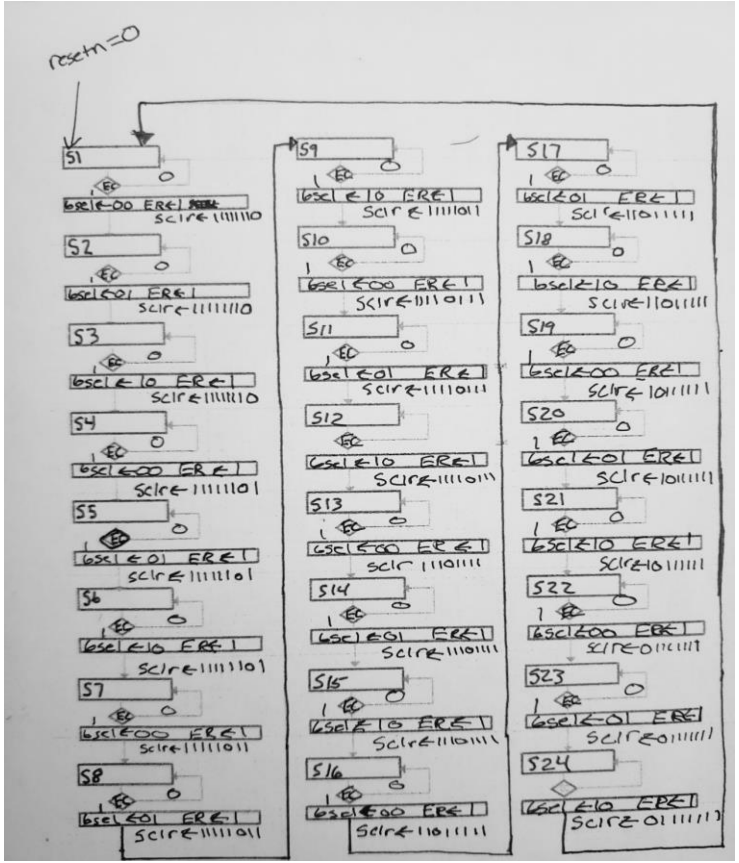


State24

State 1

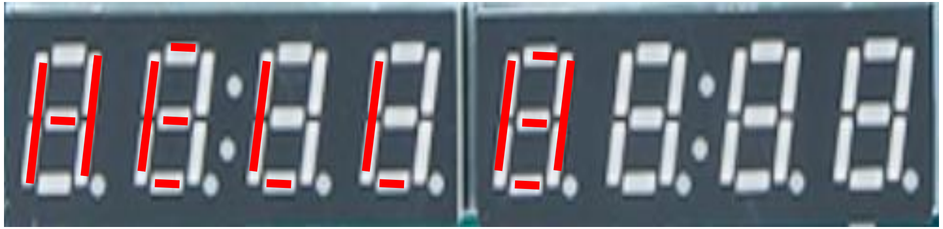
For each of the eight seven segment displays, there are three different states that illuminate on each anode (active low).

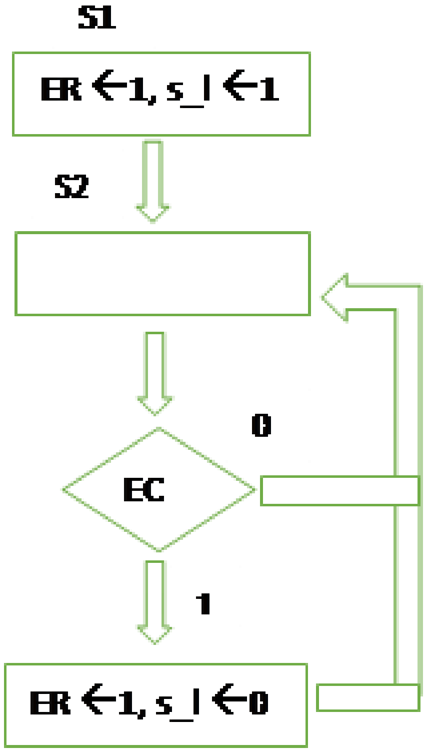
BSEL	**LEDs**
00	1000111
01	1100011
10	1110001



FSM_hello

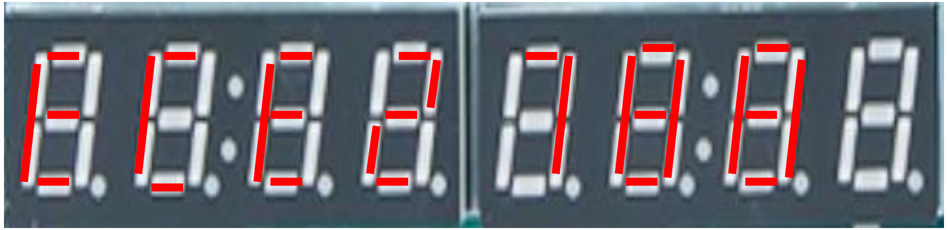
FSM controls a parallel access right shift register to allow the "HELLO" message to flow from AN7 to AN0 and repeat.

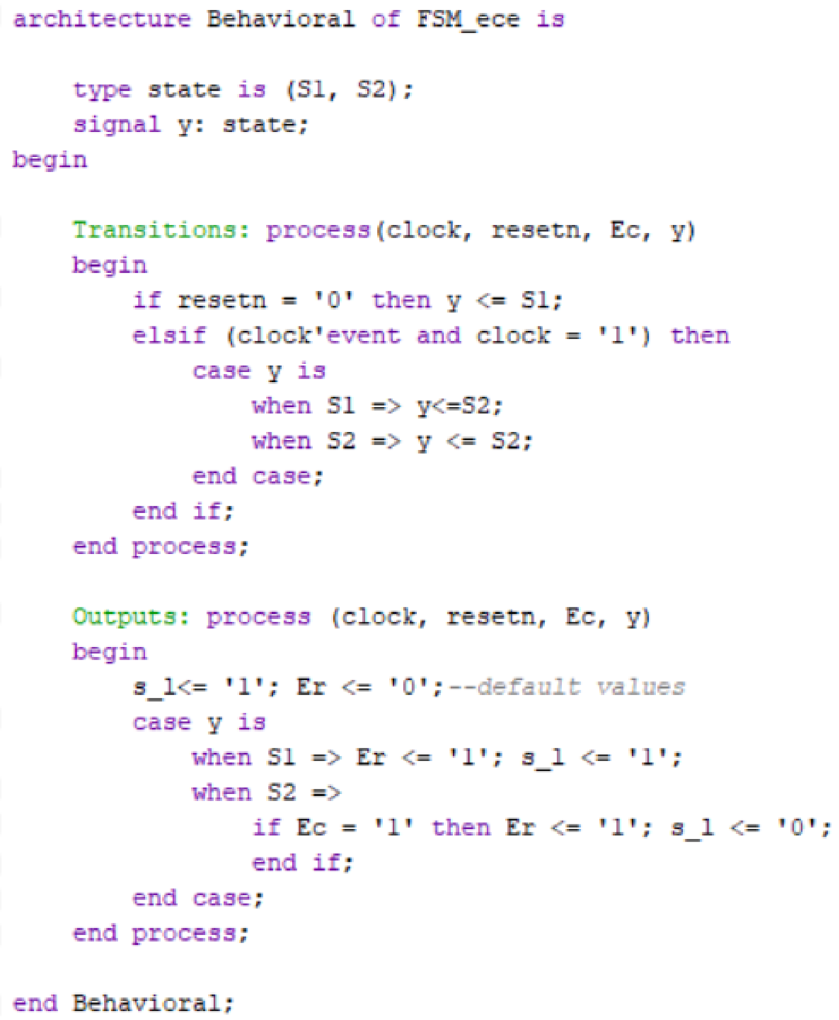




FSM_ece2700

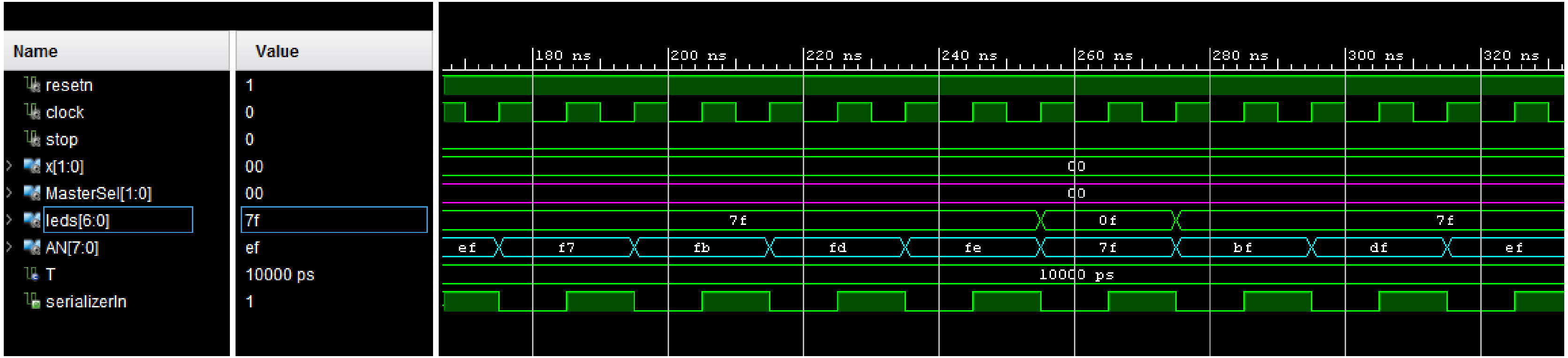
The FSM for “ECE2700” has the same state diagram as that of the FSM for “HELLO.” The transition and outputs processes are displayed.



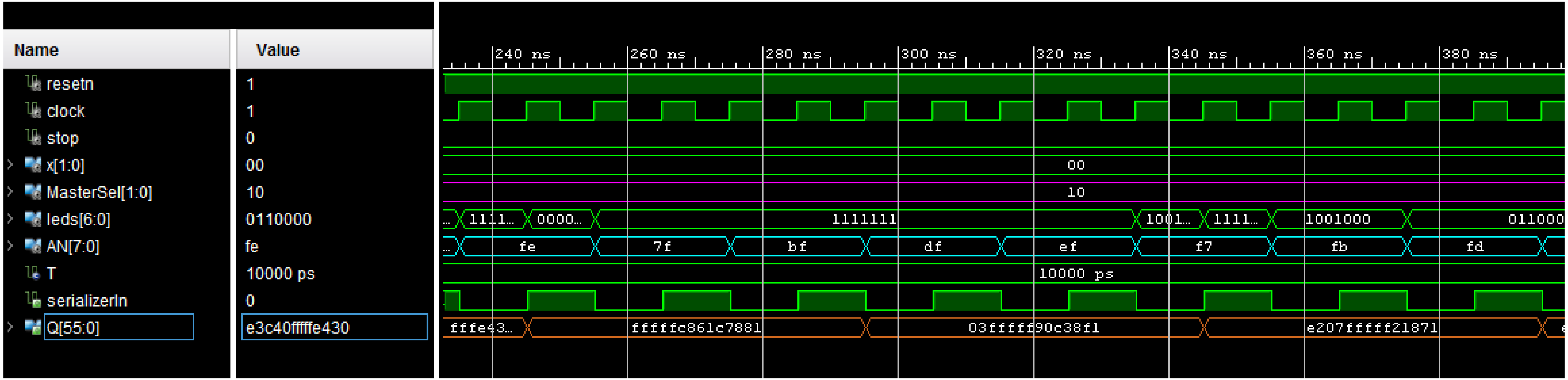


```
architecture Behavioral of FSM_ece is

    type state is (S1, S2);
    signal y: state;
begin

    Transitions: process(clock, resetn, Ec, y)
    begin
        if resetn = '0' then y <= S1;
        elsif (clock'event and clock = '1') then
            case y is
                when S1 => y<=S2;
                when S2 => y <= S2;
            end case;
        end if;
    end process;

    Outputs: process (clock, resetn, Ec, y)
    begin
        s_l<= '1'; Er <= '0';--default values
        case y is
            when S1 => Er <= '1'; s_l <= '1';
            when S2 =>
                if Ec = '1' then Er <= '1'; s_l <= '0';
                end if;
        end case;
    end process;

end Behavioral;
```

Demo



Name	Value
resetn	1
clock	0
stop	0
x[1:0]	00
MasterSel[1:0]	00
leds[6:0]	7f
AN[7:0]	ef
T	10000 ps
serializerIn	1



Name	Value
resetn	1
clock	1
stop	0
x[1:0]	00
MasterSel[1:0]	10
leds[6:0]	0110000
AN[7:0]	fe
T	10000 ps
serializerIn	0
Q[55:0]	e3c40fffffe430

Conclusions

- Four patterns and speed controlled by switches
- Total of 5 FSMs
- Datapath circuit
  - 7-bit registers
  - Shift registers
  - MUXs
  - NOT & AND gates
  - Serializer
    - FSM controlled by 1ms counter
    - Decoder
    - MUX

References

Llamocca, Daniel. “Notes - Unit 7.” *Introductions to Digital Systems Design*, Jan. 2018,pp.12–13.,moodle.oakland.edu/pluginfile.php/4385644/mod_resource/content/5/Notes%20-%20Unit%207.pdf.

Llamocca, Daniel. “Unit 7: Digital System Design.” *VHDL Coding for FPGAs*,slides6-7.,http://www.secs.oakland.edu/~llamocca/Tutorials/VHDLFPGA/Unit%207.pdf

Llamocca, Daniel. “Serializer: Four 7-segment displays.” *VHDL Projects (VHDLfiles,testbench)*,http://www.secs.oakland.edu/~llamocca/Tutorials/VHDLFPGA/ISE/Unit_7/serializer.vhd