ECE 2700 Final Project - Traffic Light Controller

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Overview of Procedure

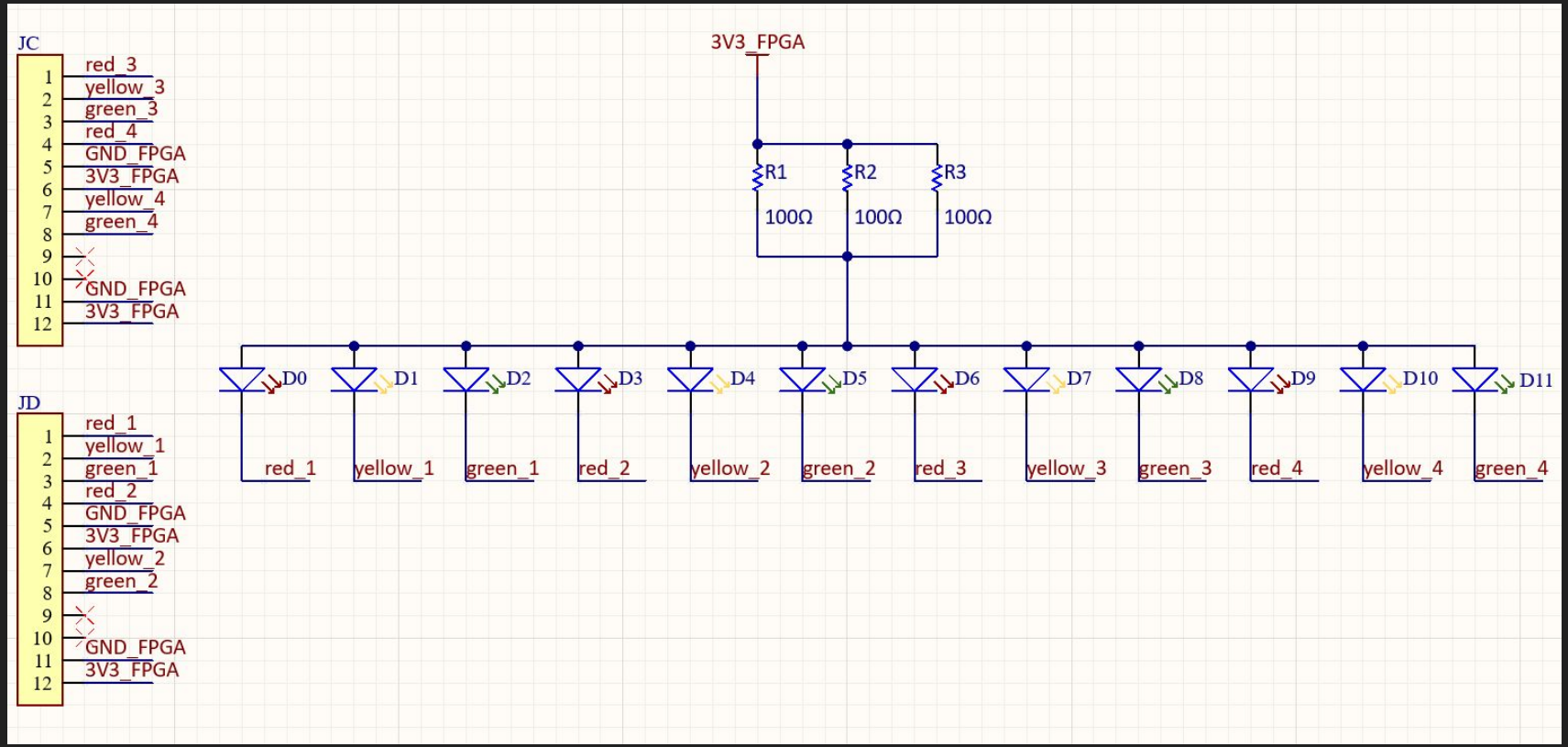
The design of our 4-way Traffic Light Controller consists of using the Vivado software along with the Nexys Artix-7 100T Board, and a circuit built on a breadboard to produce all the results.

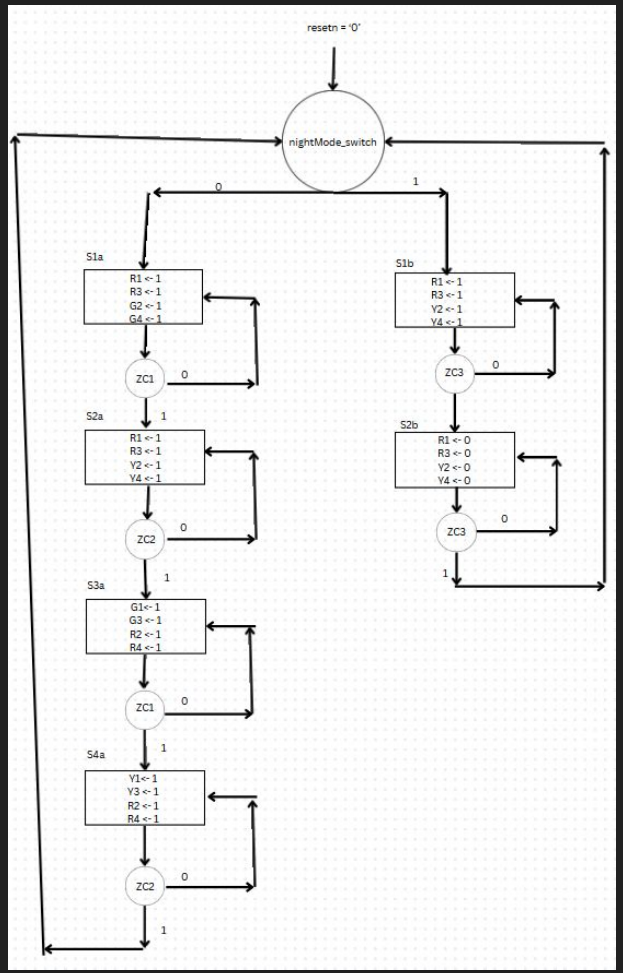
The 4-way Traffic Light Controller has a North/South and East/West group pattern that will share the same light, making 2 separate groups of traffic lights.

When one pair of lights is red, the second pair of lights will run through the cycle with the green and yellow lights until it hits red. Then, the other pair of lights will go through the cycle.

Using the power of a switch, the traffic lights will enter night-mode. The first pair of lights will flash red lights, while the other pair will flash yellow lights.

Electrical Schematic



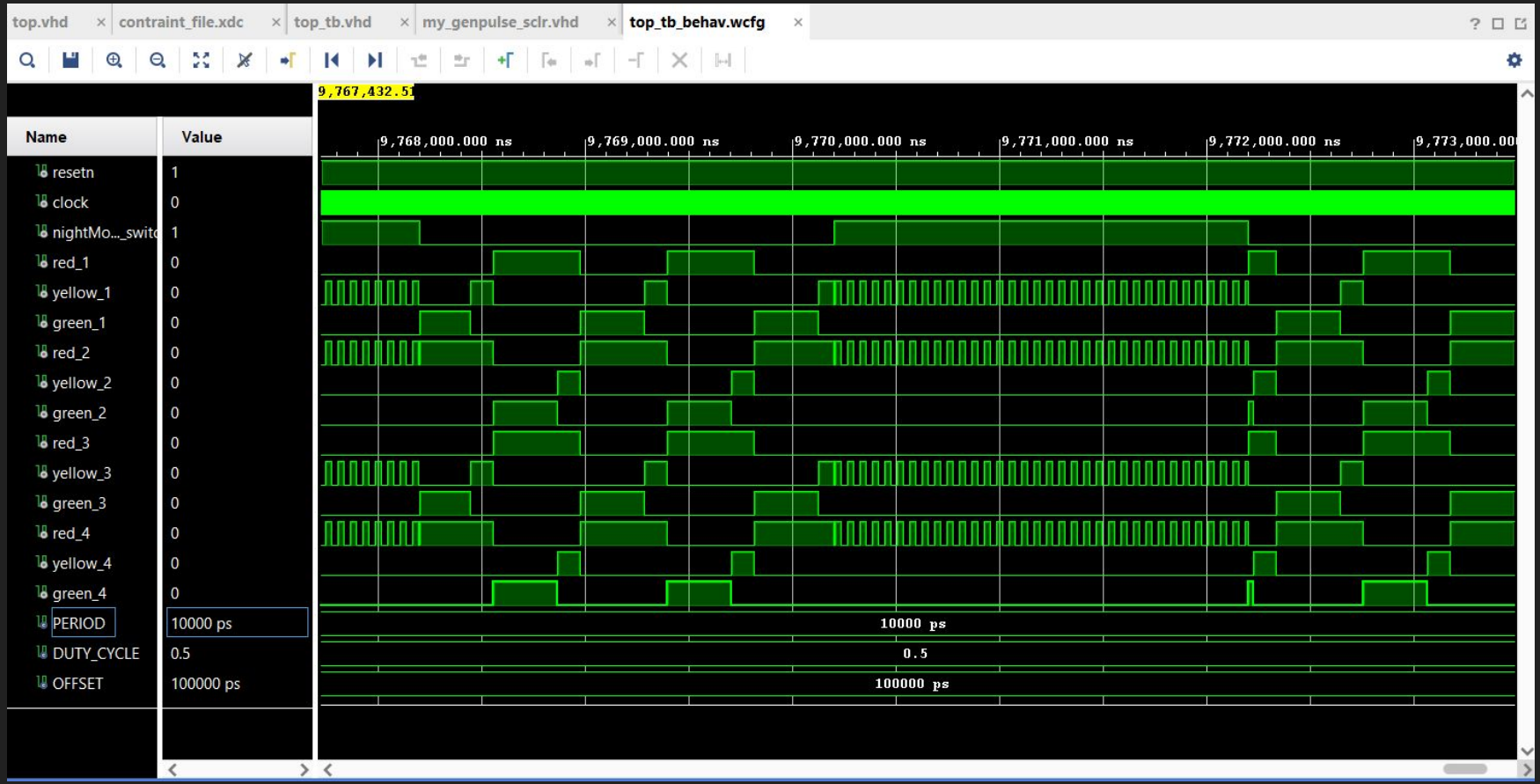


ASM Chart

Outputs: Red[3:0]
Green[3:0]
Yellow[3:0]
Inputs: zC1, zC2

The 2 timers serve as FSM inputs, which output a logic 1 when they have counted to a certain number. Based on the clock rate of the FPGA, counting serves to slow down the clock rate to a realistic time. zC1 is 3 seconds while zC2 is 1 second. The traffic lights are cyclical and flow from one state to the next based on how much time has passed. Night mode is toggled with a simple onboard switch.

Simulation


top.vhd
contraint_file.xdc
top_tb.vhd
my_genpulse_sclr.vhd
top_tb_behav.wcfg
9,767,432.51
Name
Value
resetn
1
clock
0
nightMo..._switc
1
red_1
0
yellow_1
0
green_1
0
red_2
0
yellow_2
0
green_2
0
red_3
0
yellow_3
0
green_3
0
red_4
0
yellow_4
0
green_4
0
PERIOD
10000 ps
DUTY_CYCLE
0.5
OFFSET
100000 ps
9,768,000.000 ns
9,769,000.000 ns
9,770,000.000 ns
9,771,000.000 ns
9,772,000.000 ns
9,773,000.00
10000 ps
0.5
100000 ps

Block Diagram