5 DIGIT LOCK SAFE

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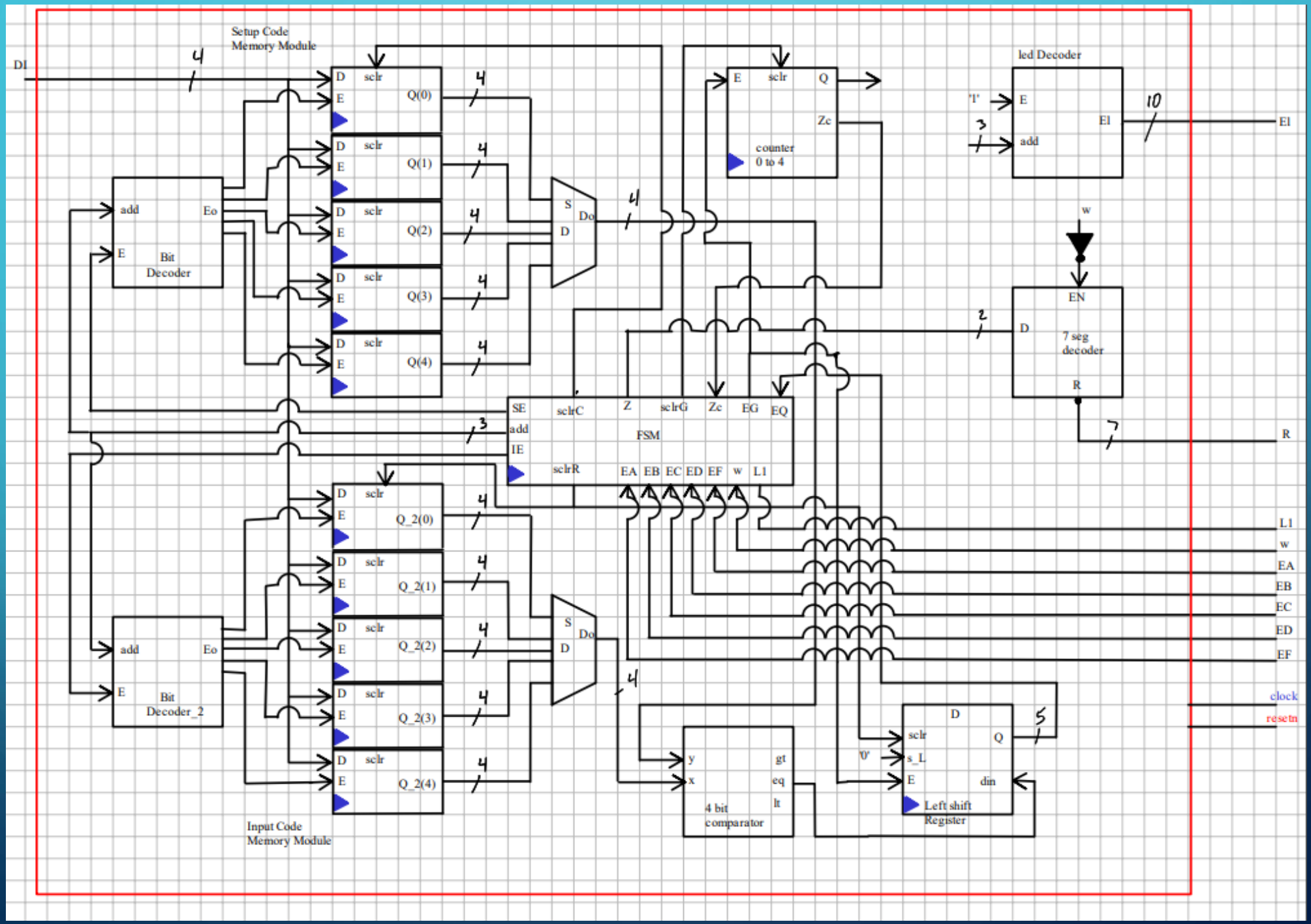
OUR CIRCUIT & SPECS

- The circuit created here can store a 5 digit 4 bit integer in 5 separate register locations that are combined into one RAM module.
- After the code is stored the circuit will display either a U on the 7 segment display if the correct code is input, or an E if the incorrect code is input.
- One of the RGB LEDs also displays green or red depending on if the correct code is input.

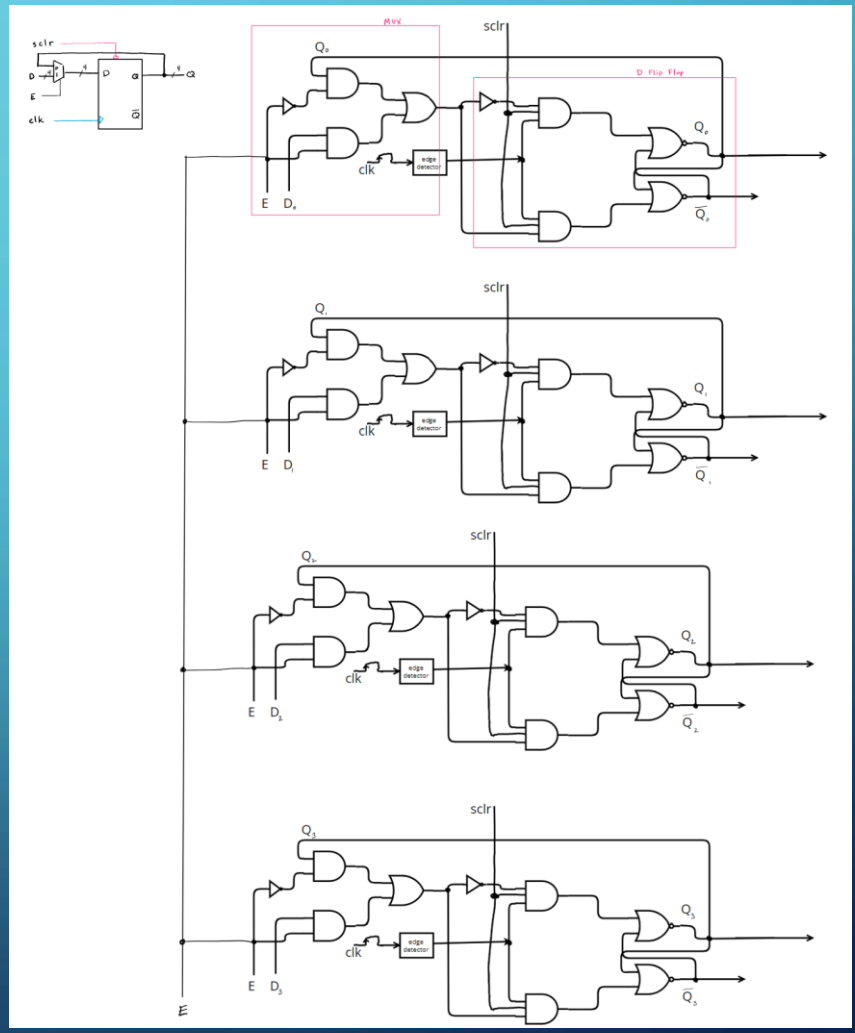
COMPONENTS

- Decoders x 3
- FSM
- 5 Location 4 bit RAM Modules x 2
- Multiplexer x 3
- 7-SEG Decoder
- Left Shift Register
- 4 Bit Comparator


Setup Code
Memory Module
DI
4
D
E
sclr
Q(0)
Q(1)
Q(2)
Q(3)
Q(4)
add
Eo
Bit
Decoder
S
D
Do
counter
0 to 4
Zc
led Decoder
'1'
3
10
El
w
EN
7 seg
decoder
R
2
7
SE
add
IE
sclrC
sclrG
sclrR
Z
EG
EQ
FSM
EA
EB
EC
ED
EF
L1
Q_2(0)
Q_2(1)
Q_2(2)
Q_2(3)
Q_2(4)
Bit
Decoder_2
Input Code
Memory Module
y
x
gt
eq
lt
4 bit
comparator
'0'
s_L
din
Left shift
Register
5
clock
resetn

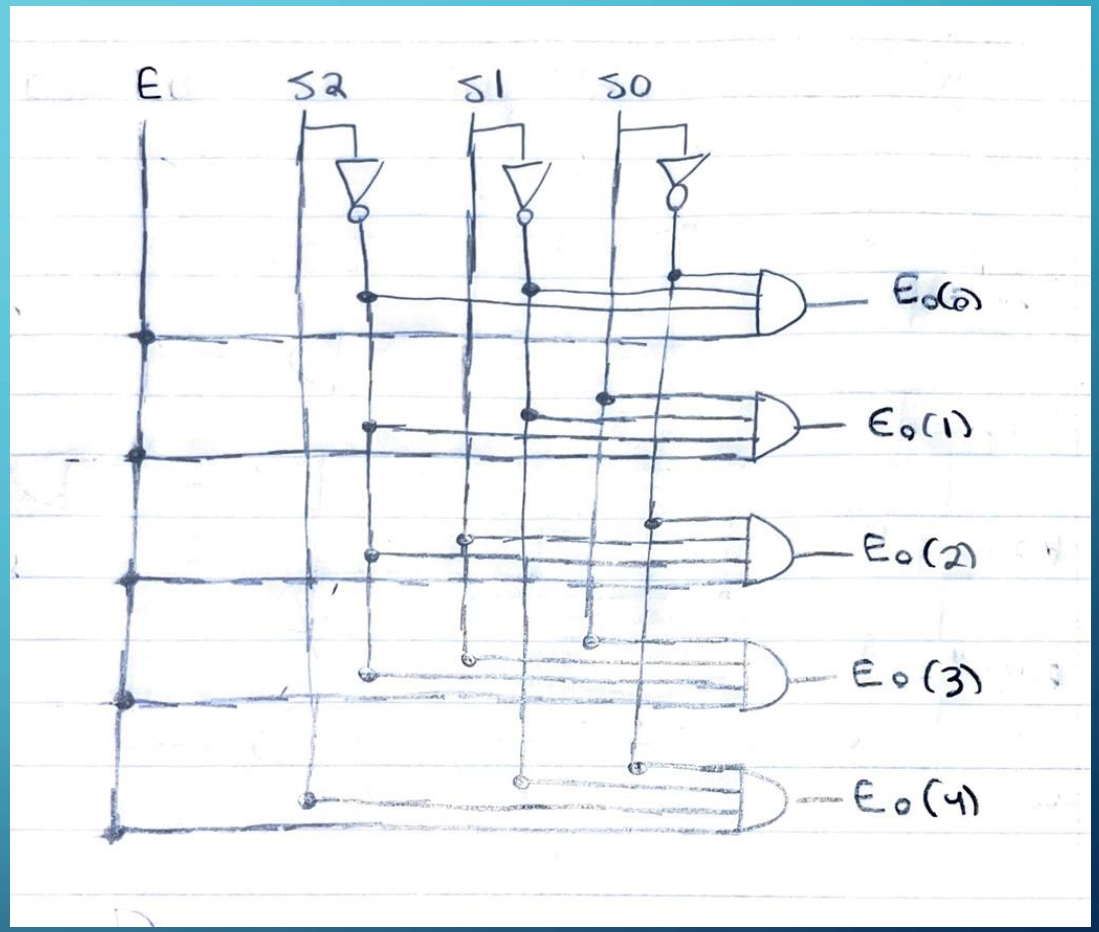
5 LOCATION 4 BIT RAM MODULES

- Inputs:
  - D (4 bits) DATA IN
  - E
  - Resetn
  - Sclr
  - clock
- Outputs:
  - Q(n)



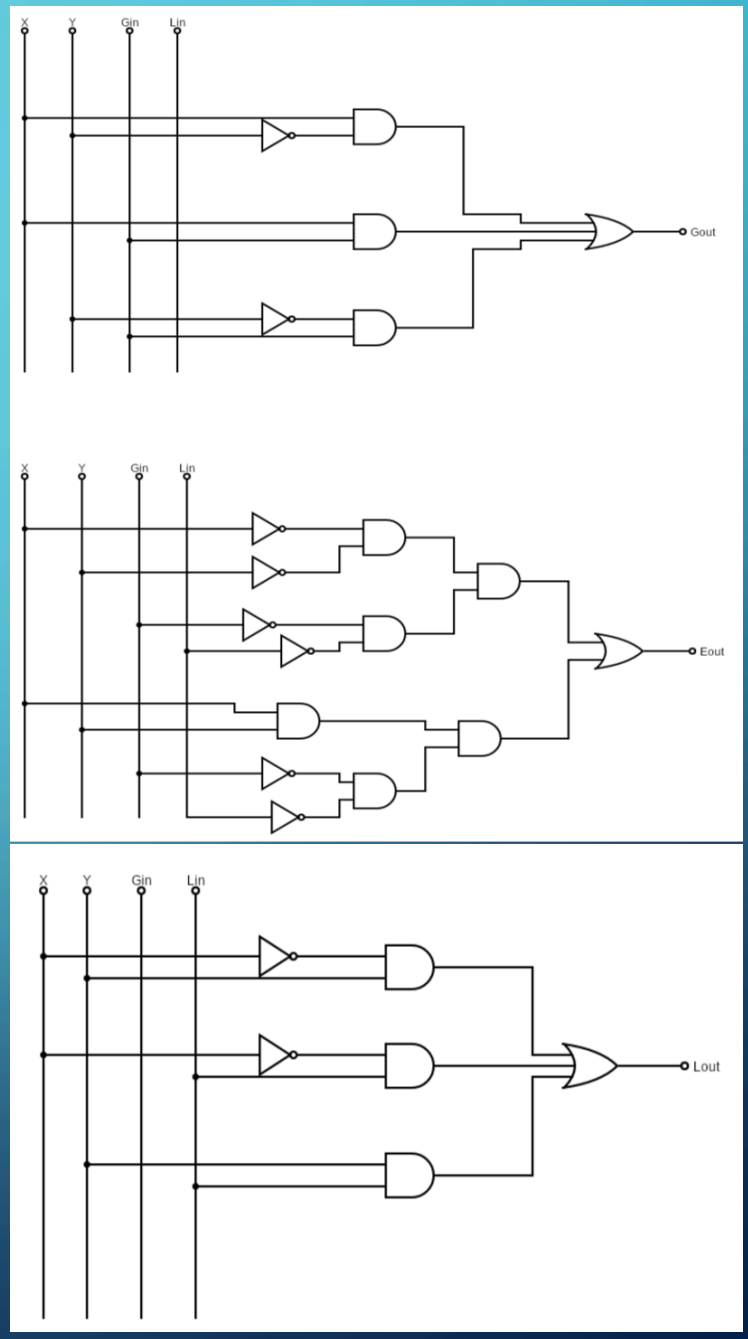
DECODER

- Inputs:
  - Add (3 bits)
  - E (w)
- Outputs:
  - Eo (input E for register enable, 5 bits)



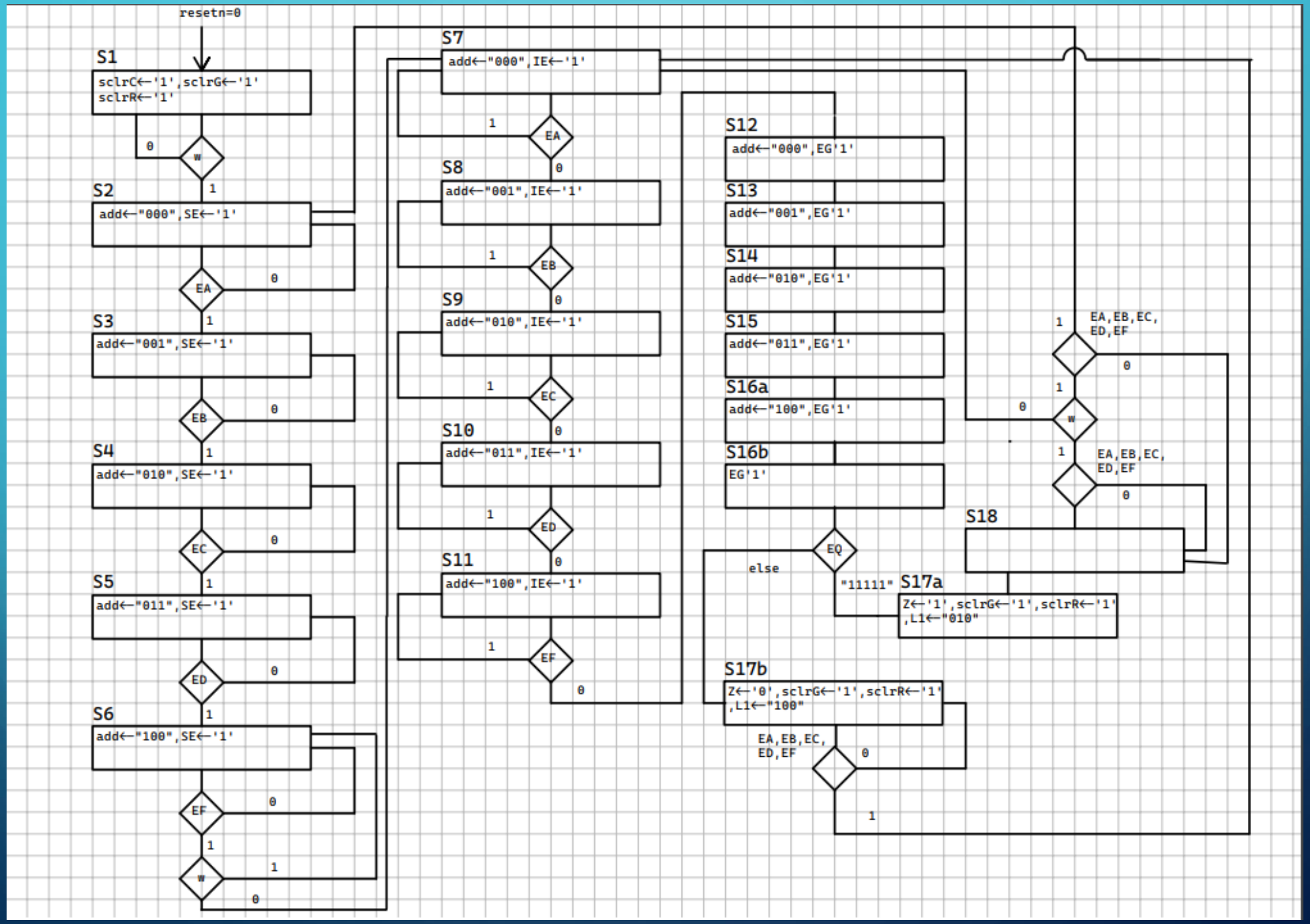
4 BIT COMPARATOR

- Inputs:
  - X (Combination Code)
  - Y (Unlocking Code)
  - Gin, Lin
- Outputs:
  - Gout, Lout
  - Eout (indicates matching code)



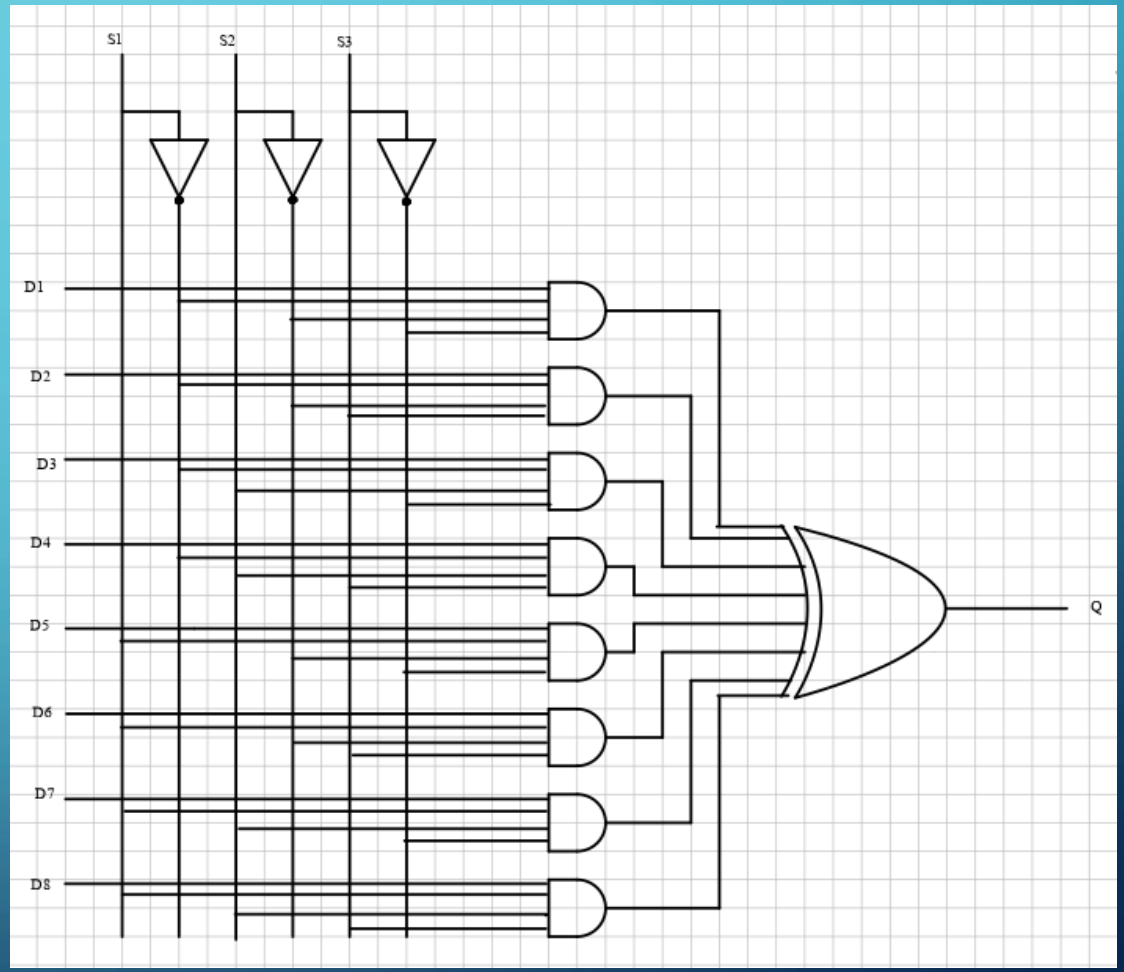
FSM

- Inputs:
  - clock
  - W
  - EA, EB, EC, ED, EF
  - EQ (5 bits)
  - Zc
- Outputs:
  - add (3 bits, becomes add for decoder)
  - sclrC, sclrG, sclrR
  - IE, SE
  - Z
  - L1


resetn=0
S1
sclrC←'1',sclrG←'1'
sclrR←'1'
0
W
1
S2
add←"000",SE←'1'
EA
0
1
S3
add←"001",SE←'1'
EB
0
1
S4
add←"010",SE←'1'
EC
0
1
S5
add←"011",SE←'1'
ED
0
1
S6
add←"100",SE←'1'
EF
0
1
W
1
0
S7
add←"000",IE←'1'
1
EA
0
S8
add←"001",IE←'1'
1
EB
0
S9
add←"010",IE←'1'
1
EC
0
S10
add←"011",IE←'1'
1
ED
0
S11
add←"100",IE←'1'
1
EF
0
S12
add←"000",EG'1'
S13
add←"001",EG'1'
S14
add←"010",EG'1'
S15
add←"011",EG'1'
S16a
add←"100",EG'1'
S16b
EG'1'
EQ
else
"11111"
S17a
Z←'1',sclrG←'1',sclrR←'1'
,L1←"010"
S17b
Z←'0',sclrG←'1',sclrR←'1'
,L1←"100"
EA,EB,EC,
ED,EF
0
1
S18
1
EA,EB,EC,
ED,EF
0
1
W
0
1
EA,EB,EC,
ED,EF
0

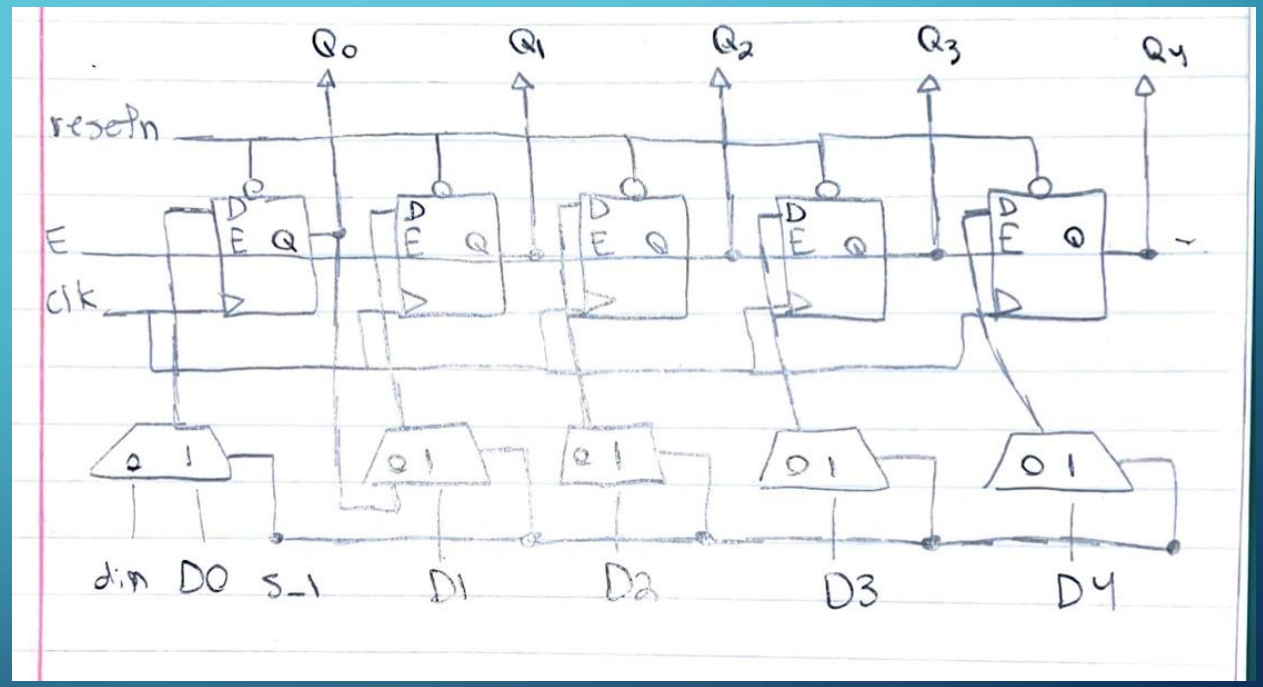
MULTIPLEXER

- Inputs:
  - E (AKA W)
  - D (from Q(n) from register)
- Outputs:
  - Q



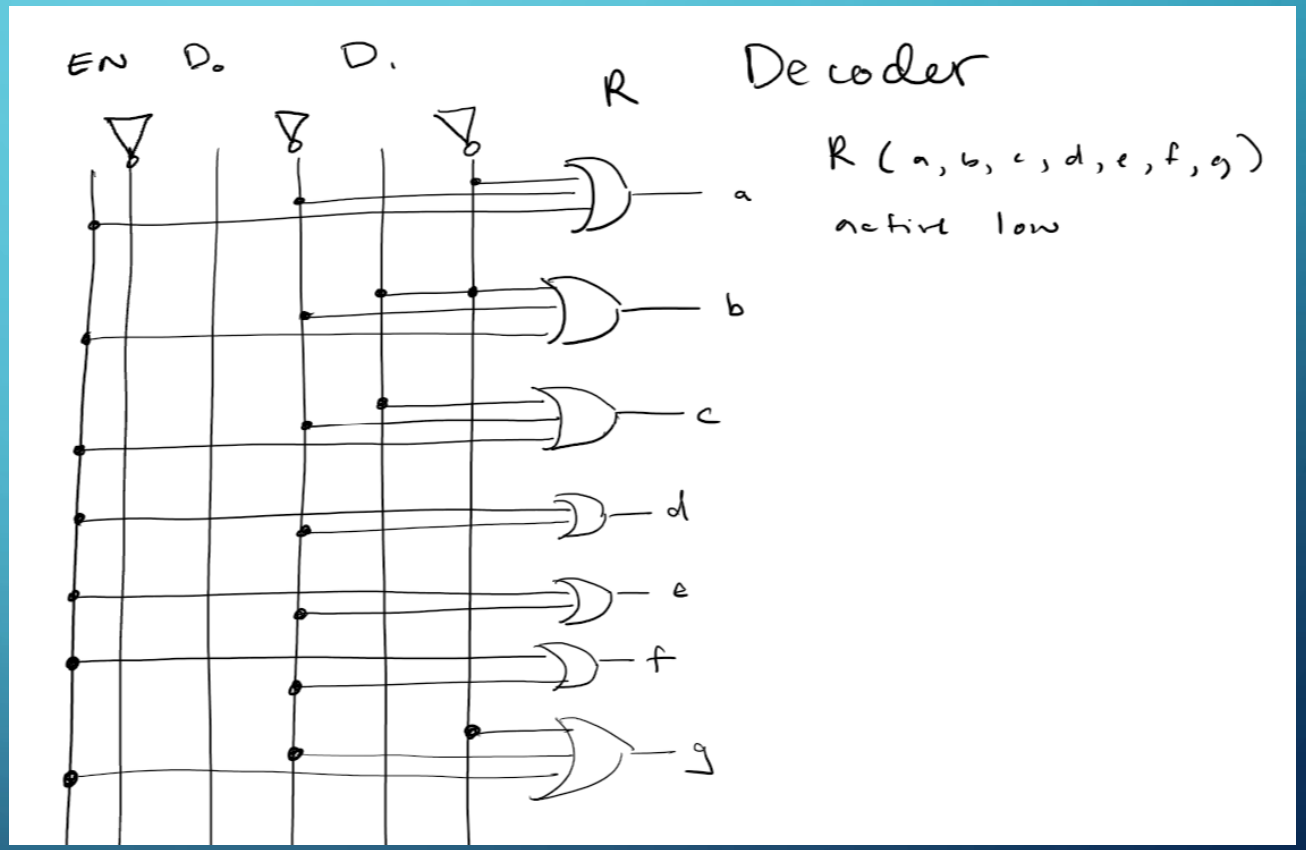
LEFT SHIFT REGISTER

- Inputs:
  - Clock
  - Resetn
  - Din, E, sclr, s_l
  - D
- Outputs:
  - Qpss
  - Shiftout

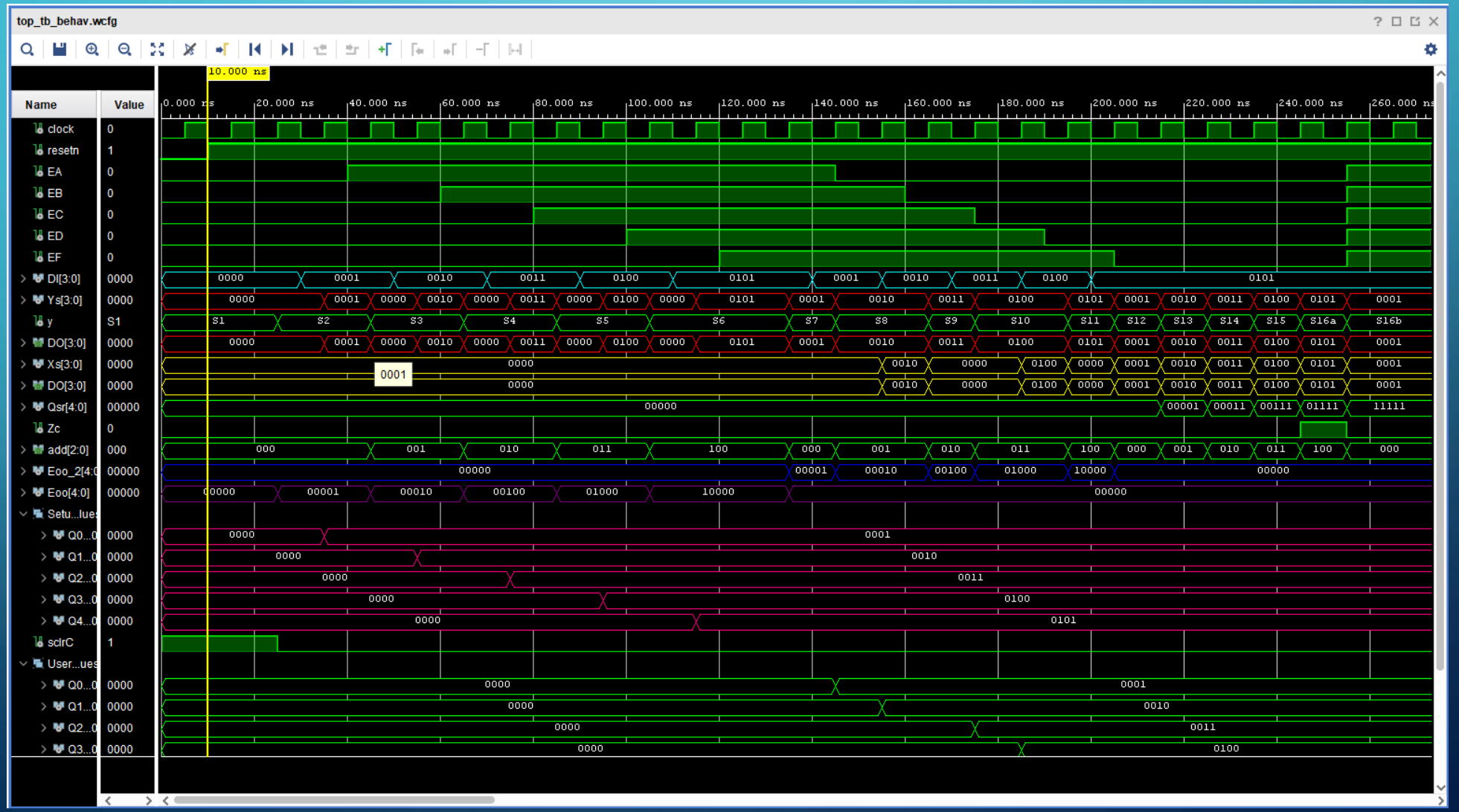


7 SEG DECODER

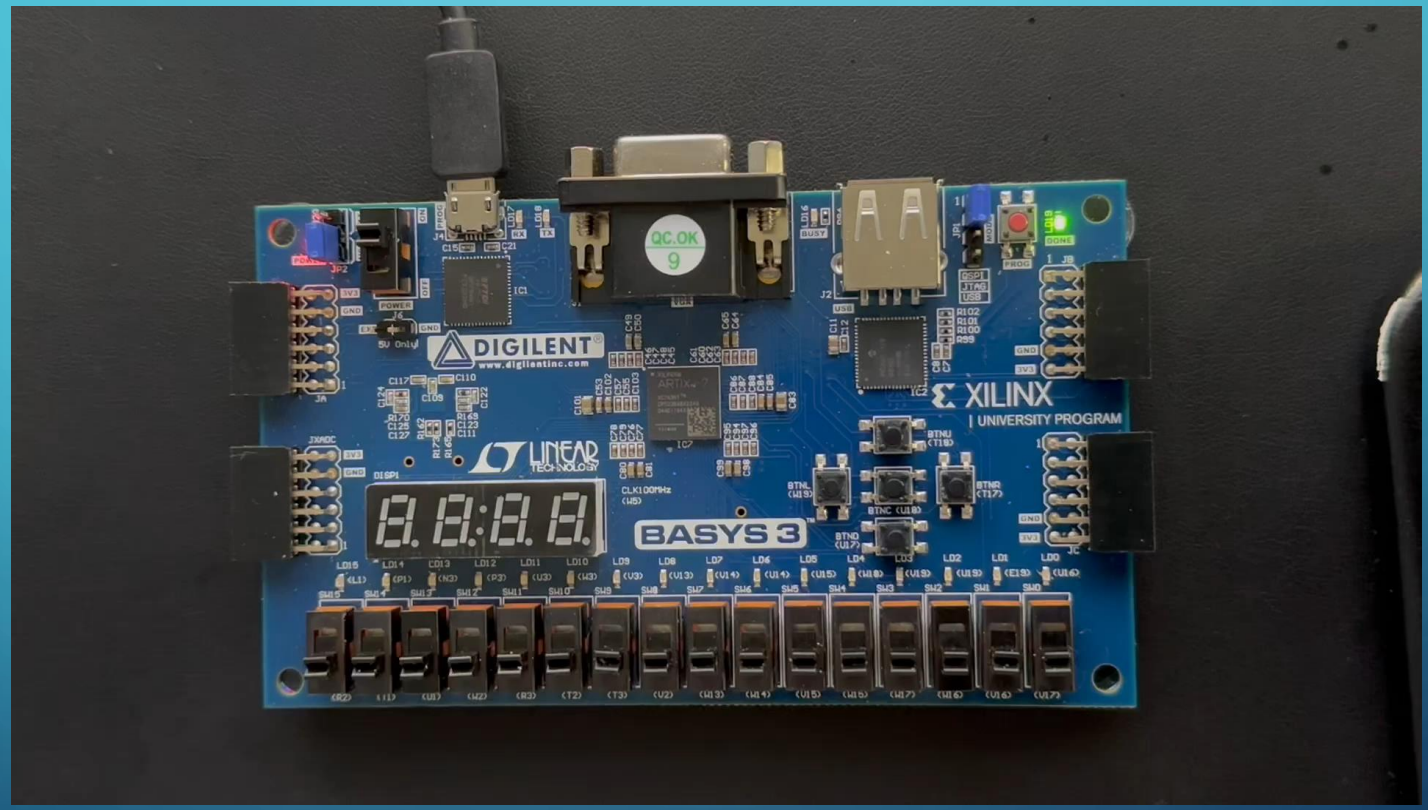
- Inputs:
  - EN (Not w)
  - D
- Outputs:
  - R



SIMULATION


top_tb_behav.wcfg
10.000 ns
Name
Value
clock
resetn
EA
EB
EC
ED
EF
DI[3:0]
Ys[3:0]
y
DO[3:0]
Xs[3:0]
DO[3:0]
Qsr[4:0]
Zc
add[2:0]
Eoo_2[4:0
Eoo[4:0]
Setu...lues
Q0...0
Q1...0
Q2...0
Q3...0
Q4...0
sclrC
User...ues
Q0...0
Q1...0
Q2...0
Q3...0
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
240.000 ns
260.000 ns
0001

DEMO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