4 Way Traffic Light

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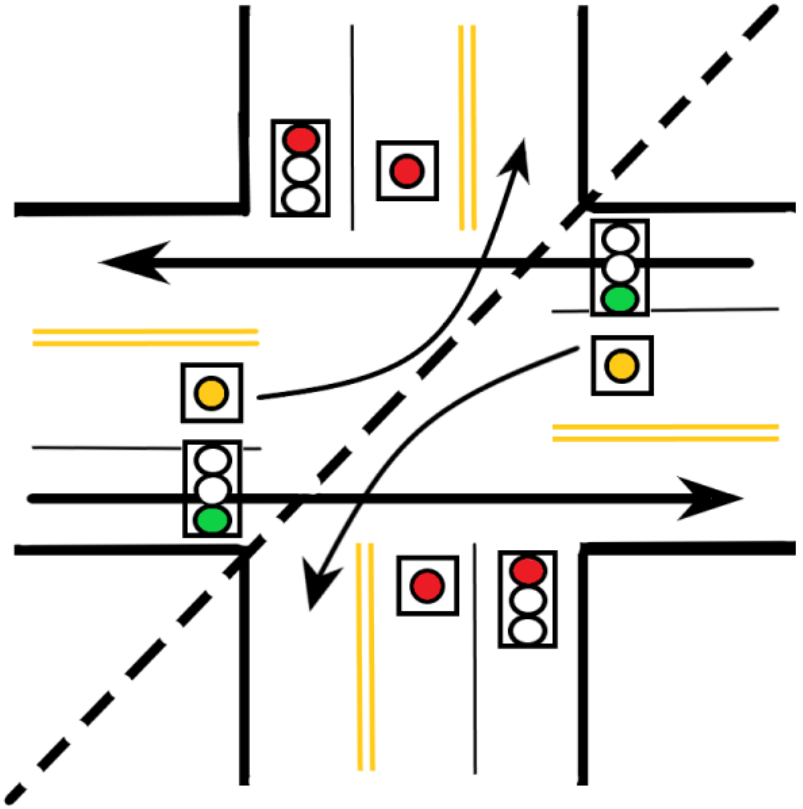
Circuit Description

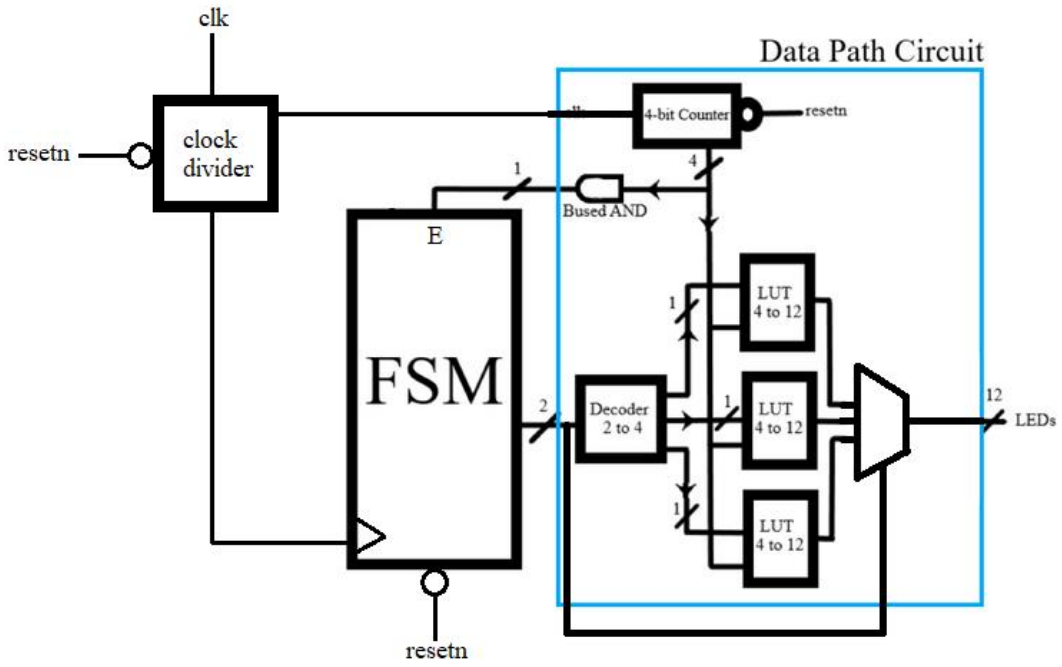
- The circuit can command a four–way intersection and is able to direct a left turn lane
- The design cycle between Red , Green and Yellow in total of 30 seconds
- The design includes 3 phase of operations: **Normal** , **Rush hour** and **Night time** that can be selected by either a timed input or physical switches

•**Circuit Components:**
  - FSM machine
  - A binary counter
  - A decoder
  - LUTs



Block Diagram

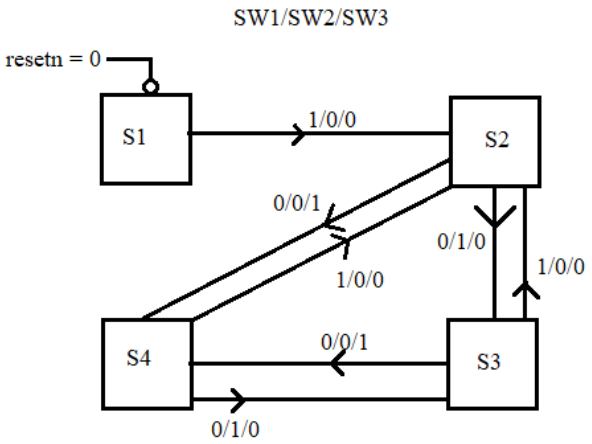
- Clock Divider controls clock cycle of FSM and 4-bit counter
- 4-bit Counter drives LUT's and FSM States
- FSM controls Decoder outputs
- Decoder controls LUT enables
- Multiplexer controls which LUT is outputted to the LEDs



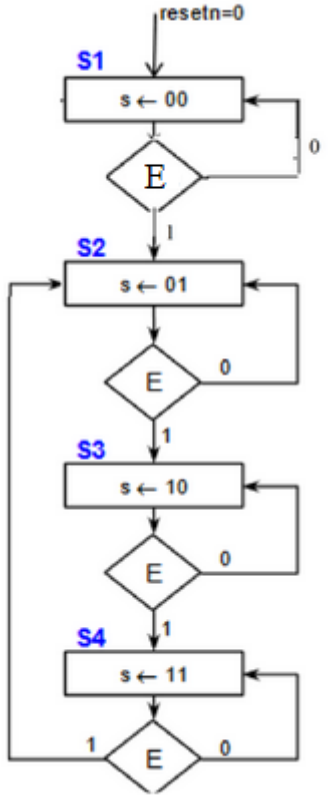
FSM

- FSM by default uses a timed enable input to select states, but if a physical switch is enabled then the switch will be used instead to determine states
- State 1 occurs when the reset switch is activated in any state
- State 2 occurs when the counter outputs “1111” in State 1 or Switch 1 is on
- State 2 also occurs when the counter outputs “1111” in State 4
- State 3 occurs when the counter outputs “1111” in State 2 or Switch 2 is on
- State 4 occurs when the counter outputs “1111” in State 3 or Switch 3 is on

Switches enabled

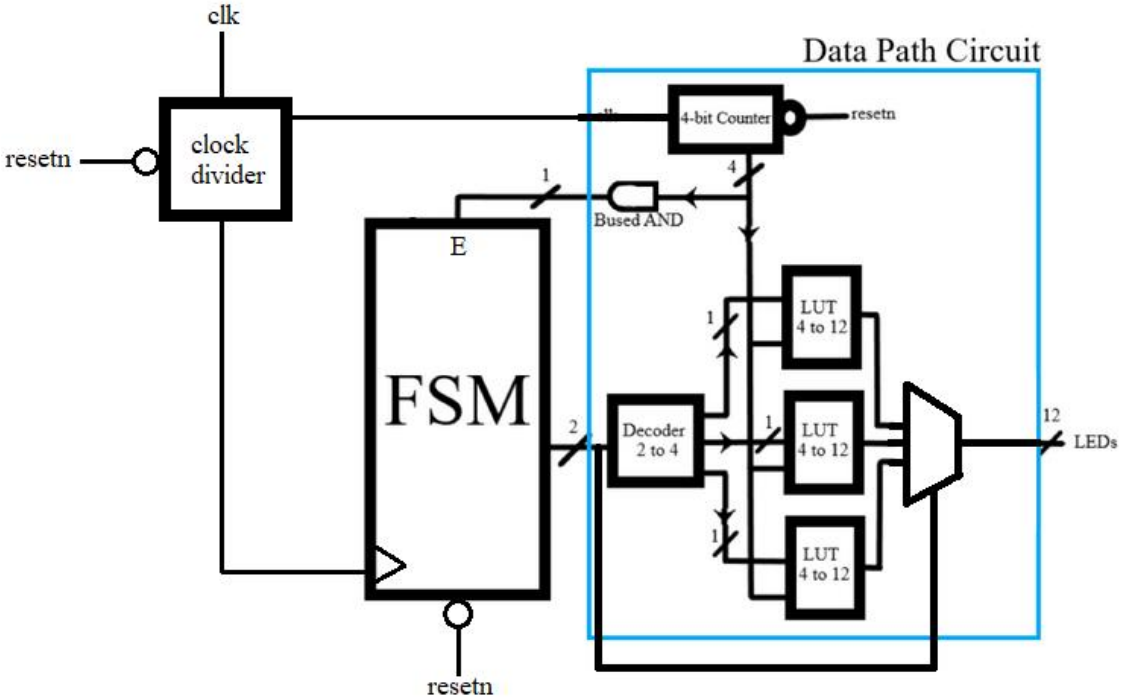


No switches enabled

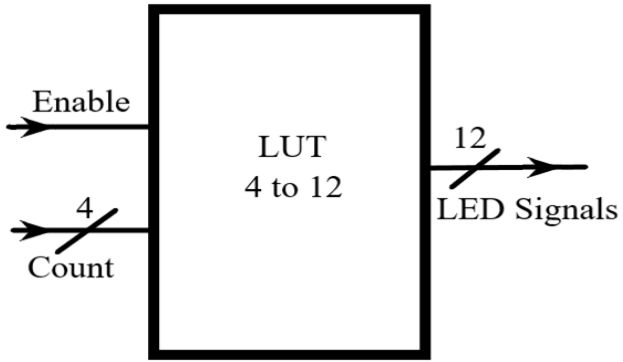


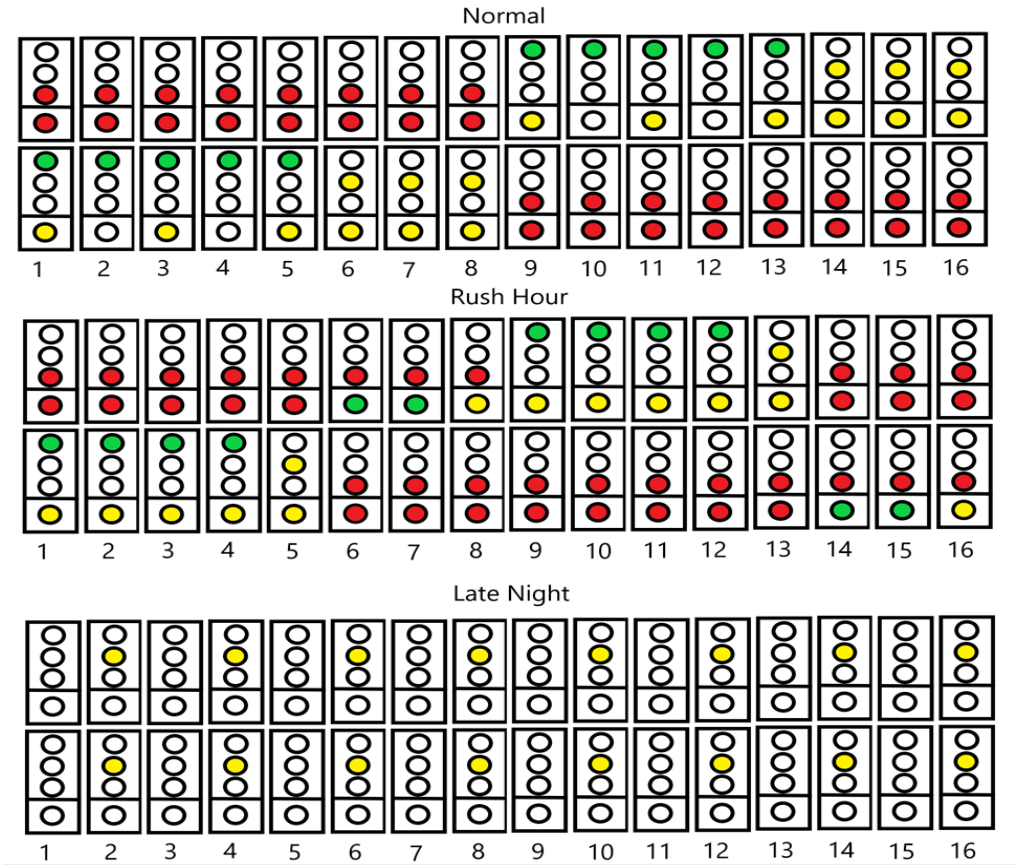
Counter

- Output increases by “0001” per clock divider tick
- Count is reset to “0000” when Resetn is ‘0’
- Count signal cycles through LUT addresses
- Count signal also used to cycle through States



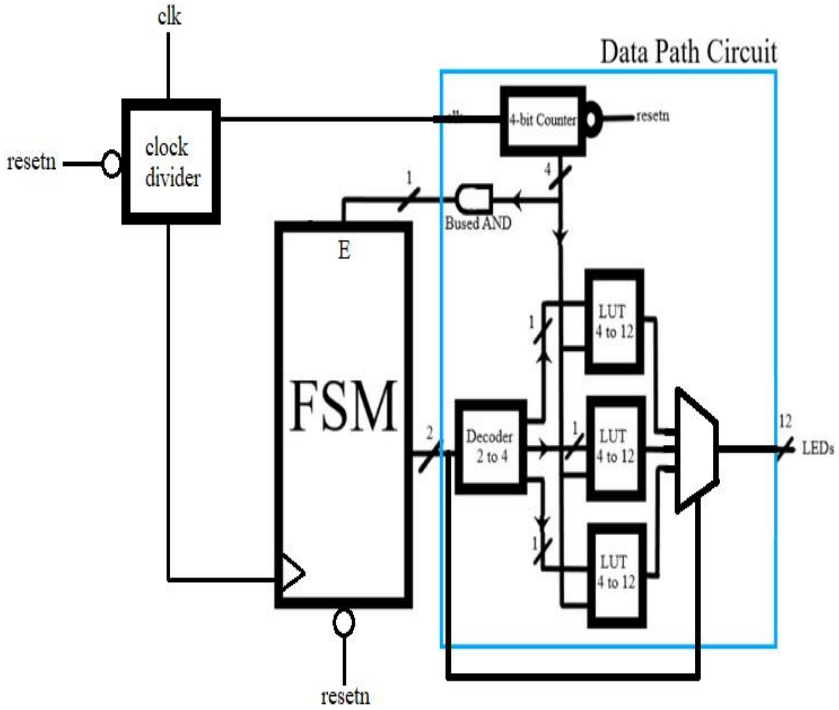
LUT’s


Enable
4
Count
LUT
4 to 12
12
LED Signals


Normal
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Rush Hour
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Late Night
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

Decoder

- Decoders are circuits that transform the inputs into outputs following a certain rule, provided that the number of outputs is greater than or equal to the number of inputs.
- These decoders have n inputs and 2^ n outputs.
- We show: a 2-to-4 decoder. The output yi(y4 y3 y2 y1) is activated when the decimal value of the input w is equal to i.



Circuit Demo

https://youtu.be/IXaIUCt0joY