ECE 2700 Final Project

By: Foster Caragay, Marko Wassef, Vincent Tran, Athanathios Bebawy

What is it?

Our circuit resembles the logic of digital safes. A combination is set, and to unlock the system the same combination must be entered.

The option to reset the combination is available if the system is unlocked, or the system can be relocked. This option is selected by the select switch.

The combination is selected by putting a switch high (with an assigned decimal value) and selecting the “next” button. As the 4 digit combination is entered the 7-segment display will show what digit in the combination you are setting. Ex; if you are setting the third digit of the combination, the 7-segment will show a 3.

Once a combination has been set, the system awaits an input from the user. The input process for unlocking the system is the same as that used to set the combination.

Upon entering the correct combination, the system will illuminate led0 and display a U on the 7 segment display.

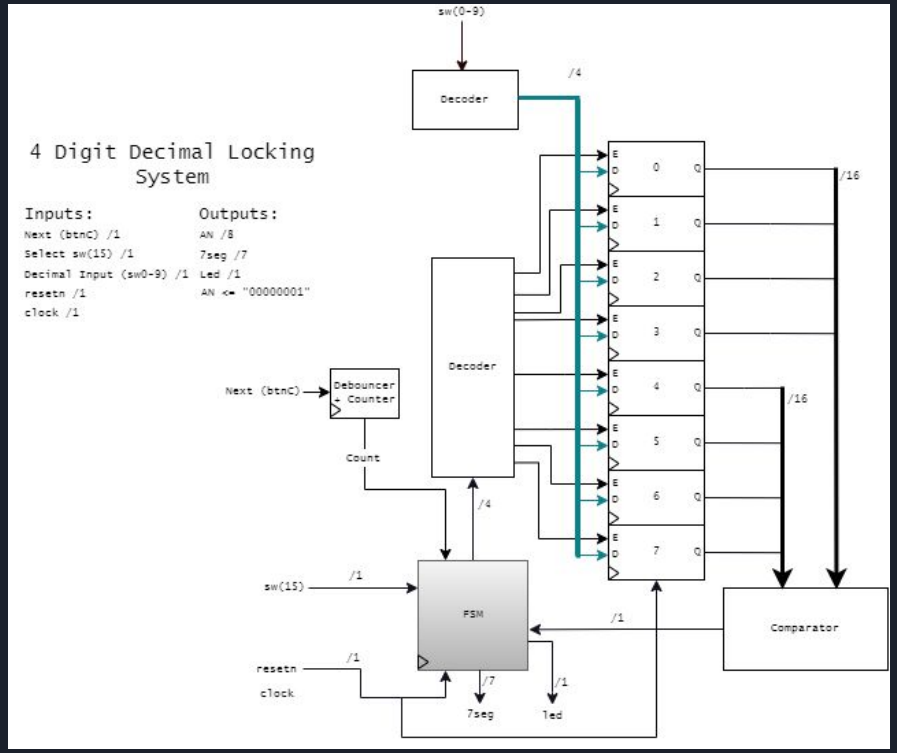
If the wrong combination is entered, the system will display an E and at the next button press, allow you to try again.

The input values are selected by sw0-9
The next button is assigned to btnC
The function select switch is assigned to sw15

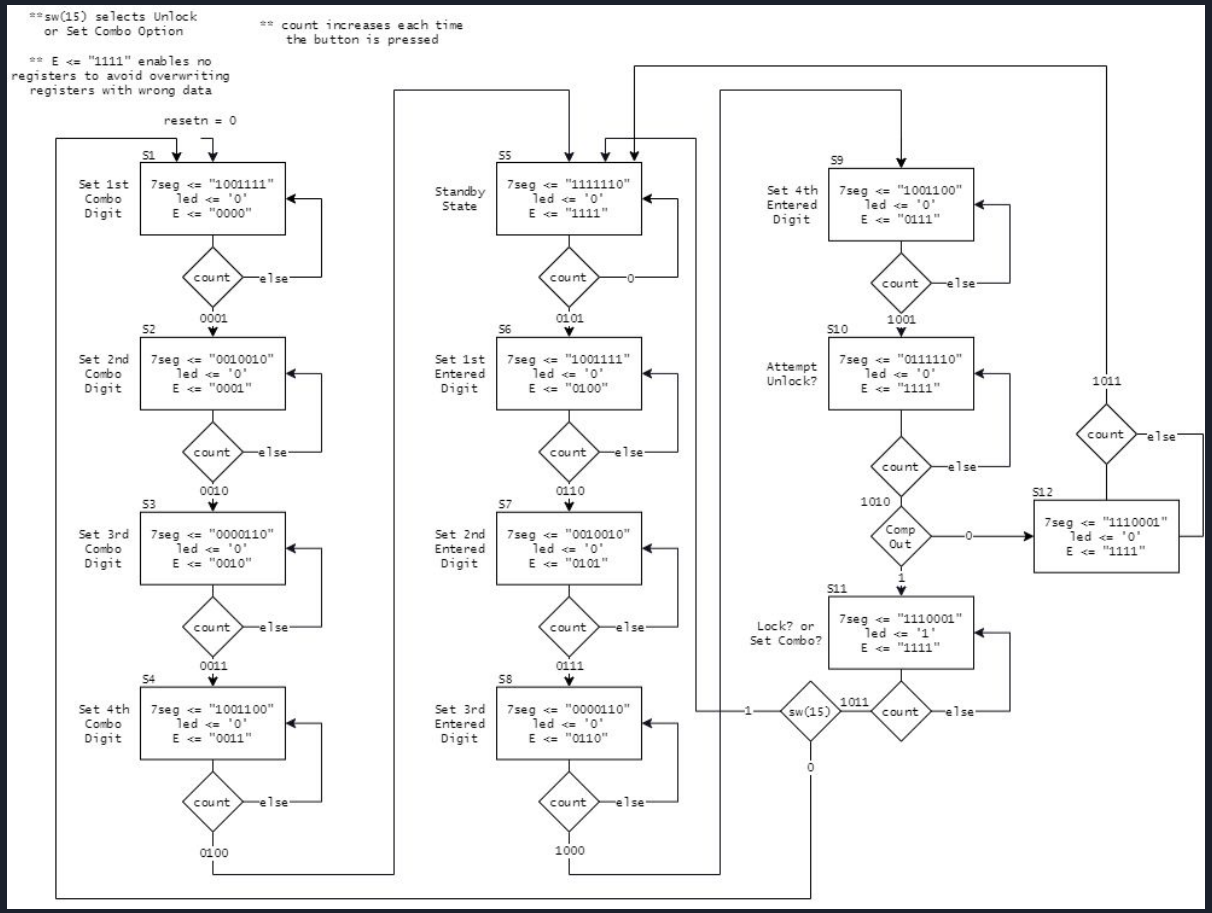
Video

https://youtu.be/LSA9jJgUTYc

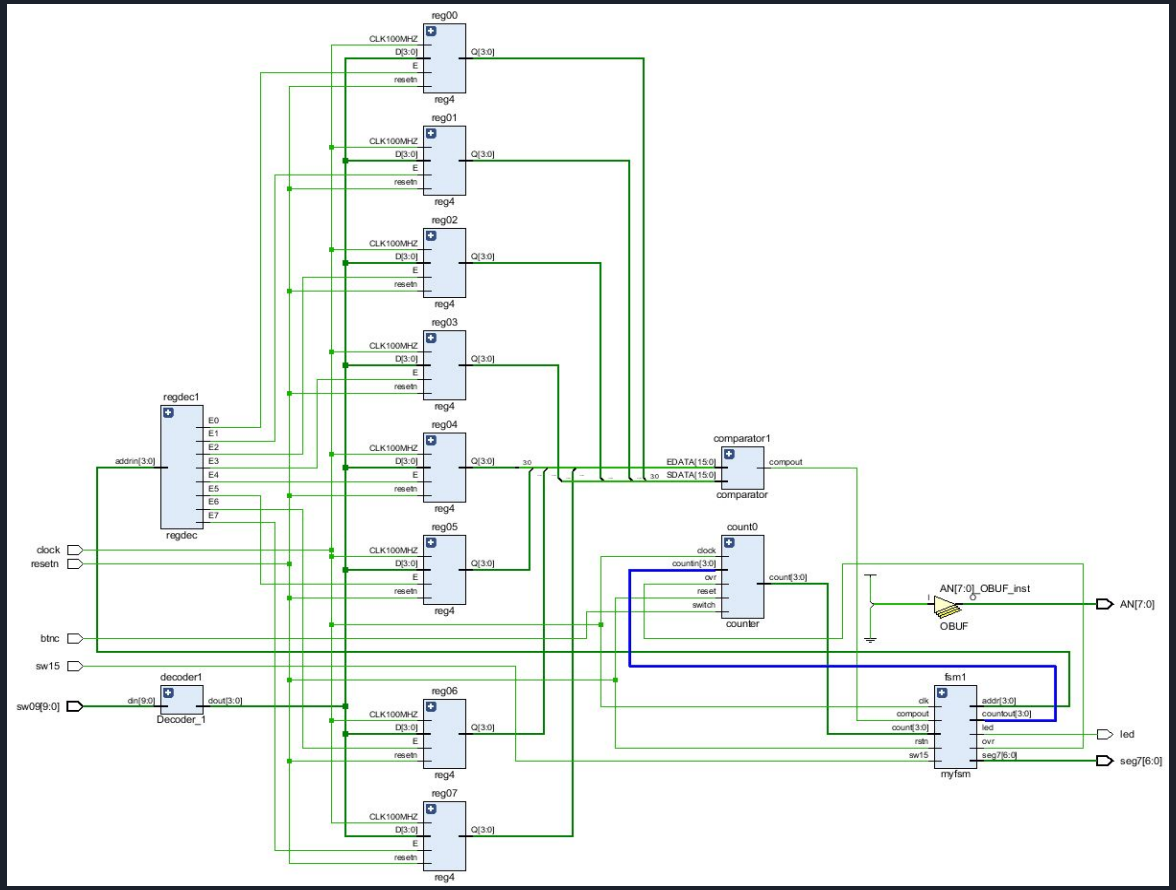
Methodology - TOP Block Diagram/Datapath



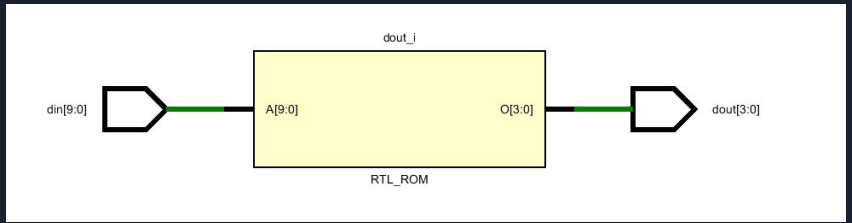
Methodology - FSM/Control

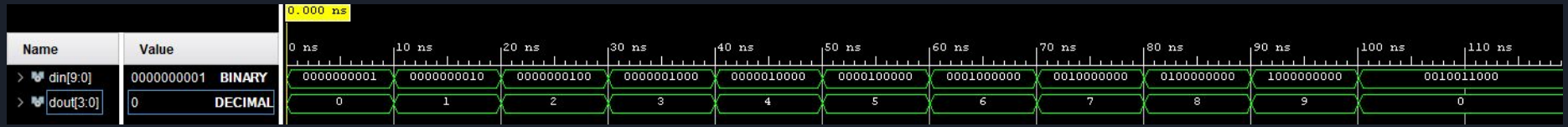


TOP Schematic



10 bit - 4 bit Decoder





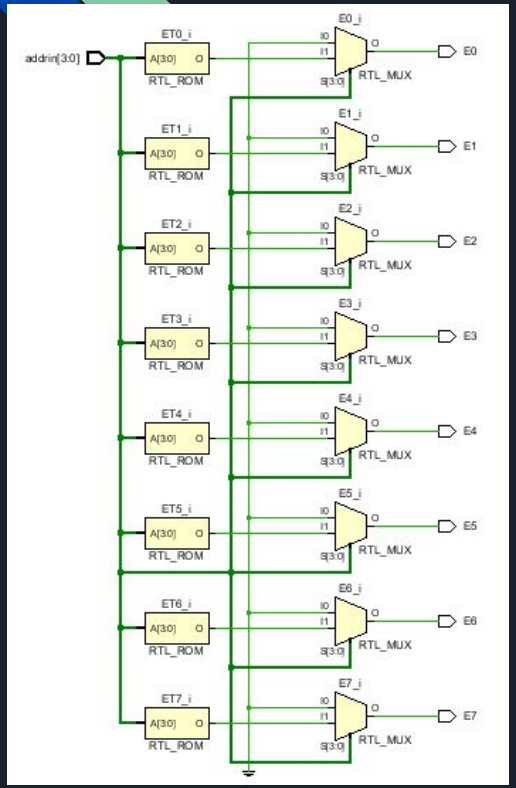
Example:

Input: “0000001000” = Output: “0111”

Input: “9876543210” = Output: Binary of bit that is high

*Asynchronous

Register Enable Decoder



Example:

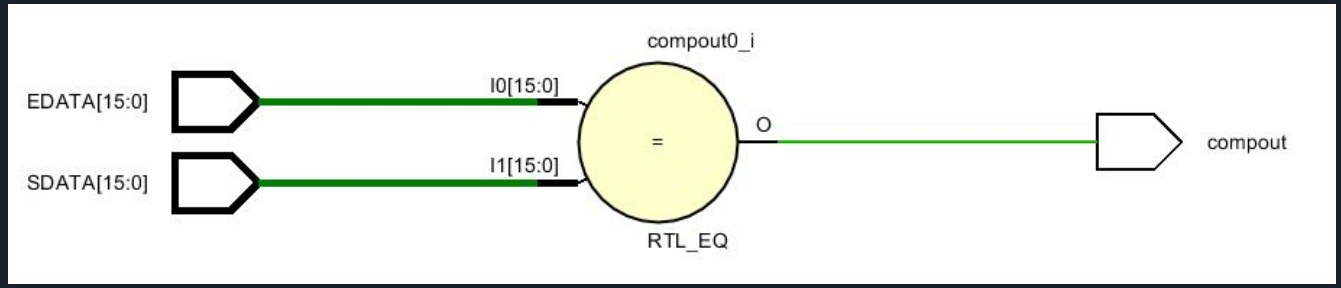
Addrin enables respective register in binary.

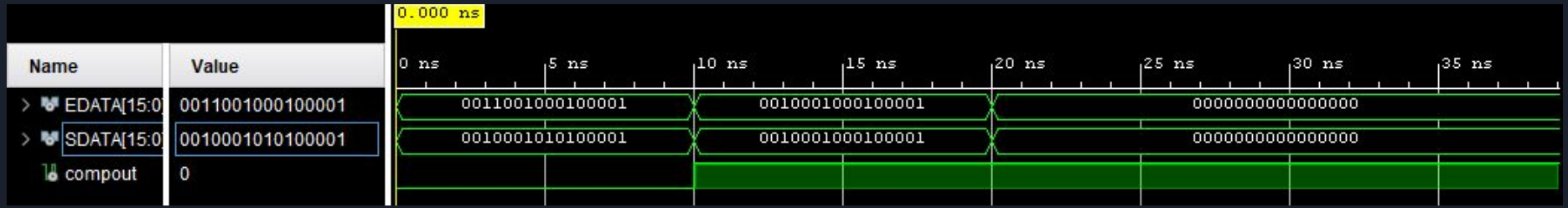
Addrin = “0010”, enables register 2..

Addrin = “1111”, disables all registers to prevent overwrites

*Asynchronous

Comparator



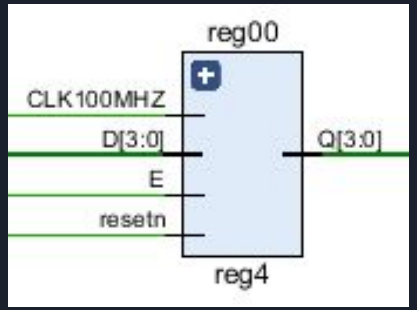


Example:

If EDATA = SDATA then compout = ‘1’ else compout = ‘0’ end if;

*Asynchronous

4 bit Register



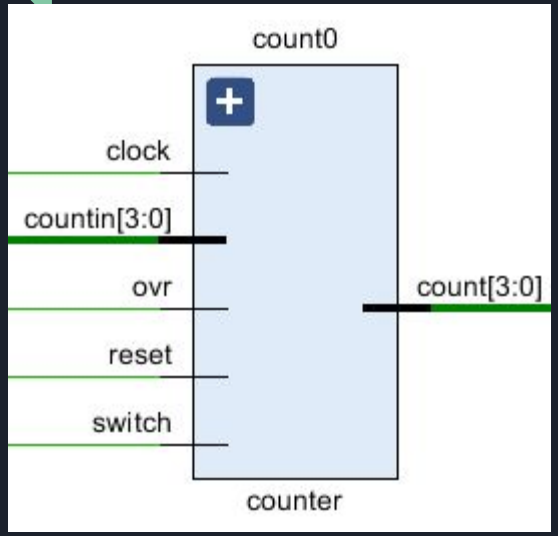
Example:

On rising edge of clock, if E = ‘1’ load D => Q

If resetn = ‘0’ Q => “0000”.

*Synchronous

Debouncer/Counter



Example:

On rising edge of clock, count a “pulse”.

If switch is high, it must remain high for X amount of clock cycles (pulses) until count is iterated.

If ovr is high, overwrite the current count with, countin.

If reset is low, reset the system.

*Synchronous

Experimental Setup

Criteria for experimental setup:

- Evaluation of individual components and functions
- Evaluation of the entire system
- Test edge cases

In order to verify the individual components, we tested each component with test data generated by a test bench.

In order to verify the functionality of the entire system we tested the top level functionality of the system with test data generated by a test bench.