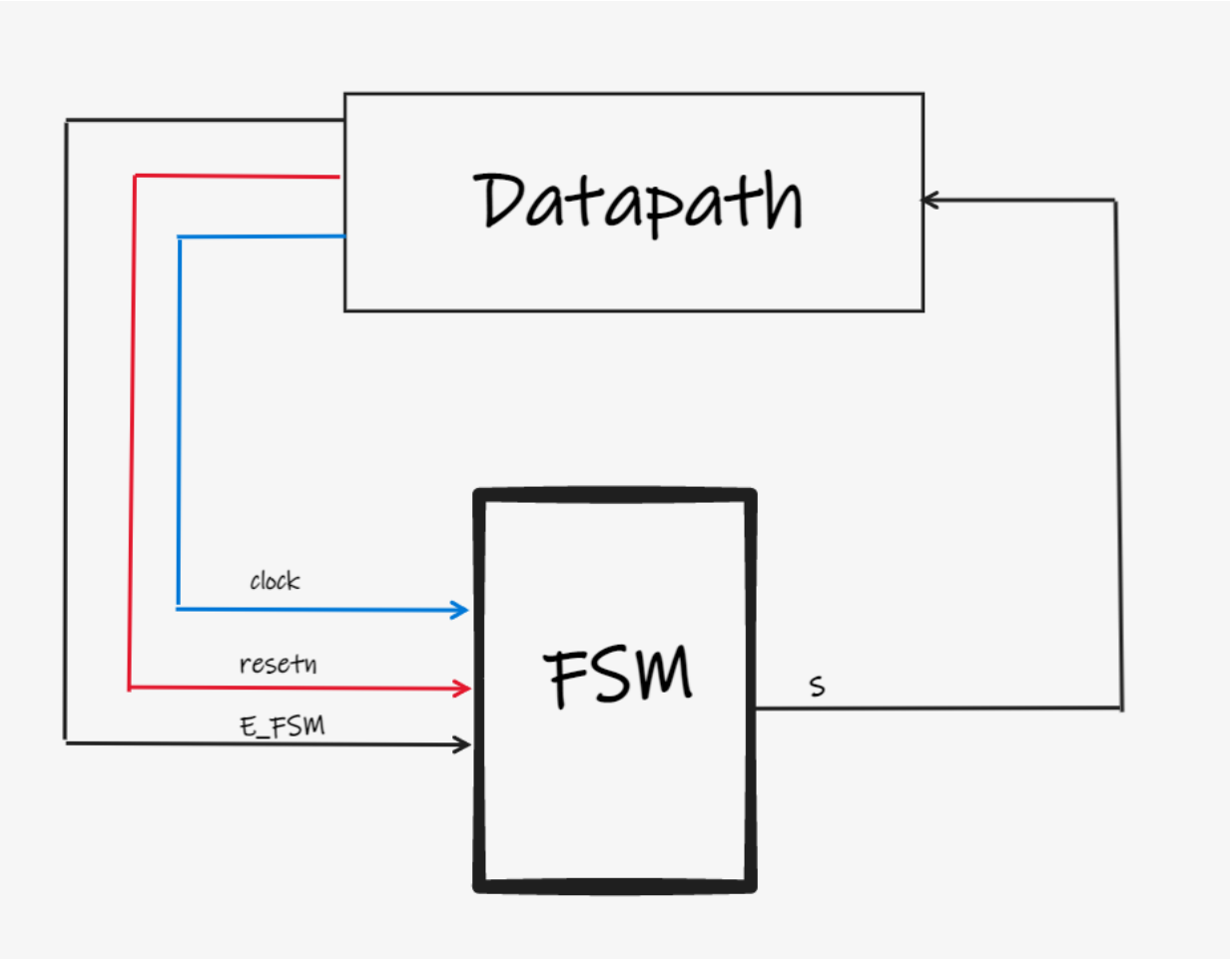
Stopwatch

Mohammed Shatit, Matthew Adams, Austin Nguyen

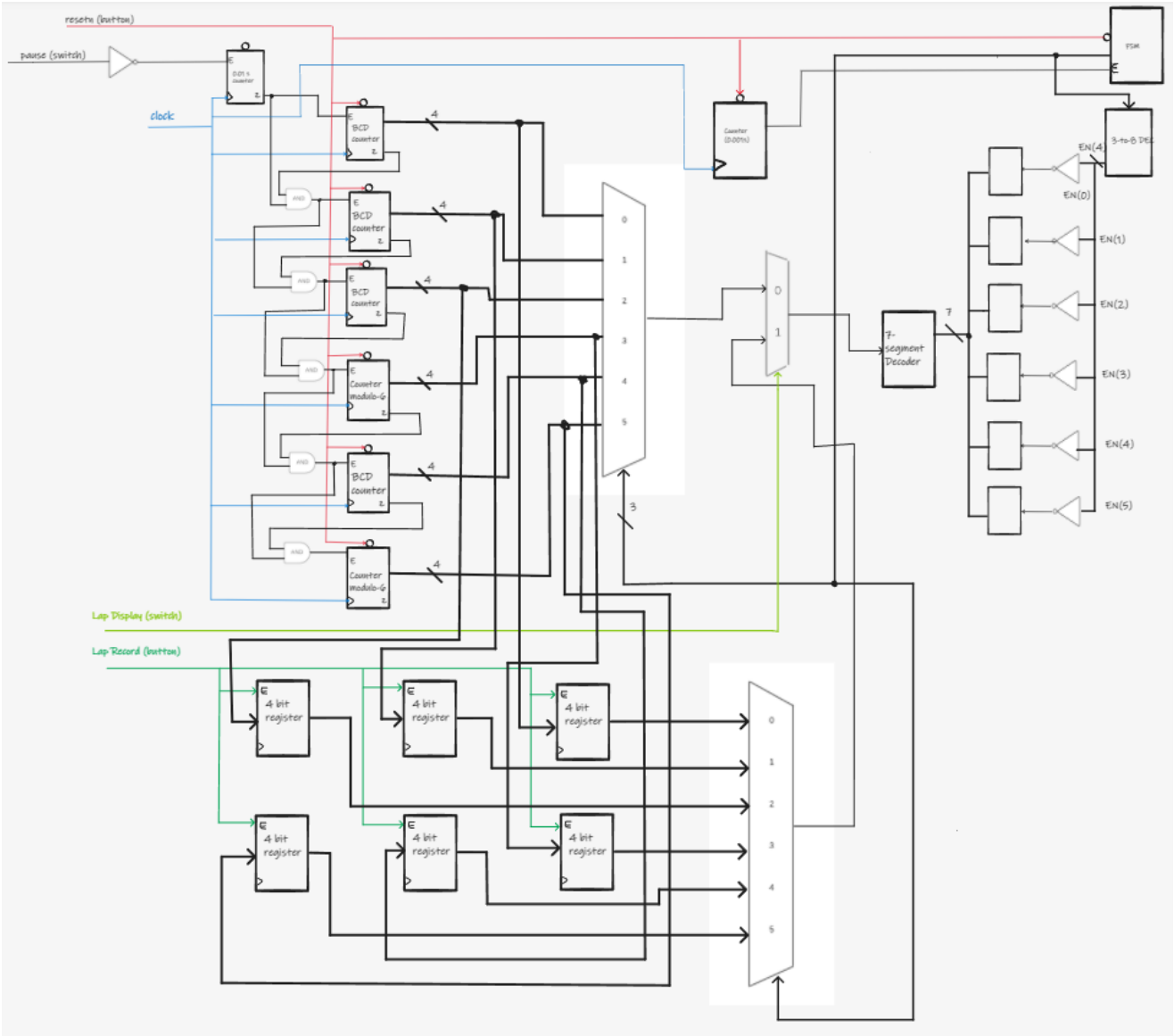
Digital Stopwatch Features

- **Start / Pause -** Controlled by switch, should be “high” on boot. Switch to “low” to begin counting and switch “high” to pause.
- **Restart -** Controlled by a button that resets the stopwatch and clear the saved lap to "0" when set to "high"
- **Lap -** Controlled by a button to capture the time of the lap and displayed using a switch to switch between current time and lap time

Circuit Design: Overview



Circuit Design: Datapath



Circuit inputs/outputs

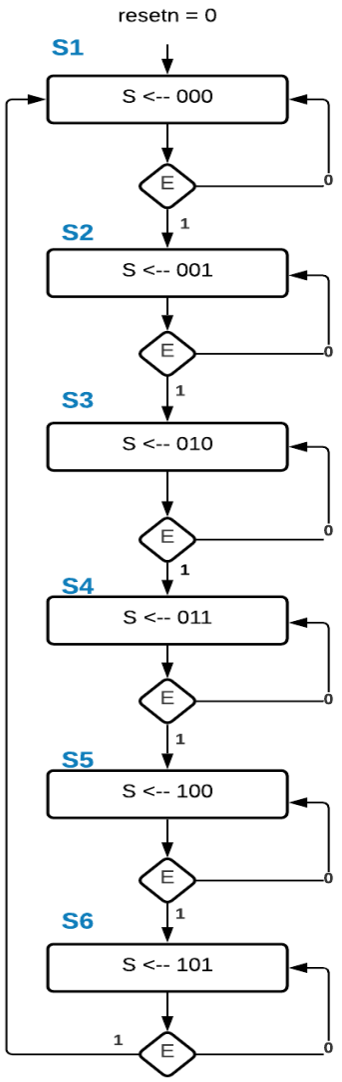
Inputs

+ Start/pause - switch
+ Clock – running clock
+ resetn – button to reset the running count and the saved lap
+ LapWrite – button to write the current time to the register and save it as lap time
+ LapRead – to switch between displaying current and lap time

Outputs

+ 6-bit EN
+ 6-bit CACG

Circuit Design: Algorithmic State Machine

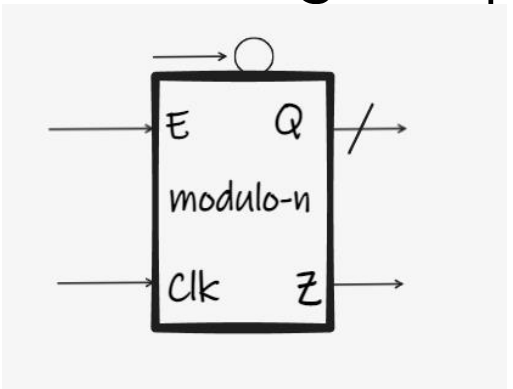


Algorithmic State Machine

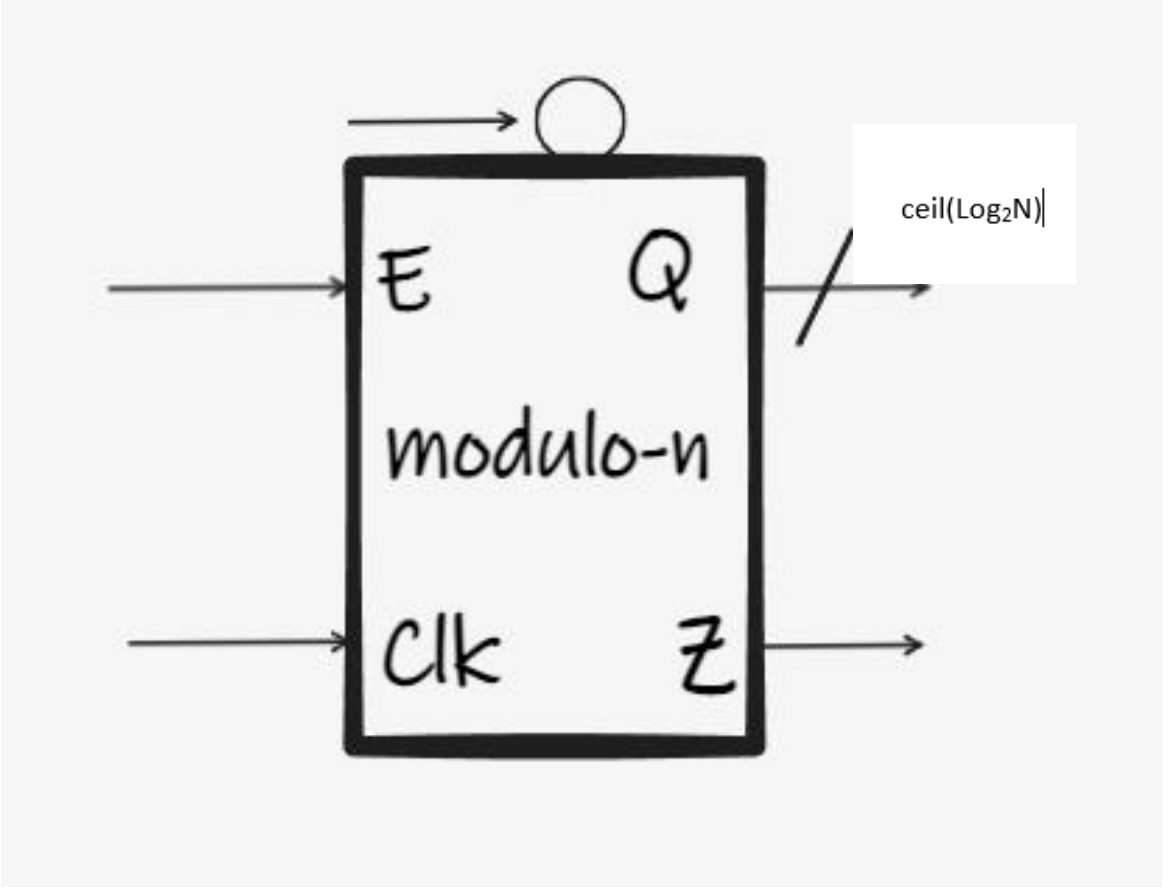
- 6 states
- 2 inputs (E, resetn)
- 1 3-bit output (S)
- The finite state machine is used to loop through six states to have one display on at a time
- It controls the select signals of the 6-to-1 multiplexers
- Its state is changed based on the 0.001 milliseconds counter

Modulo-N Counter

- 2 modulo-6 counters to represent the tens place of the seconds and minutes
- 1 modulo-1,000,000 counter to count for 0.01 seconds
- 1 modulo-100,000 counter to change the state of the finite state machine every millisecond with "high" input for enable at all times

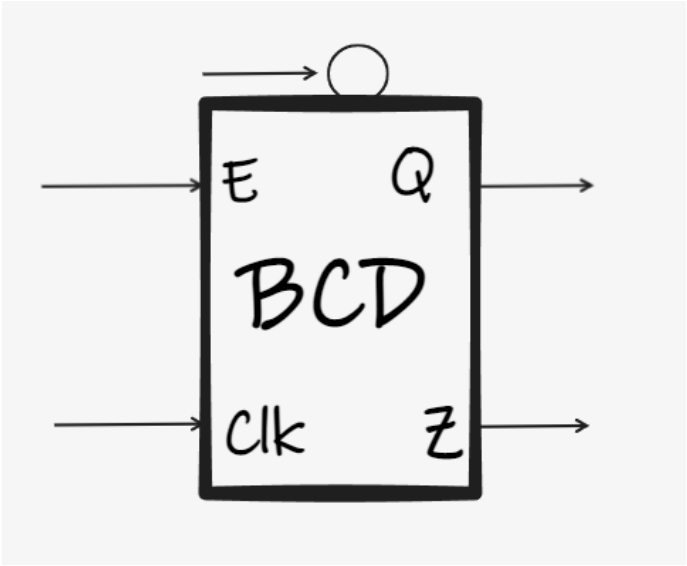


Modulo-N Counter



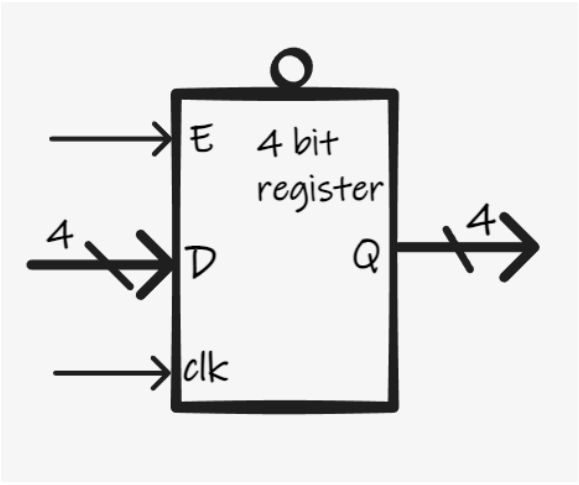
BCD Counter

- Used to represent the ones of the minutes and seconds and the tenths and hundredths of seconds



Register

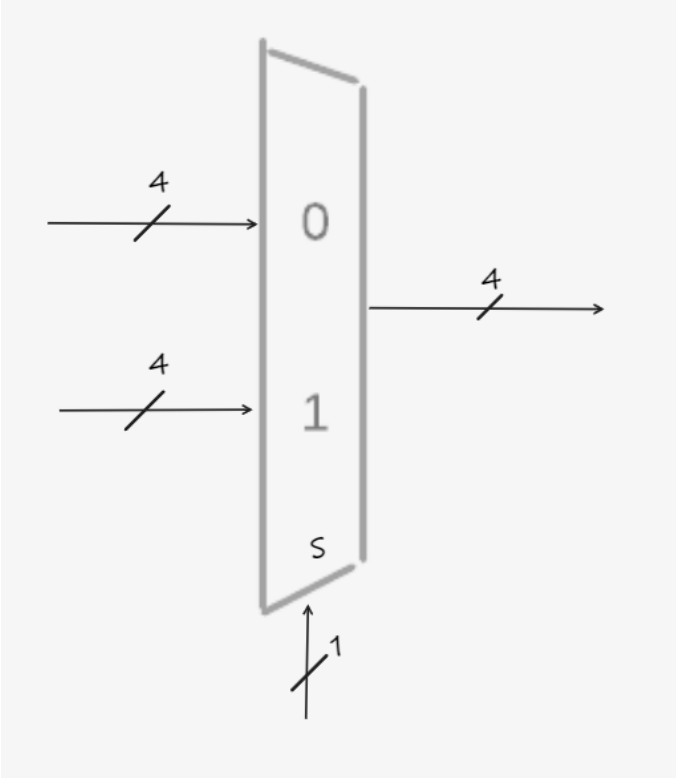
- 6 Register used to hold the value of each counter for the lap functionality, enabled when the lap button is pressed



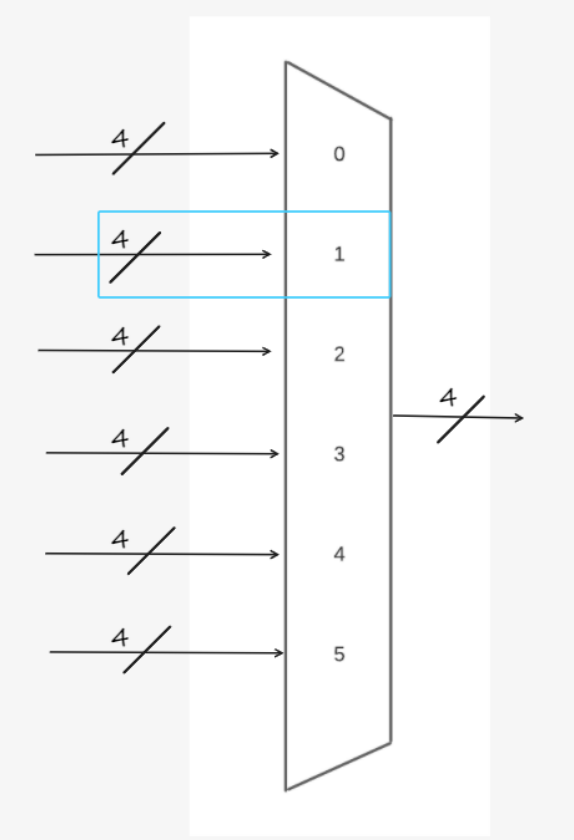
Multiplexer

- 2 6-to-1 multiplexers. One used to loop through and display the current time of the counters and the other is used to display the time of the save lap. Their selects are controlled by the FSM
- 2-to-1 multiplexer controlled by a switch to flip between displaying the current or lap time

Multiplexer 2-to-1

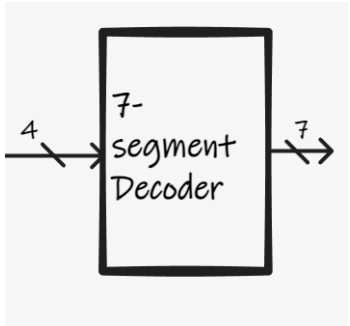


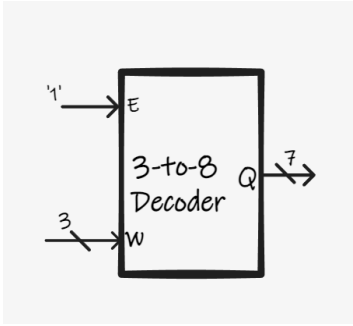
Multiplexer 6-to-1



Decoder

- 3-to-8 decoder to convert the 3-bit output of the FSM into an 8-bit AN signal to power up the 7-segement displays
- 7 segment decoder to convert the 4-bit output of the counters into a 7-bit signal for the LEDs of the display

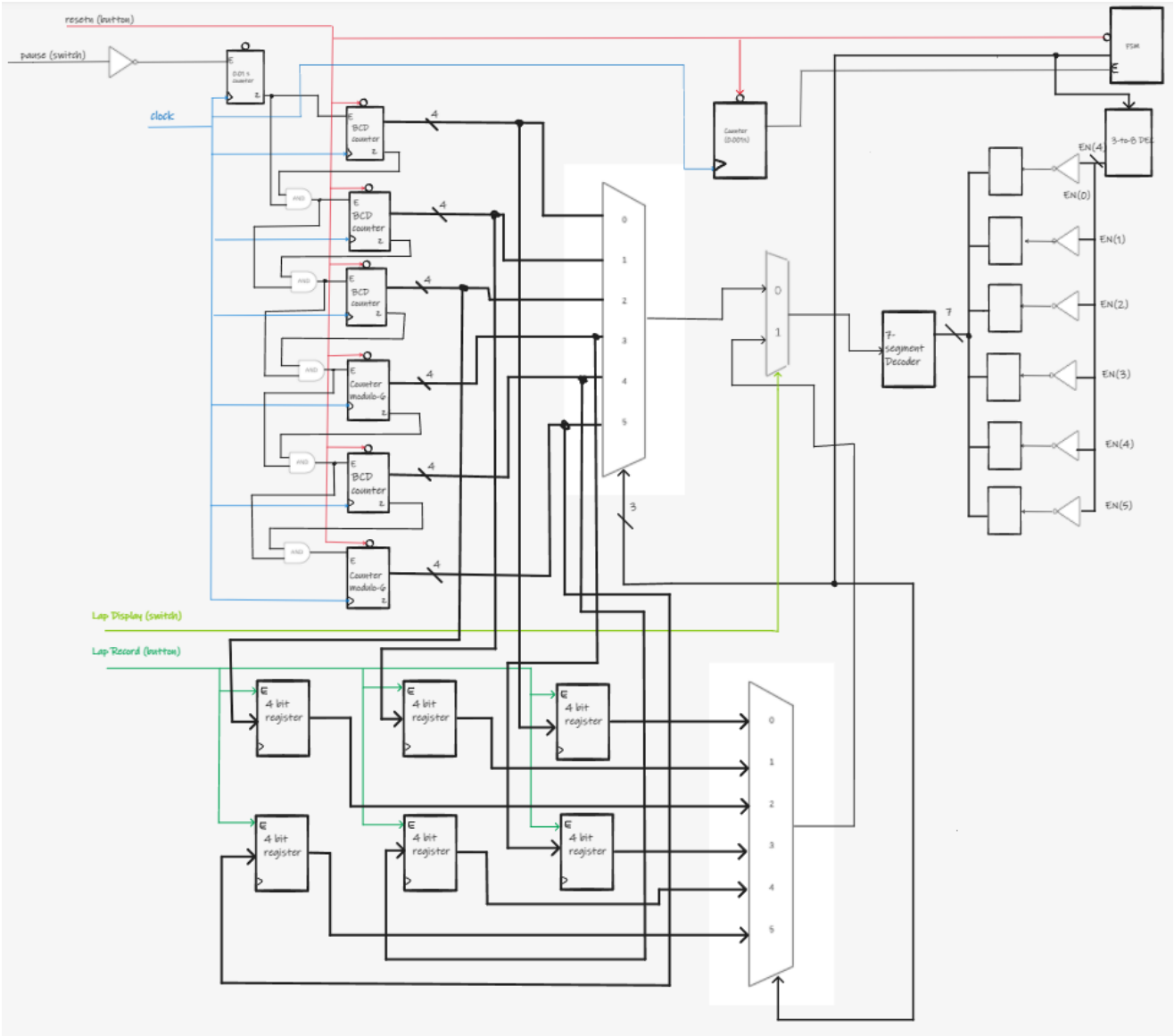




Logic Gates

- AND Gates: used to and the signal of the Z output of the counter and the previous Enable signal so that the next counter increment only if the previous counter's Z is "high" and pause is "low"
- NOT Gates: used to invert some signals from high to low and from low to high

Circuit Design: Datapath



Video Representation