Signed 6-Bit Calculator

Designed and Presented By:

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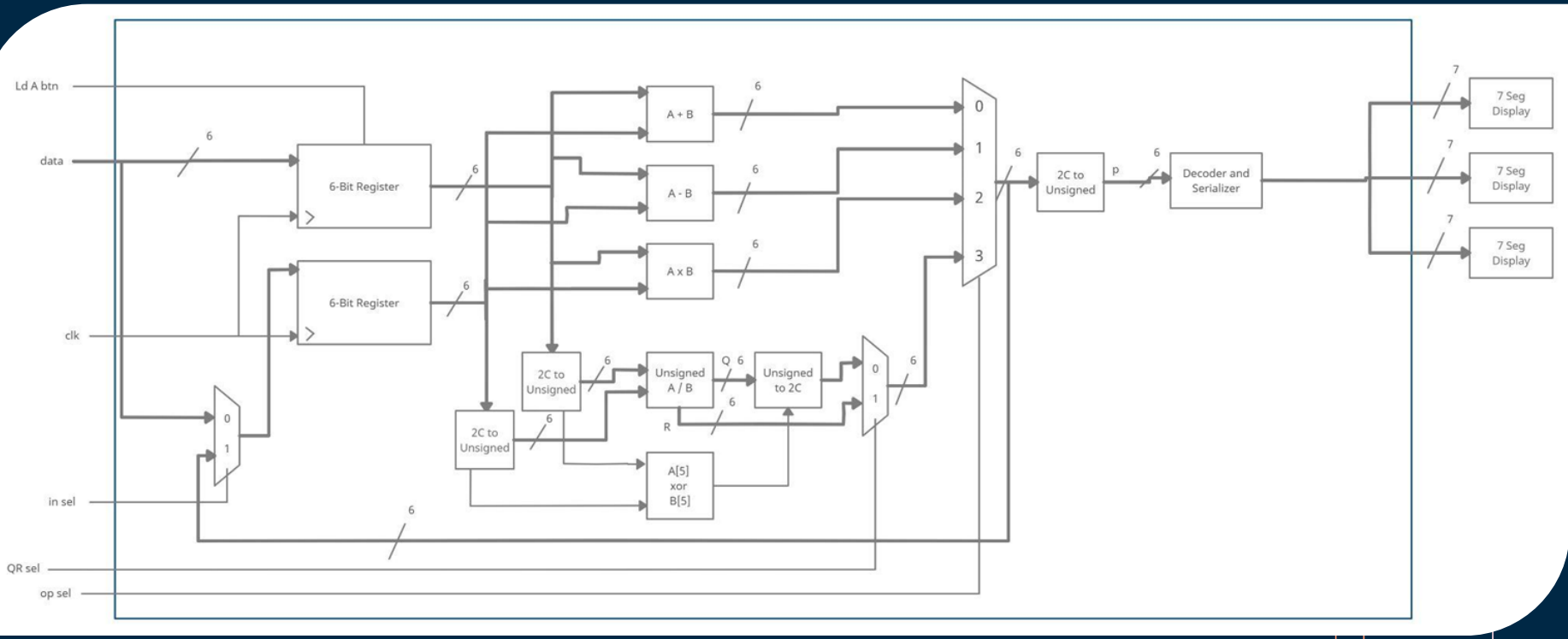
The Design:


Ld A btn
data
clk
in sel
QR sel
op sel
6-Bit Register
6-Bit Register
A + B
A - B
A x B
2C to Unsigned
2C to Unsigned
Unsigned A / B
Unsigned to 2C
A[5] xor B[5]
2C to Unsigned
Decoder and Serializer
7 Seg Display
7 Seg Display
7 Seg Display

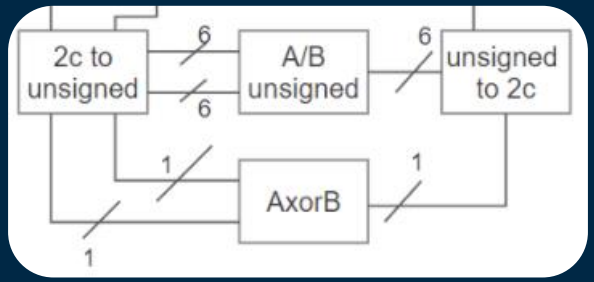
Divider:

- Based on Professor Llamocca's Unsigned Divider

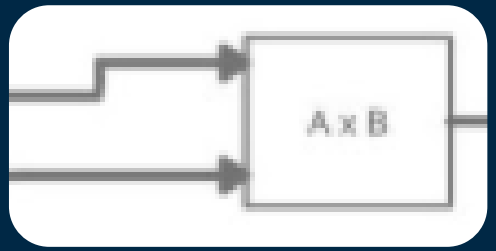
Comes in as a signed(2C) number

Converted to unsigned and put through unsigned divider

Use the MSB of both inputs to convert back to a 2C Signed Answer



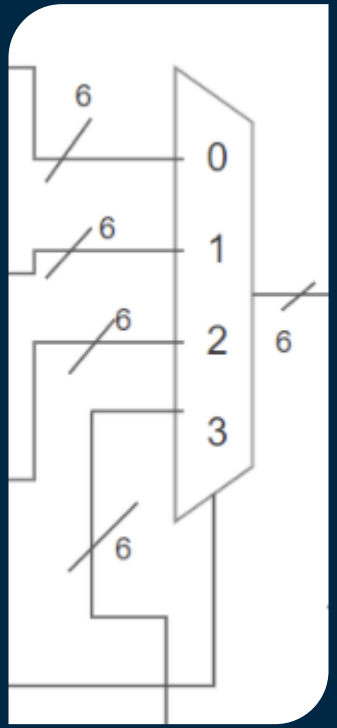
Multiplier



- Very basic component takes advantage of VHDL's built in math functions.
- Takes two 6-bit inputs and saves them as a 12 bit output
- F <= A*B;

Basic 4-to-1 MUX

- Backbone of the output function of the calculator
- Receives the answer of all four operations and outputs only the desired answer.



Key:

00 -> Addition

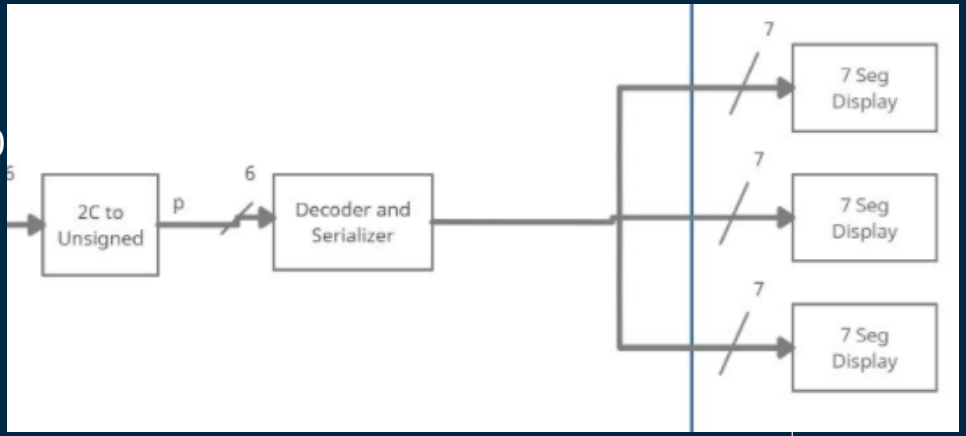
01 -> Subtraction

10 -> Multiplication

11 -> Division

7-Segment Decoder

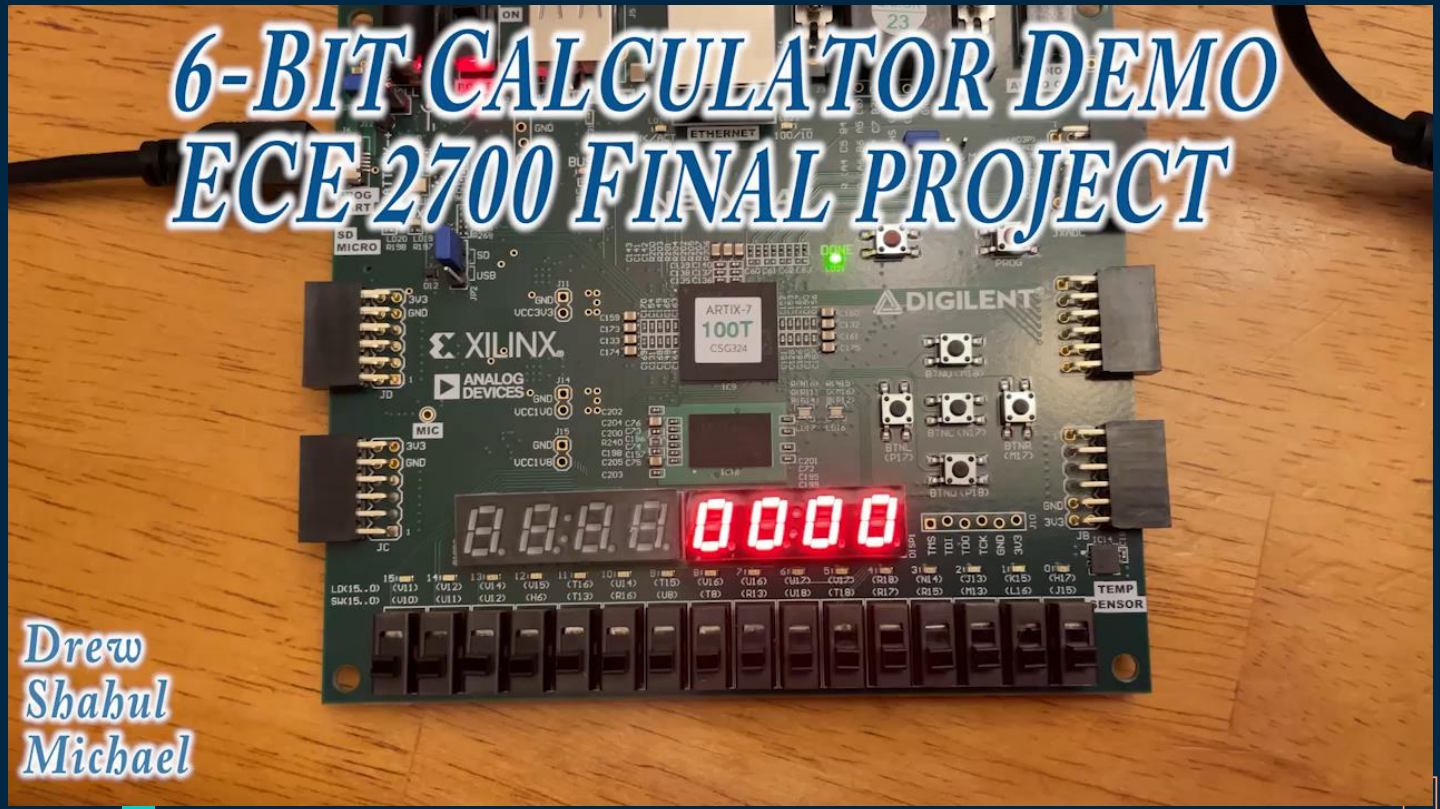
- Receives answer as a 6-bit signed(2C) number
- Converts to a 12 bit signed BCD and then segmented into three four bit numbers
- A counter and state machine enables each display and changes the data once every millisecond.



Problems Faced

- Organizing Files
  - Each member made files with the same function that needed to be consolidated when all the files were put together. (e.g. ‘Full Adder’ vs ‘FA’)
- Using multiple 7-segment displays at the same time
- Code working individually but not when integrated together

Demonstration:



Thank You!

Any Questions?