Digital Stopwatch

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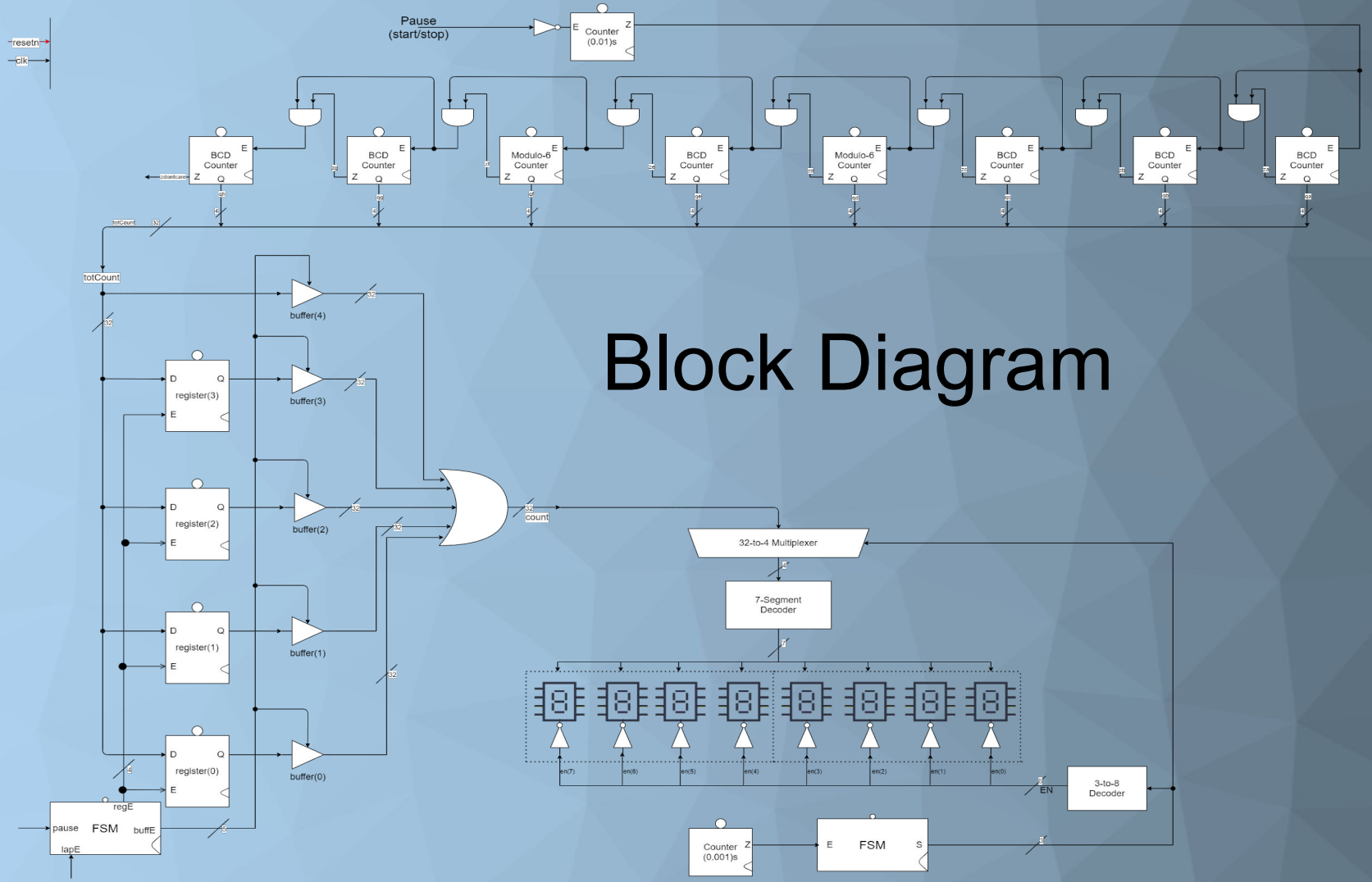
What is it?

We designed and implemented a fully functional stopwatch

Features include:

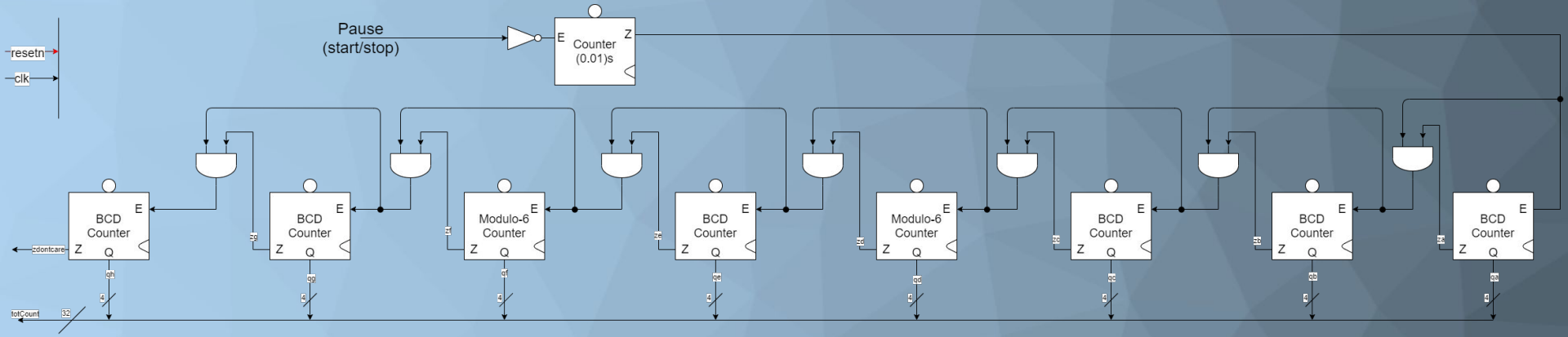
- Start/ stop, lap, and reset button
- Ability to track up to 99 hours, 59 minutes, and 59.99 seconds



Block Diagram

Components

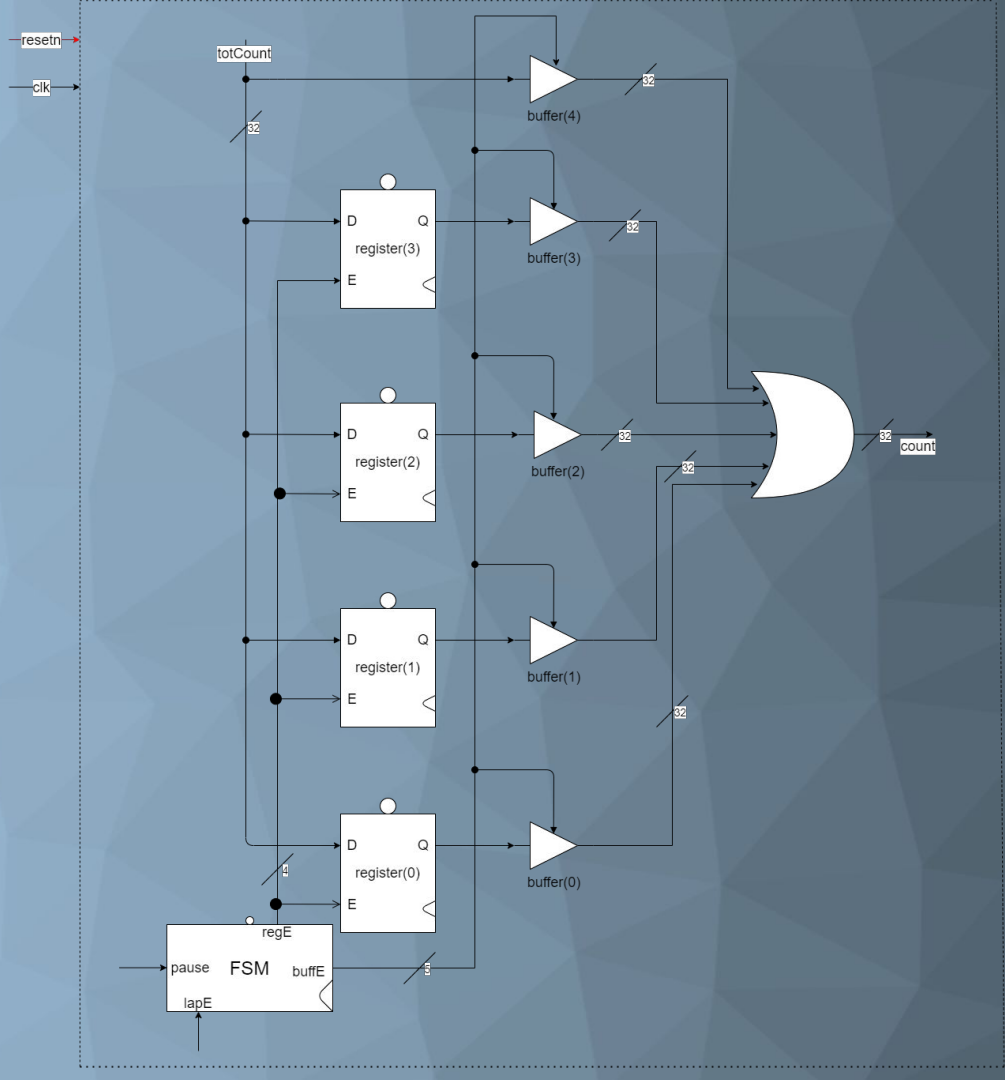
Counting Element



- Used to count time passed
- Made up of 9 total counters to reach as high as 99 hours, 59 minutes, 59 seconds
- 1 counter used to regulate the count of all others, connected to their enable

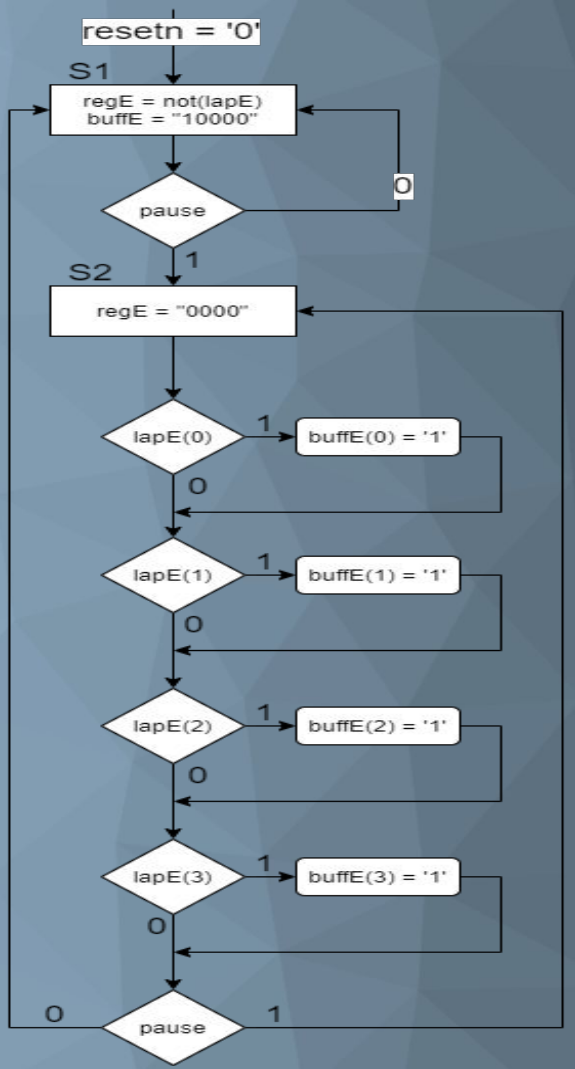
Lapping Element

- Uses registers and tri-state buffers
- Registers will store data when enabled, otherwise will keep previous value
- Tri-state buffers used to determine whether the data may pass on to be displayed



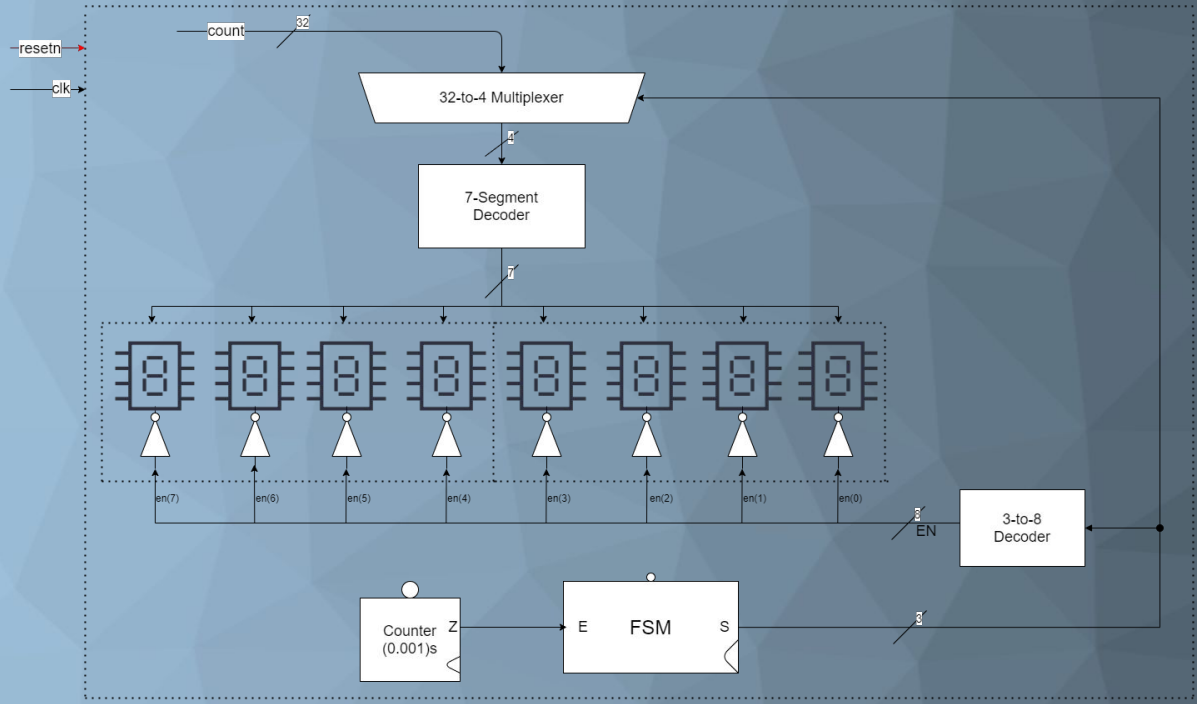
Finite State Machine For Lapping

- This FSM is a three state machine
- Allows users to store up to four lap times
- Uses switches on FPGA board to choose which lap time is displayed



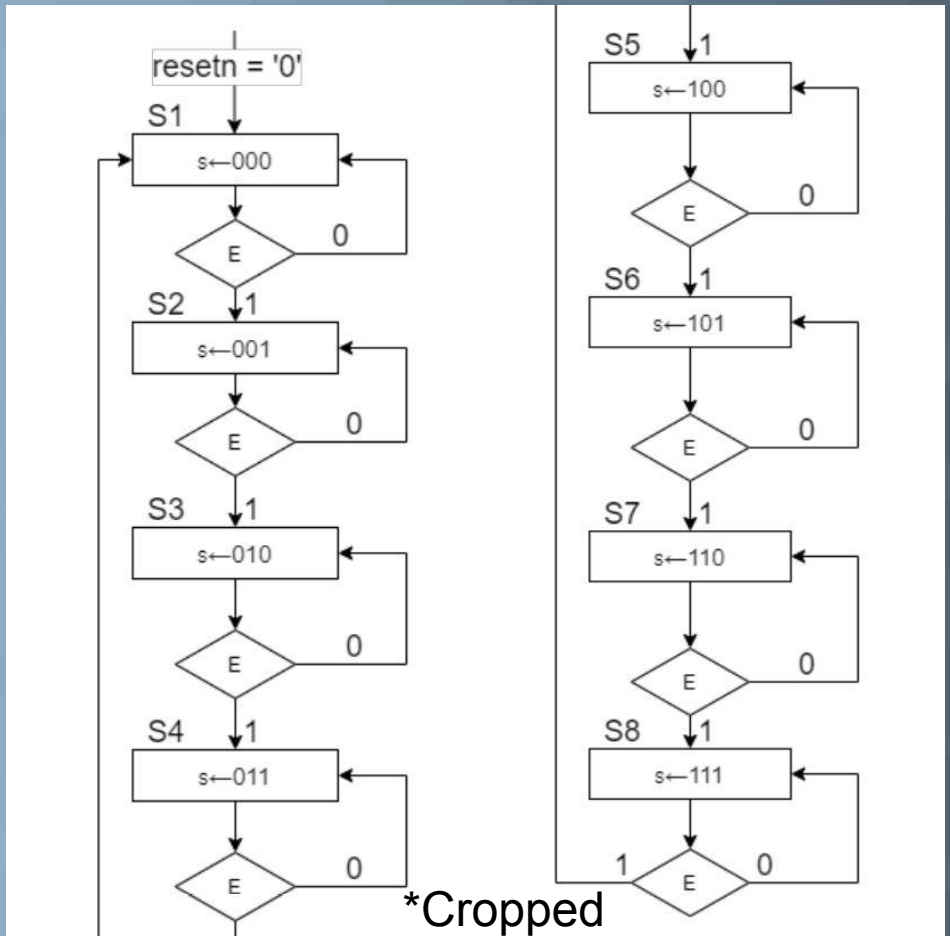
Display Element

- Used to display elapsed time
- Serializer illuminates each digit for 1 ms every 8 ms.



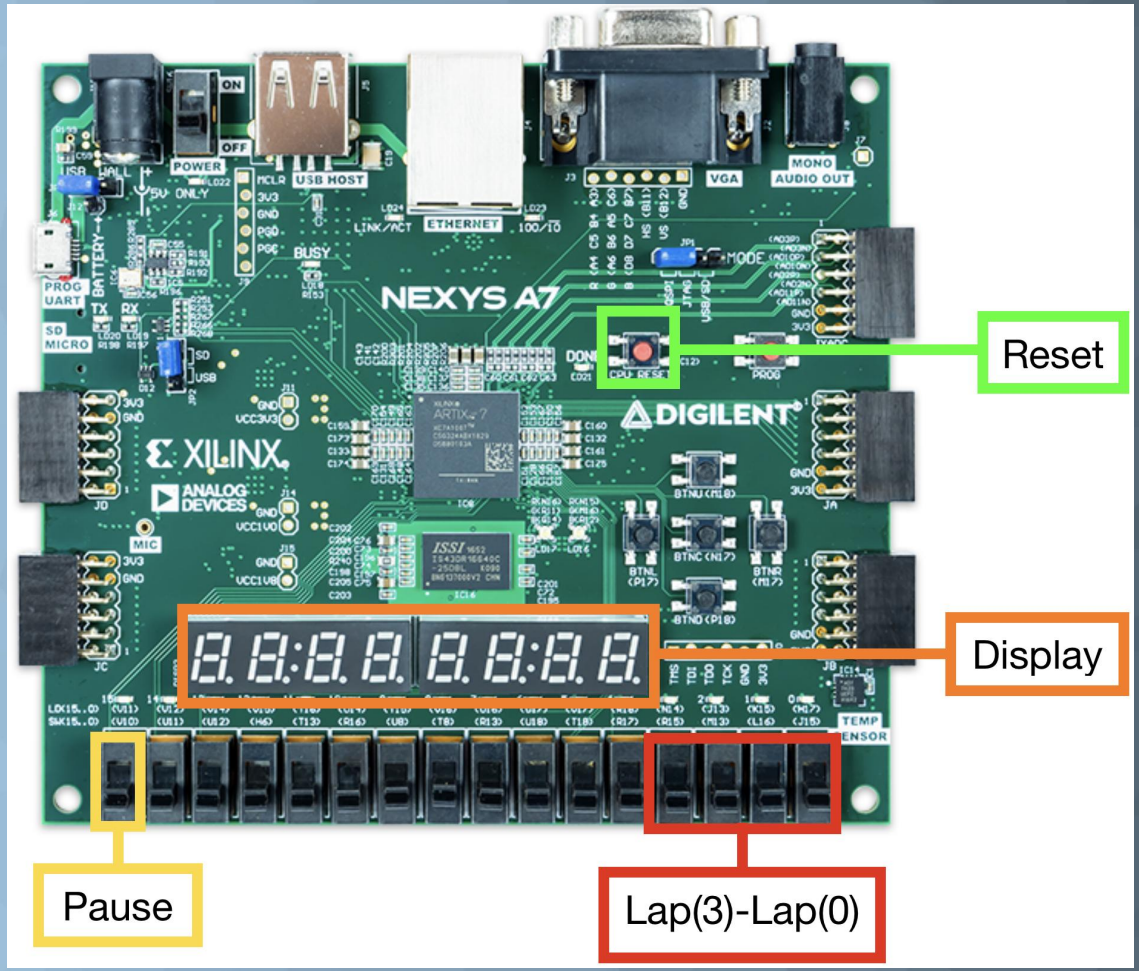
Finite State Machine For Display Element

- Selects new input every millisecond
- Acts as selector for the multiplexer
- Uses an enable controlled a .001 second counter
- Counter output pulse feeds into enable of FSM every millisecond to select new input for multiplexer



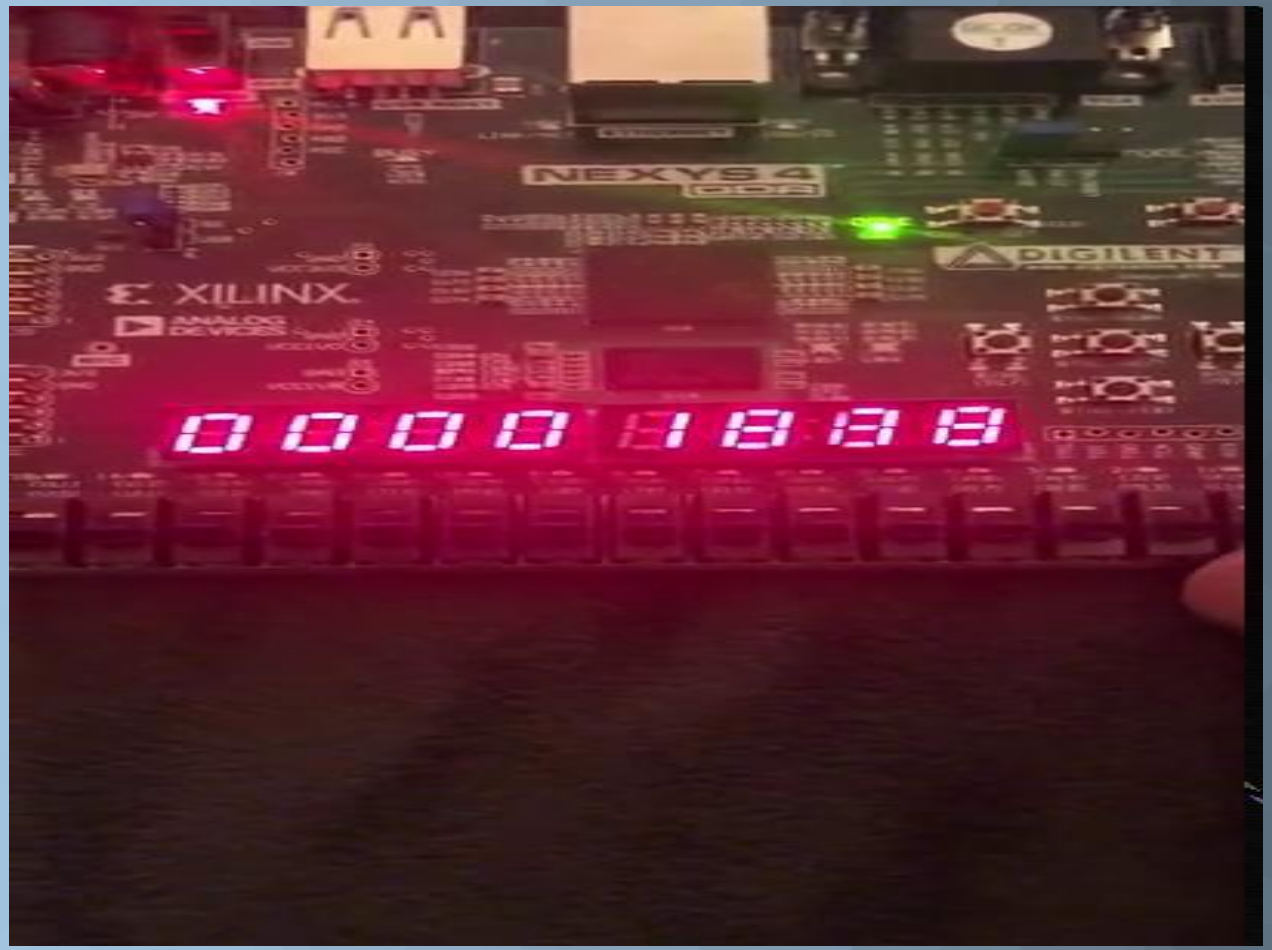
*Cropped

FPGA Implementation



Demo

https://youtu.be/1j8GTl7T30w



Any Questions?