INSTRUMENT TUNER

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ECE 2700 DIGITAL LOGIC DESIGN

DESCRIPTION

- Our circuit is an instrument tuner that identifies and displays the musical note being played into it from an external source.

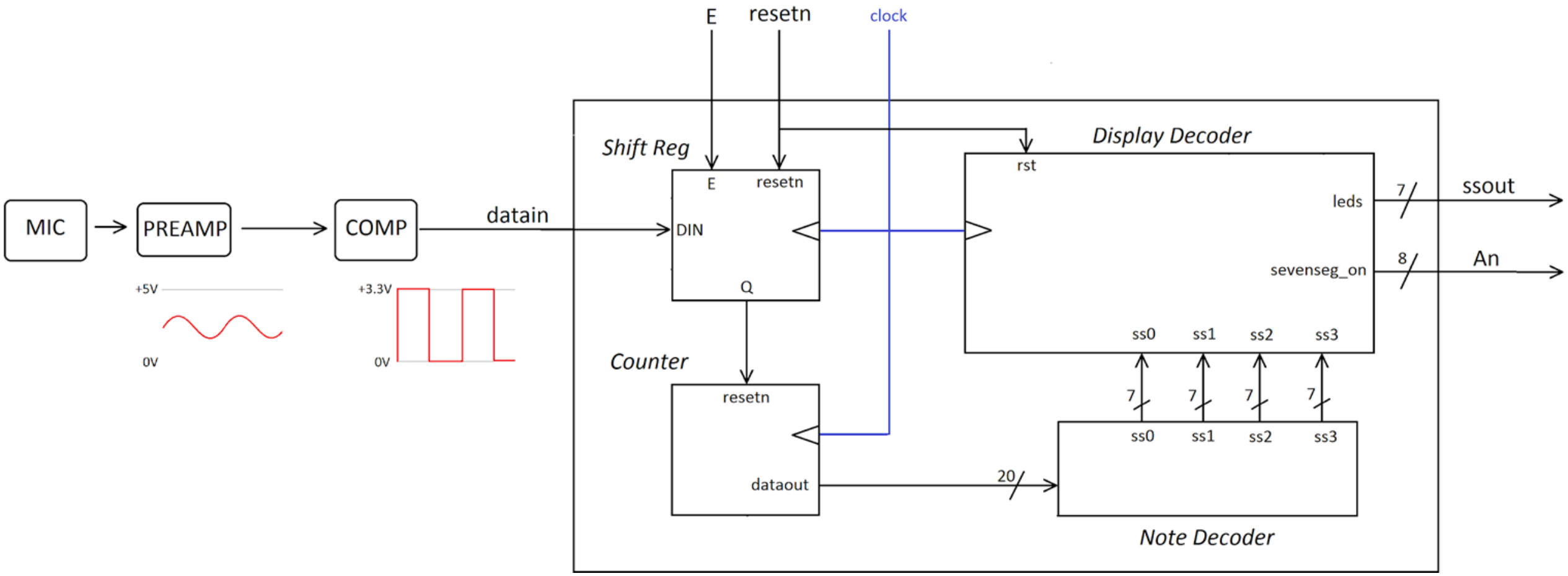
- Two Parts:
  - External circuit
  - Digital Circuit

BACKGROUND

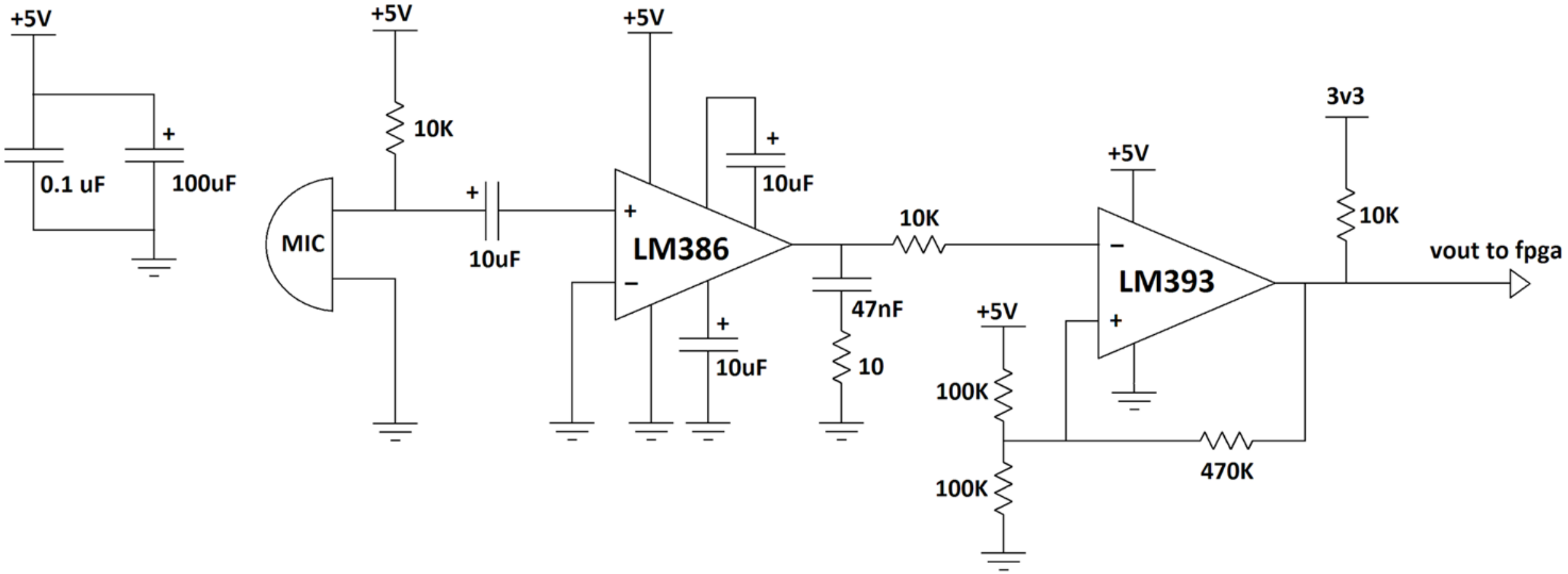
In Western musical notation there are a total of 12 notes, each set at a specific pitch according to a pitch standard (A440)

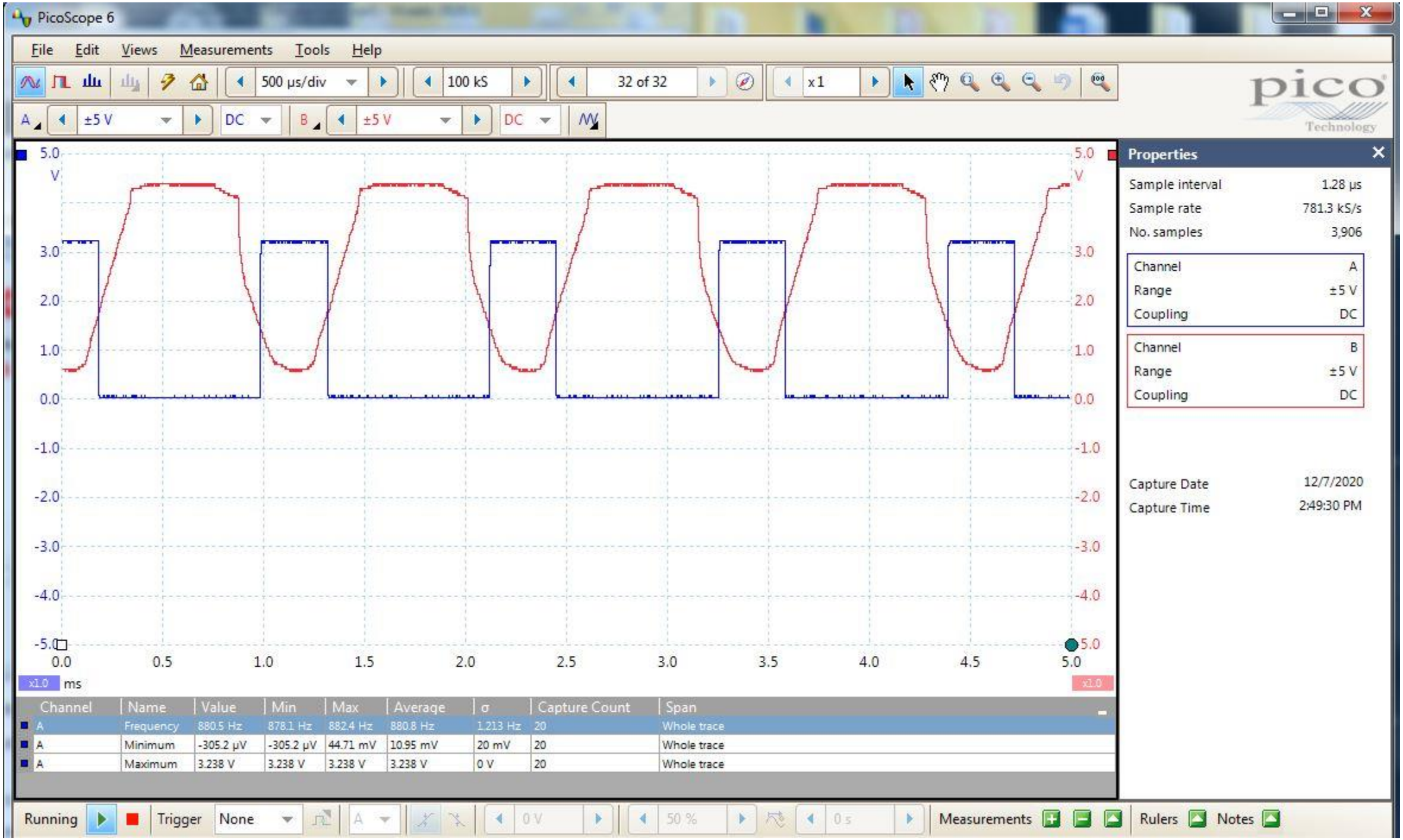
A --- Bb --- B --- C --- Db --- D --- Eb --- E --- F --- Gb --- G --- Ab

Circuit (Block Diagram)



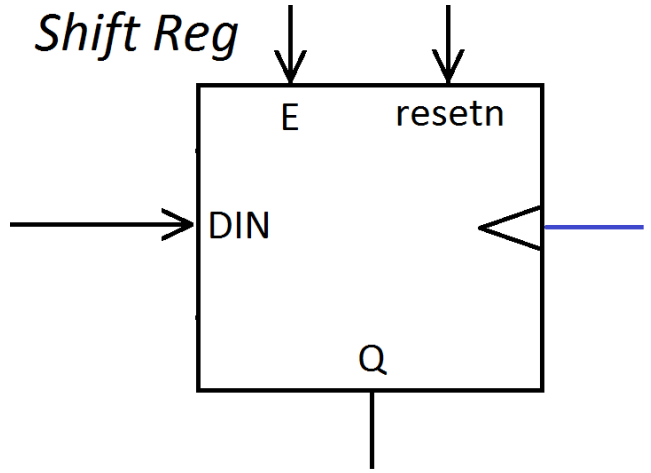
External Circuit




PicoScope 6
File Edit Views Measurements Tools Help
500 µs/div
100 kS
32 of 32
x1
A ±5 V DC
B ±5 V DC
pico Technology
Properties
Sample interval 1.28 µs
Sample rate 781.3 kS/s
No. samples 3,906
Channel A
Range ±5 V
Coupling DC
Channel B
Range ±5 V
Coupling DC
Capture Date 12/7/2020
Capture Time 2:49:30 PM
5.0 V 3.0 2.0 1.0 0.0 -1.0 -2.0 -3.0 -4.0 -5.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 ms
Channel Name Value Min Max Average σ Capture Count Span
A Frequency 880.5 Hz 878.1 Hz 882.4 Hz 880.8 Hz 1.213 Hz 20 Whole trace
A Minimum -305.2 µV -305.2 µV 44.71 mV 10.95 mV 20 mV 20 Whole trace
A Maximum 3.238 V 3.238 V 3.238 V 3.238 V 0 V 20 Whole trace
Running Trigger None
Measurements Rulers Notes

SHIFT REGISTER

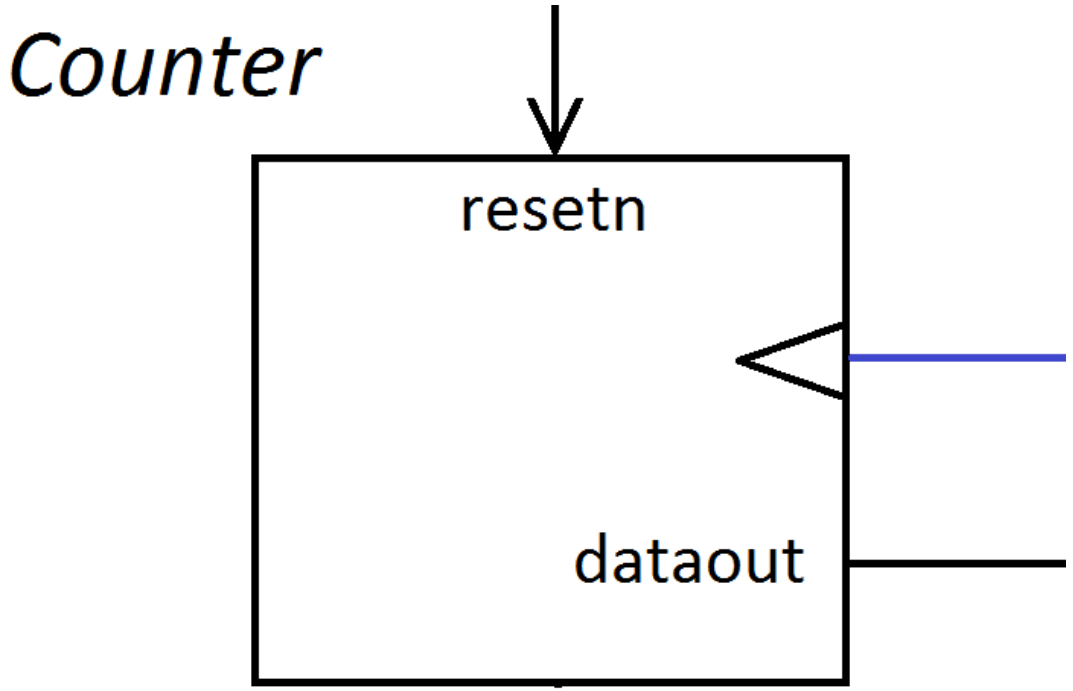
- 2-bit shift register
- datain carries the input wave
- Output Q signifies that the wave has been “registered”



MSB	LSB	Q
0	0	0
0	1	0
1	0	1
1	1	0

COUNTER

- Add 1 to count ‘n’ for every clock event (rising edge).
- Q from the shift register acts as a reset for the counter, which outputs the final count and sets the count back to zero.

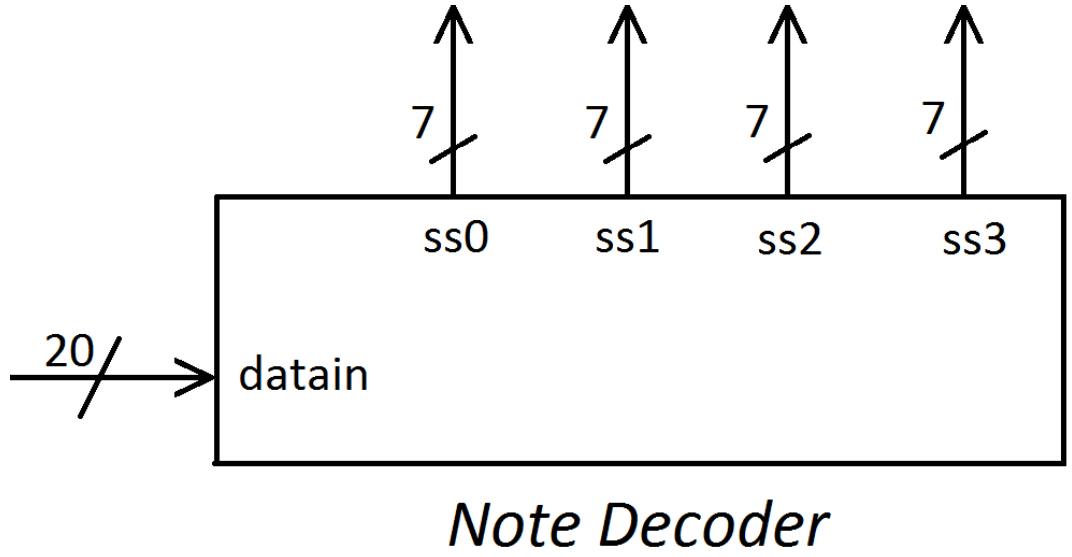


NOTE DECODER

Final count = datain = 50MHz / (Freq. in Herz)

Note/Condition	Frequency Range (Hz)	Final Count Range
E4	328.688 to 330.592	152119 to 151244
In Between E4 and F4	330.592 to 348.232	151243 to 143583
F4	348.232 to 350.252	143582 to 142754

Note/Condition	Disp 0	Disp 1	Disp 2	Disp 3
Bb4	-------	--------	“B”	“b”
In Between Bb4 and B4	“B”	“b”	“-”	“B”
B4	---------	--------	---------	“B”



Note Decoder

DISPLAY CONSIDERATIONS

- Out from the note decoder are four std_logic_vector outputs intended for four 7-seg displays, but on the Nexys 4/DDR only one 7-seg configuration can be displayed at a time, so we have to implement a data selector/7-seg serializer.

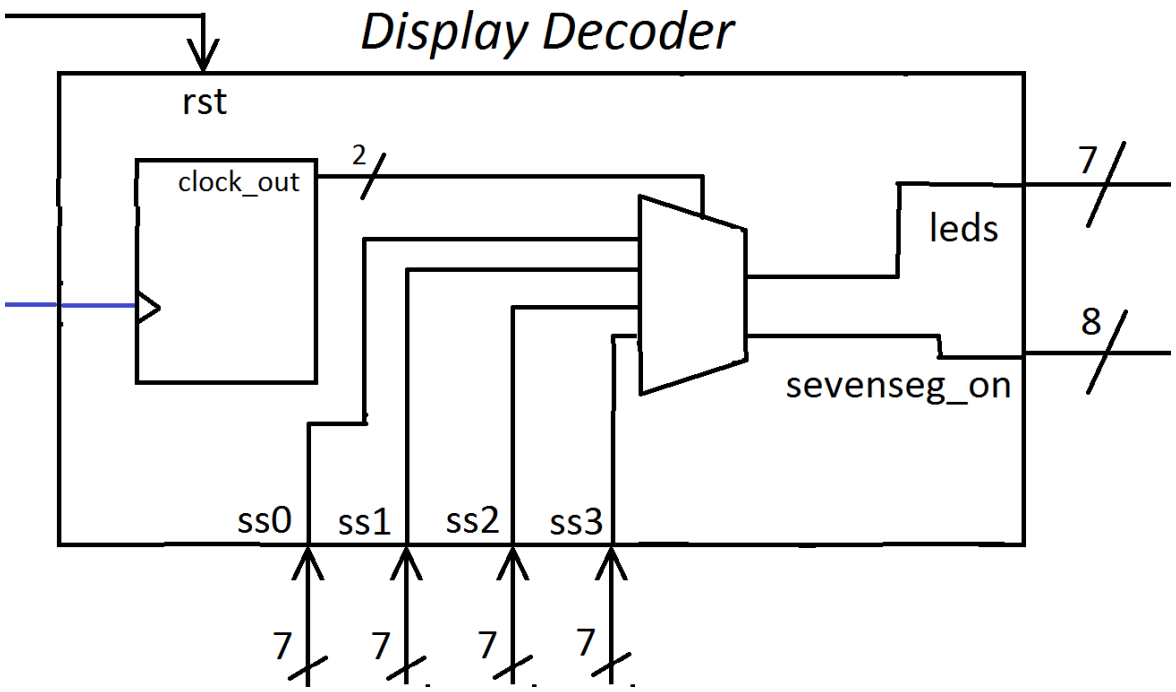
- 7-seg has limited amount of potential states
  - Due to this, we are using “9” to display a G note, an “8” for a B note, etc.

DISPLAY DECODER

-Implemented as a 7-seg serializer

-Internal clock divider

-Internal data selector



DEMO

https://youtu.be/yW7LucIZ39Q

CONCLUSIONS