UNSIGNED 2X2 MATRIX MULTIPLIER

ECE 2700 Final Project Presentation

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} e & f \\ g & h \end{bmatrix} = \begin{bmatrix} ae+bg & af+bh \\ ce+dg & cf+dh \end{bmatrix}$$

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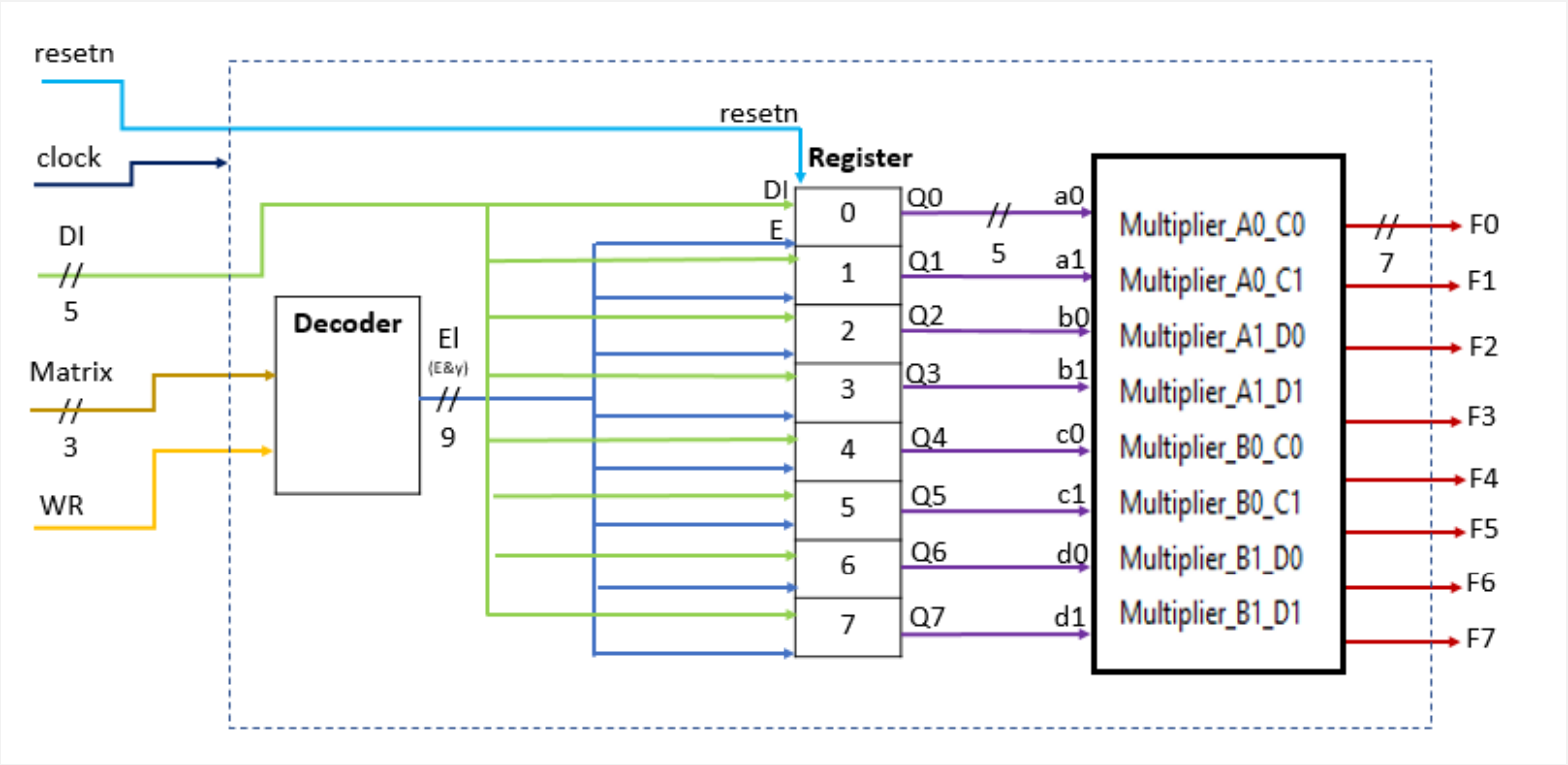
Input Circuit Schematic

Input from Switches

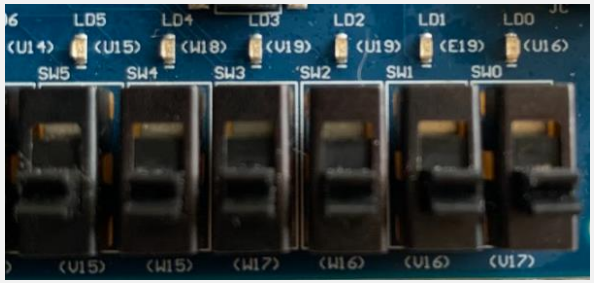


Output to Adders

Input Components

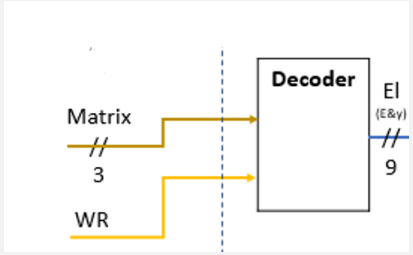
Switches

- (5) Switches for a 5-bit binary number
- (3) Switches for binary numbers representing each of the eight elements in the input matrices.



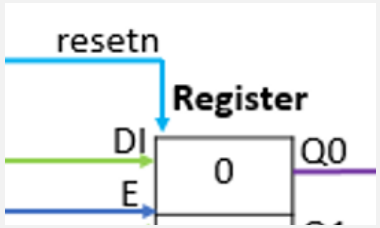
Decoder

- 2 to 1 Decoder that has a 3-bit input from the matrix selectors along with a logic signal representing the register write function. The inputs are pared with a 9-bit output that associates a memory slot in the registry with the matrix element selection.



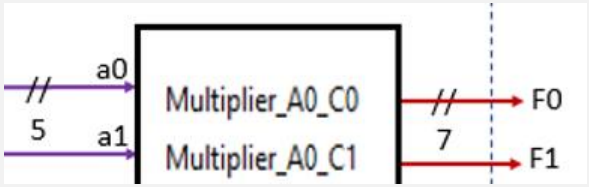
Registry

- (8) memory slots for each matrix element.
- Receives and stores the 5-bit binary input.

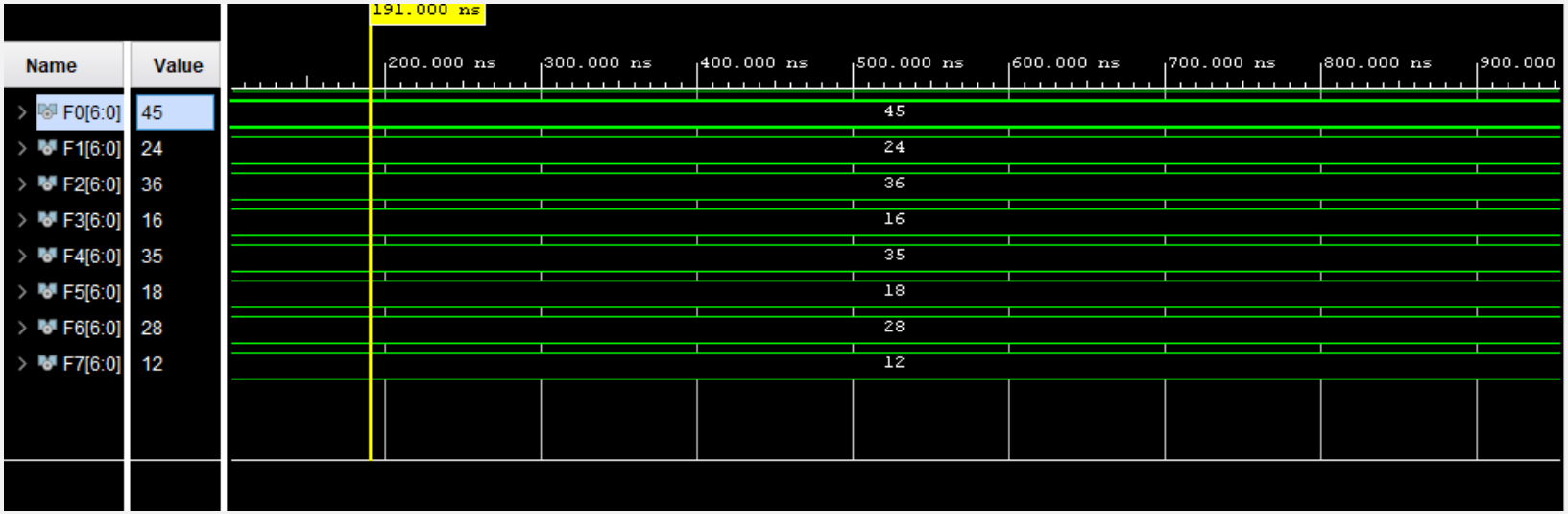


Multiplier

- Performs multiplication of registry data in accordance with a 2x2 matrix multiplication algorithm.

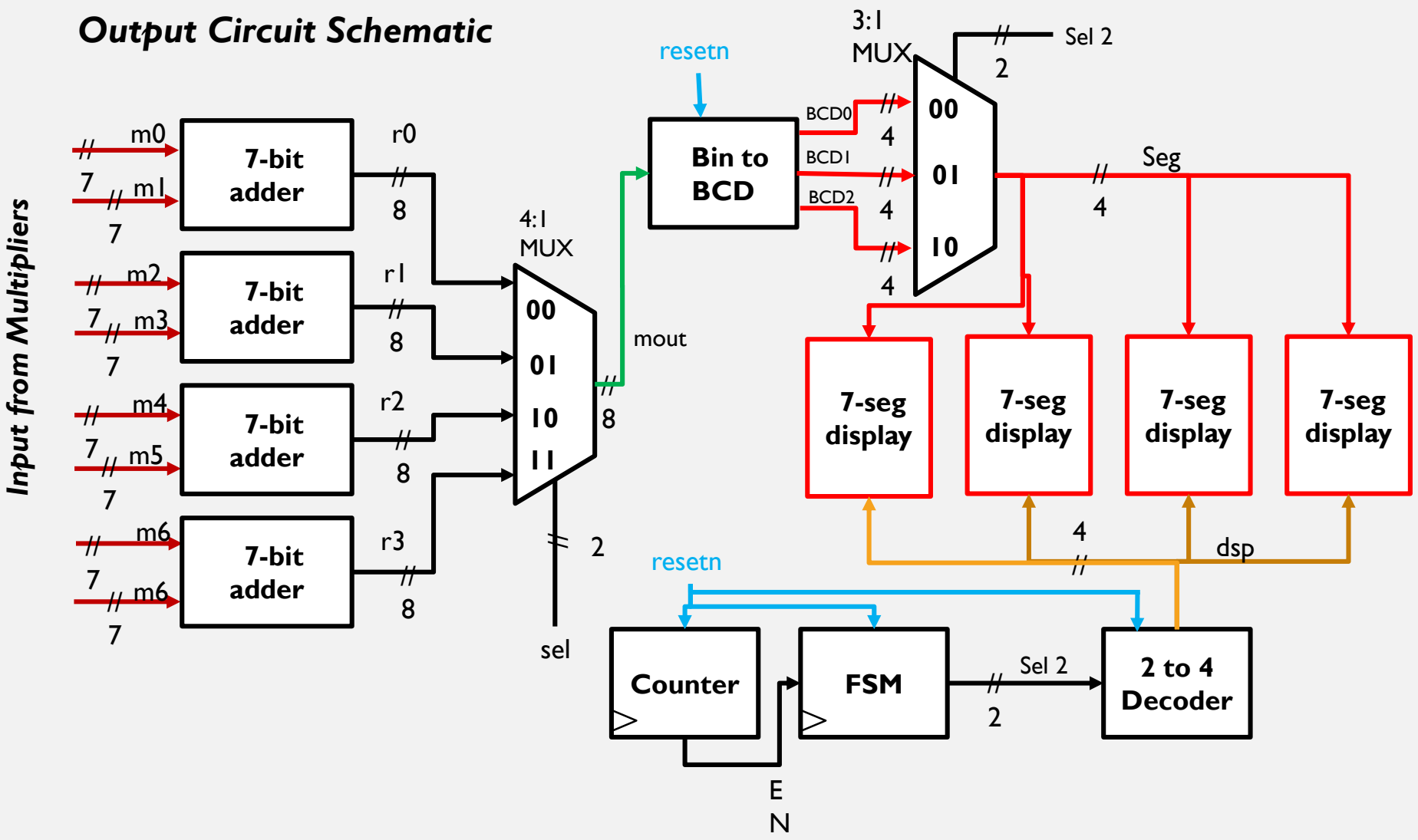


Multiplier Timing Diagram



$$\begin{bmatrix} 9 & 8 \\ 7 & 6 \end{bmatrix} x \begin{bmatrix} 5 & 4 \\ 3 & 2 \end{bmatrix} = (9*5)+(8*3),\ (9*4)+(8*2),\ (7*5)+(6*3),\ (7*4)+(6*2) =$$

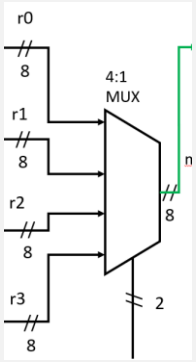
$$45 + 24,\ \ 36 + 16,\ \ 35 + 18,\ \ 28 + 12$$


Output Circuit Schematic
Input from Multipliers
m0
m1
7
7
7-bit adder
r0
8
m2
m3
7
7
7-bit adder
r1
8
m4
m5
7
7
7-bit adder
r2
8
m6
m6
7
7
7-bit adder
r3
8
4:1 MUX
00
01
10
11
2
sel
8
mout
resetn
Bin to BCD
BCD0
BCD1
BCD2
4
4
4
3:1 MUX
00
01
10
2
Sel 2
Seg
4
7-seg display
7-seg display
7-seg display
7-seg display
4
dsp
resetn
Counter
FSM
Sel 2
2
2 to 4 Decoder
E
N

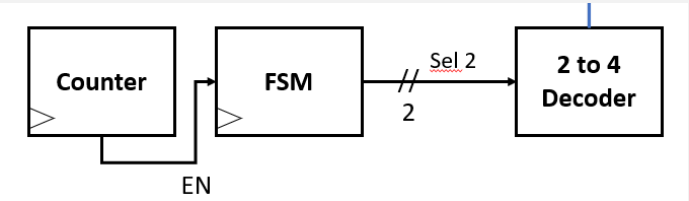
Output Components

7-bit Adders
- (4) Adders, one for each resultant matrix element
- Inputs two 7-bit unsigned signals each
- Output one 8-bit unsigned signal each

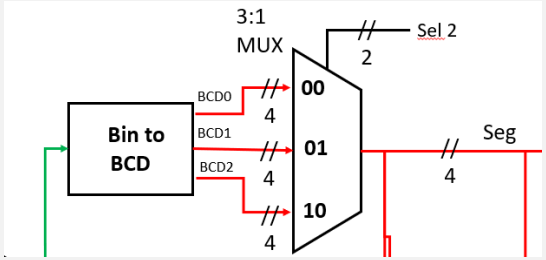
Multiplexers
- 4 to 1 MUX selects resultant matrix element displayed
- 3 to 1 MUX to control character displayed



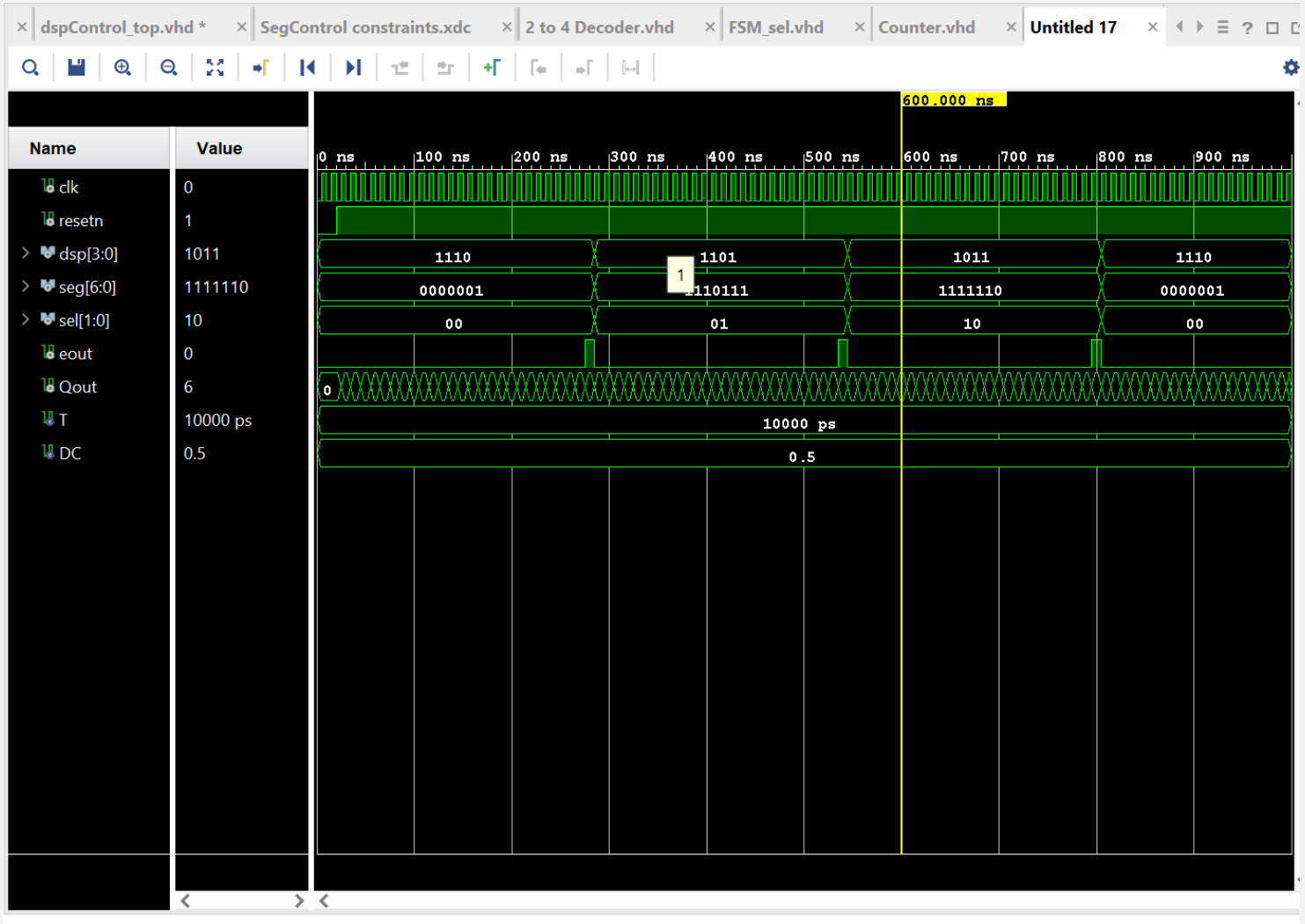
Finite State Machine
- (3) states, one for each 7-seg display used
- Input enable signal from counter (every 100us)
- Output "sel2" signal controlling serial 7-seg display



BIN to BCD Converter
- Input 8-bit 4 to 1 MUX output "mout"
- Output three 4-bit BCD signals
- One BCD signal for each digit to be displayed



Display Control Timing Diagram



Functionality Demonstration

Input Matrices

$$\begin{bmatrix} 9 & 8 \\ 6 & 5 \end{bmatrix} x \begin{bmatrix} 9 & 4 \\ 7 & 3 \end{bmatrix}$$

Output Matrix

$$\mathrm{R} = \begin{bmatrix} 137 & 60 \\ 89 & 39 \end{bmatrix}$$