Course Information

INSTRUCTOR	Daniel Llamocca
CONTACT INFO	email: llamocca@oakland.edu
OFFICE HOURS	Tuesday 2:00 to 4:00 pm @ Room EC-438, or by appointment Monday and Wednesday: 4:30 to 5:30 pm @ Room EC-562 (TA office hours)
LECTURES	Monday/Wednesday 5:30 pm - 7:17 pm @Room SFH-266 (South Foundation Hall)
LABORATORY	002: Monday 7:30 pm – 10:30 pm @ Room EC-562 003: Monday 12:00 pm -2:59 pm @ Room EC-562 004: Tuesday 12:00 pm -2:59 pm @ Room EC-562 005: Wednesday 12:00 pm -2:59 pm @ Room EC-562 TAs: Ekhlass Alkharabsheh emalkharabsheh@oakland.edu Prakruthi Jagadeesh pjagadeesh@oakland.edu Aishwarya Shitole aashitole@oakland.edu

COURSE CATALOG DESCRIPTION: ECE 2700 – Digital Logic Design (4 credits)

Boolean algebra; number systems and arithmetic, combinational logic circuits; synchronous sequential circuits; asynchronous sequential circuits; introduction to a hardware description language (HDL). With Laboratory. (Formerly ECE 278).
Prerequisite(s): EGR 240 or EGR 2400.

COURSE WEBPAGE

- The course material will be hosted on Moodle (moodle.oakland.edu). Grades will be periodically posted via this system.
- As a backup resource, the material will also be posted at: www.secs.oakland.edu/~llamocca/Fall2019_ece2700.html
- VHDL for FPGAs Tutorial: Available at the following permanent link: www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

TEXTBOOK:

- There is no required textbook. Students are encouraged to use the extra references.

EXTRA REFERENCES:

- Bryan J. Mealy, James T. Mealy, *Digital McLogic Design*, Free Range Factory, 2012.
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- Bryan Mealy, Fabrizio Tappero, Free Range VHDL, Free Range Factory, 2013
  - ✓ Free download: http://www.freerangefactory.org/books_tuts.html
- S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, 3rd ed., McGraw Hill, 2009. (suggested)
- Richard Haskell, Darrin M. Hanna, *Digital Design using Digilent FPGA Boards VHDL/Active-HDL Edition*, LBE Books, 2009.
- Peter J. Ashenden, The Designer's Guide to VHDL, 3rd ed., Elsevier, 2008.

COURSE OBJECTIVES

1. Design and analyze combinational and sequential logic circuits. (1)
2. Design and analyze finite state machines. (1)
3. Perform addition, subtraction, and multiplication in binary arithmetic. (1)
4. Describe memory operation and memory addressing. (1)
5. Describe digital circuits using VHDL and implement them on an FPGA. (1, 6)
6. Perform functional and timing simulation of a digital circuit described in VHDL. (1,6)
7. Describe how combinational and sequential components can be used to design a datapath and control unit for implementing digital systems. (1, 2)
8. Work in a team environment to design a digital system and communicate the results in a written report and an oral presentation. (1, 2, 3, 6)

ABET Course Outcomes:

1	2	3	4	5	6	7

GRADING SCHEME:

Homeworks:	15%	**Final Project:**	15%
Quizzes:	10%	**Midterm Exam**:	20% (October 16th, 5:30-7:17 pm)
Laboratory:	20%	**Final Exam**:	20% (December 9th, 7:00-10:00 pm)

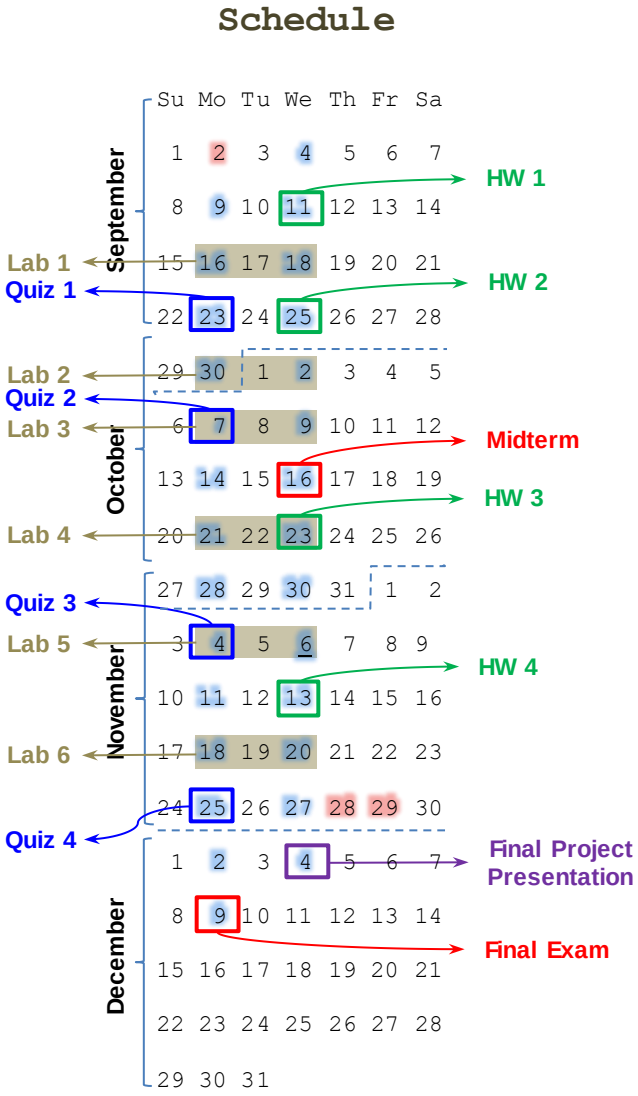
- **Homeworks:** Homework assignments are meant to strengthen your conceptual understanding of the topics. Completing homework assignments is a key component of this course as it will help students master the course material and prepare them for the exams.
  Homeworks will be posted according to the schedule (green rectangles). Students have one week to turn in the completed assignments in class. Late submissions are NOT accepted.

- **Quizzes:** They will have a duration of 20 minutes at the beginning of the class.

- **Exams:** Closed-books, closed-notes, in-class exams. The final exam will be a comprehensive test that will cover the whole syllabus. Students are not allowed to take the exams neither before nor after the exam date. Make-up exams are given *only* under extreme circumstances (e.g.: medical emergency, jury duty).

- **Laboratory:** This important component of the class will reinforce your understanding of the topics. There will be six (6) labs throughout the semester.
  TAs will be present every week during the regularly scheduled laboratory times. Students can work during those times or at any other time and place.
  Students have one week to complete the lab assignments and have them checked off by the TA.

- **Final Project:** Students will work in groups (up to 4) in a Final Project. Each group will prepare an oral presentation and submit a final report. Presentations will take place on December 4th.



GRADE ASSIGNMENT:

96-100	A	4.0
90-95	A-	3.7
85-89	B+	3.3
80-84	B	3.0
72-79	B-	2.7
66-71	C+	2.3
60-65	C	2.0
56-59	C-	1.7
53-55	D+	1.3
50-52	D	1.0
49 and below	F	0.0

LABORATORY MATERIALS

- **Hardware**: Nexys™ A7 FPGA Trainer Board - Option: A7-50T (you can also use the Nexys™-4 DDR Artix-7 FPGA Board)
  - ✓ To order: https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
    Go to: Get Academic Pricing ($171.75)

  If you do not plan to take ECE4710, you can use the Basys3 Trainer Board:
  - ✓ To order: https://store.digilentinc.com/basys-3-artix-7-fpga-trainer-board-recommended-for-introductory-users/
    Go to: Get Academic Pricing ($111.75)

- **Software**: Vivado HL Webpack Edition
  - ✓ To download: http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

OUTLINE OF TOPICS

Introduction to Logic Circuits	▪ Boolean Algebra ▪ Sum-of-Products and Product-of-Sums forms ▪ Logic Gates. Timing diagrams	
Optimized Implementation of Logic Functions	▪ Basic Techniques ▪ Karnaugh Maps ▪ Quine-McCluskey algorithm	
Implementation Technology	▪ Logic Levels, CMOS Logic gates ▪ Tri-state buffers, Transmission Gates ▪ Practical aspects: propagation delay, noise margin, hazards ▪ Programmable Logic Devices, Field Programmable Gate Arrays	
Number Systems and Computer Arithmetic	Unsigned integer numbers	Binary representation Octal and hexadecimal representation Addition and subtraction
	Signed integer numbers	Binary representation Addition and subtraction
	Multiplication of integer numbers	Array multiplier for unsigned numbers Multiplication of signed numbers
	▪ Binary Codes ▪ Introduction to Fixed-point arithmetic	
Combinational Circuits	Basic circuits	Multiplexers, De-multiplexers Decoders, Encoders, Comparators Code Converters: BCD to 7-segment, Gray to BCD, etc. Parity generators and parity checkers
	Complex circuits	Look-up Tables Arithmetic Logic Unit (ALU) Design Barrel shifter
Synchronous Sequential Circuits	Basic circuits	Flip flops and latches Registers, shift registers Parallel access shift registers: parallel-to-serial/serial-to-parallel conversion Counters: synchronous, BCD, Ring, Johnson Random Access Memory
	Finite State Machines (FSMs)	Moore and Mealy state Models Design Steps: State Diagram, State Table, State assignments. Algorithmic State Machine (ASM) charts
Introduction to Digital System Design	▪ Digital system (or special-purpose processor) components: Datapath circuit, Control Circuit ▪ Design examples: Small processor, shift-and-add multiplier, sequential divider.	

VHDL: For every topic, an aspect of VHDL description will be explored.

Introduction	▪ Design Flow: Design Entry, Functional Simulation, Mapping, Timing Simulation, Implementation ▪ Data Types ▪ VHDL Description: Logic Gates ▪ VHDL Testbench Generation
Concurrent Description	▪ Concurrent statements: 'with-select', 'when-else' ▪ Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux.
Behavioral Description	▪ Asynchronous processes ▪ Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux. ▪ Sequential statements: 'if-else', 'case', 'for-loop'
Structural Description	▪ Hierarchical design: Use of port-map, for-generate, if-generate. ▪ Examples: Adder, multiplier, Arithmetic Logic Unit, Look-up Table
Sequential Circuits	▪ Testbench: generating clock stimulus ▪ Asynchronous processes: Latches ▪ Synchronous processes: flip-flops, counters, registers ▪ Description of Finite State Machines
Parameterization	▪ Simple techniques ▪ Use of for-generate, if-generate.

CLASS POLICIES

- **Laboratory**: Students must be aware of their Laboratory section: 002, 003, 004, 005. This will be used to determine whether a student is late in their laboratory submission. Students are advised to attend on the day of their respective Laboratory Section. However, students can attend any other Laboratory Section if there is space available. Students will be able to complete a TA evaluation form at the end of the semester.

- **Academic conduct policy**: All members of the academic community at Oakland University are expected to practice and uphold standards of academic integrity and honesty. Academic integrity means representing oneself and one's work honestly. Misrepresentation is cheating since it means students are claiming credit for ideas or work not actually theirs and are thereby seeking a grade that is not actually learned. Academic dishonesty will be dealt with seriously and appropriately. Academic dishonesty includes, but it is not limited to cheating on examinations, plagiarizing the works of others, cheating on lab reports, unauthorized collaboration in assignments, hindering the academic work of other students.

- **Special Considerations**: Students with disabilities who may require special consideration should make an appointment with campus Disability Support Services, 106 North Foundation Hall, phone 248 370-3266. Students should also bring their needs to the attention of the instructor as soon as possible. For academic help, such as study and reading skills, contact the Academic Skills/Tutoring Center, 103 North Foundation Hall, phone 248 370-4215.

- **Add/Drops**: The university policy will be explicitly followed. It is the student's responsibility to be aware of deadline dates for dropping courses.

- **Attendance**: It is assumed that the students are aware of and understand the university attendance policy. Attendance is mandatory and maybe monitored. Students are responsible for all material covered in classes that they miss. There will be no excuses for being late to quizzes/exams.

- **Athlete Excused Absences**: Students shall inform the instructor of dates they will miss class due to an excused absence prior to the date of that anticipated absence. For activities such as athletic competitions whose schedules are known prior to the start of a term, students must provide their instructors during the first week of each term a written schedule showing days they expect to miss classes. For other university excused absences, students must provide the instructor at the earliest possible the dates that they will miss.

- **Special Circumstances:** The instructor should be notified as early as possible regarding any special conditions or circumstances which may affect a student's performance during the course timeframe (e.g., medical emergencies, family circumstances).

- **Cellphones**: A ringing cellphone going off during a lecture is disruptive to other students as well as the instructor. Students are strongly advised to set their cellphones to vibrate (not ringing) and leave the classroom discretely to answer the phone.