Multilingual Greeting Banner on 7-Segment Display

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Objective

- Implement logical circuit and FSM
- Create a multilingual sign
- Use switches to navigate between different languages

VHDL Code

- Components:
  - 1 ms counter
  - Decoder (3 to 32 and 3 to 8)
  - MUX (3 to 8 and 4 to 4)
  - Hex to 7-Seg
  - Top
  - FSM

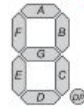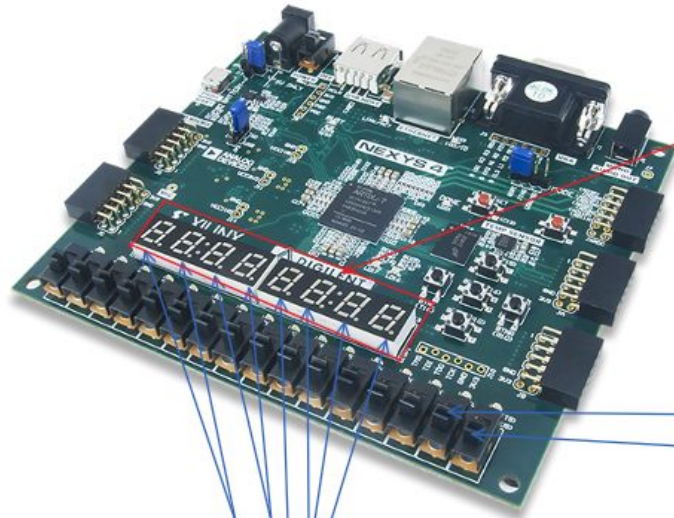Finite State Machine VHDL Code

```
-- FSM
Transitions: process (resetn, clock, E)
begin
        if resetn = '0' then -- asynchronous signal
                y <= S1; -- if resetn asserted, go to initial state: S1
        elsif (clock'event and clock = '1') then
                        case y is
                                when S1 => if E =  '1' then y <= S2; else y <= S1; end if;
                                when S2 => if E =  '1' then y <= S3; else y <= S2; end if;
                                when S3 => if E =  '1' then y <= S4; else y <= S3; end if;
                                when S4 => if E =  '1' then y <= S5; else y <= S4; end if;
                                when S5 => if E =  '1' then y <= S6; else y <= S5; end if;
                                when S6 => if E =  '1' then y <= S7; else y <= S6; end if;
                                when S7 => if E =  '1' then y <= S8; else y <= S7; end if;
                                when S8 => if E =  '1' then y <= S1; else y <= S8; end if;
                        end case;
                end if;
end process;

Outputs: process (y)
begin
        case y is
                when S1 => s <= "000";
                when S2 => s <= "001";
                when S3 => s <= "010";
                when S4 => s <= "011";
                when S5 => s <= "100";
                when S6 => s <= "101";
                when S7 => s <= "110";
                when S8 => s <= "111";
        end case;
end process;
```

Architecture

- Our top file is "Top"
  - ▷ This source contained the multiplexers, decoders, and the finite state machine.
- "My_genpulse" is a component of "Top".
  - ▷ This source is the 1 ms counter.
- "Hex2sevenseg" is a component of "Top".
  - ▷ This source determines which of the 7 segments will display in order to create a letter.

External Interface

*segs[0]-segs[6] correspond with segments g to a, respectively
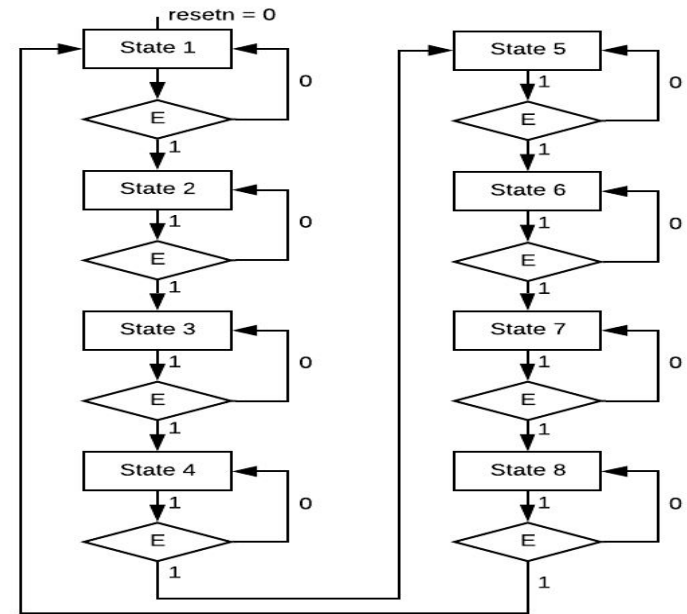
sw[0] & sw[1]

*Decides which message is going to be displayed on the 7-segment display
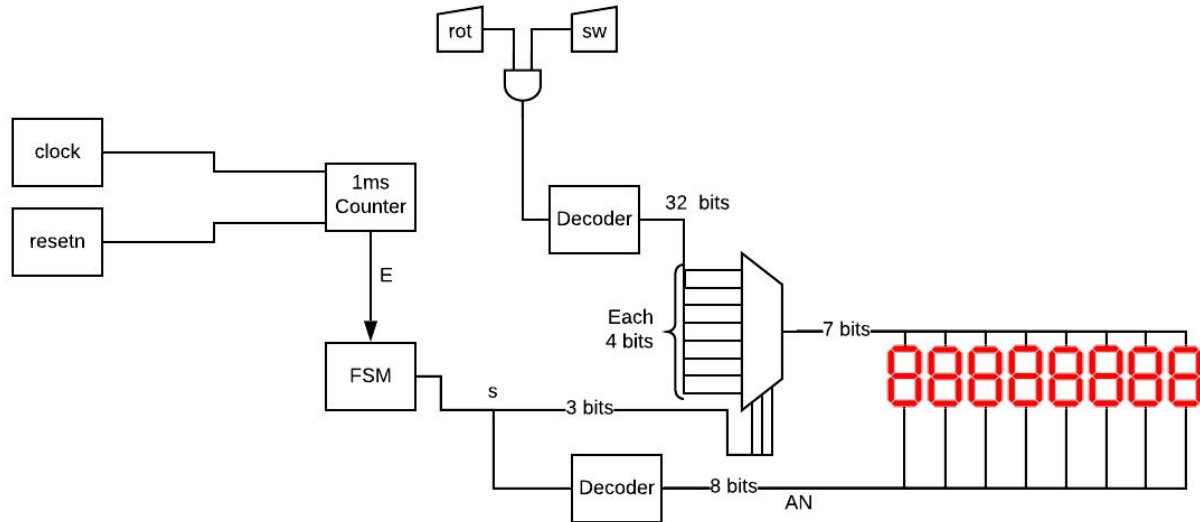
AN[0]-AN[7]

*7-segment display is determined through the selector switches sw[0] and sw[1]

Finite State Machine

- States:
  - S1-S8
  - Based off clock speed (1ms)
  - When clock is high, change states
  - Used to control:
    - Anodes
    - Letters to display

Block Diagram

Demonstration

English (00)

Spanish (01)

Chinese (10)

Arabic (11)

Conclusion

- Used learned knowledge of VHDL to code circuit
- Able to successfully implement multi-language banner on 7-Segment Display
- Improvements:
  - Could be scrolling
  - External user-input for custom message