# Banner on a Seven Segment Display

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***The purpose of this project is to program an FPGA board to display a message (pre-determined) scrolling across eight seven segment displays using the information learned throughout the semester. It was found that this is best implemented using a finite state machine to control the seven-segment displays while an additional system of registers outputs a message to them via multiplexers. The user has the ability to select between two messages to display.***

## I. INTRODUCTION

In this project, a circuit is to be designed in Xilinx Vivado 2018 that has a message scroll across a series of eight seven-segment displays. The core theory behind this project is using a clock pulse and having each seven segment display flash a certain light pattern at a time. The human eye can be "tricked" into seeing a message scrolling across seven segment displays. With this being stated, the concepts of finite state machines and synchronous circuits learned in the course will be very valuable in the development of this project. In addition, the development of components in laboratory assignments will be useful to implement. Such circuits include seven segment display drivers, decoders, finite state machines, and multiplexers, to name a few. This project is useful in all applications that display data on seven segment displays due to its efficiency, since out of eight seven segment displays, only one display is activated, which saves energy. This is used in many applications, from gasoline pumps to billboards.

## II. METHODOLOGY

### A. Design

The circuit to be implemented will consist of two counters, a finite state machine, eight 3-bit shift registers, a 2 to 1 multiplexer, and an 8 to 1 multiplexer. The circuits will also use a modified version of the hex to 7-segment display decoder module used in previous labs so that it will be able to decode letters instead of integers. The purpose of the 2 to 1 multiplexer and eight shift registers will be to feed the character inputs in hexadecimal form to the 3-bit shift register as shown in the circuit diagram, in a scrolling fashion. The finite state machine will be used to control which 7-segment display at a 1 millisecond period. This will be used to give the illusion to the user that multiple displays are being shown at the same time.

### B. Implementation

*(See block diagram on second page)* The circuit was implemented in VHDL using Xilinx Vivado 2018 which can provide synthesis and implementation tools so the circuit can be implemented on a Nexys A7 FPGA board. The software side of the project consists of program files to describe each module in the circuit, and a constraints file to directly tie the I/O of the circuit to the FPGA components. No test bench circuit was required for this project, as it was tested on the board immediately after successfully passing synthesis and implementation.The sections of the circuit that "tricks" the human eye into seeing multiple images is derived from an example from the ECE 2700 class notes, but altered to support eight 7-segment displays instead of four. obtained from the example projects that are available on Moodle, but modified using generics to work at different speeds. For the "shiftRAM" module responsible for storing the letters and their positions on the display, a custom datatype was needed to be created called "bus_array" in order to store an array of STD_LOGIC_VECTORs. This custom "bus_array" data type greatly simplifies and improves the readability of the VHDL code.

## III. EXPERIMENTAL SETUP

VHDL was used to provide a description of the circuit being used in the experiment which was then simulated via software in Xilinx Vivado 2018. After this step, the circuit's outputs was bound to the 7- segment display outputs in accordance to the constraints file for the Nexys A7 board. Finally, after performing the synthesis and implementation steps in Vivado, the bit-stream for the program was generated and downloaded to the FPGA board and tested. The user has access to two switches. One that determines the message he or she would like to display and the other that toggles between loading the message onto the display and shifting it across the display.

## IV. RESULTS

The expected output of the circuit was two messages ("HELLO" and "ECE2700") successfully scrolling across the set of seven-segment displays. These messages were switched using a switch on the FPGA to toggle between them. The load and shift inputs also worked as expected. Some additional features that could be added to this project include adding more registers to the circuit to allow longer messages to be stored as well as an input that give the user the ability

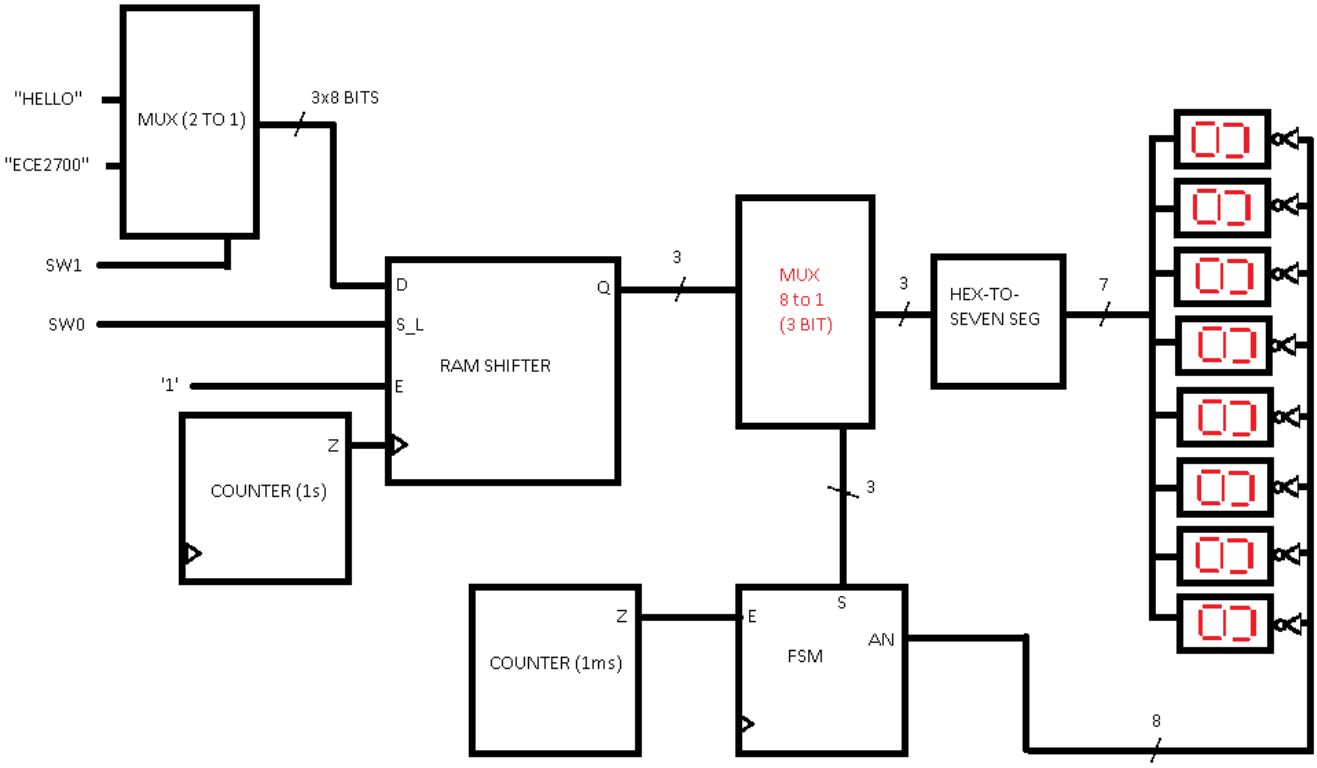
to adjust the scrolling speed of the message across the display.

## References

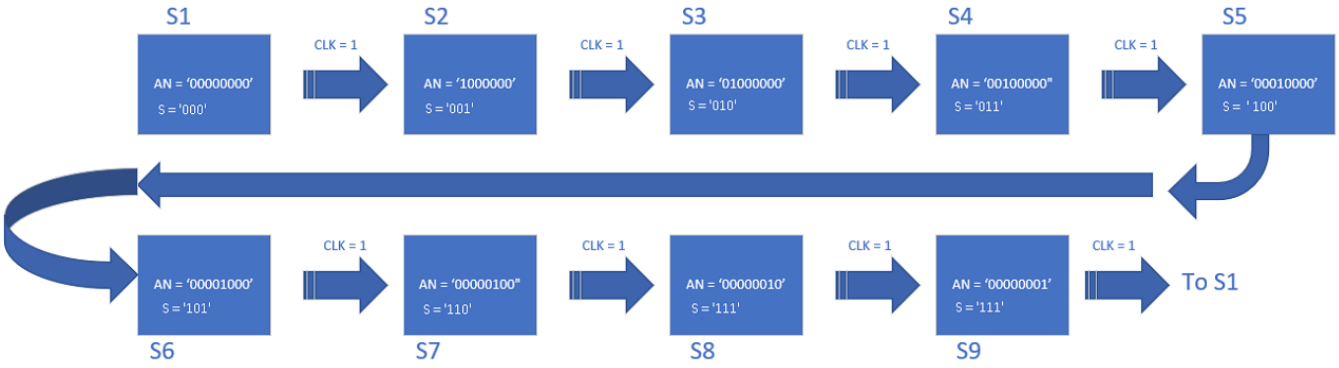

*[1] Llamocca, Daniel. "DIGITAL SYSTEM DESIGN VHDL Coding for FPGAs]." RECRLab, Electrical and Computer Engineering Department, Oakland University, www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html.*

*[2] "Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics." Xilinx.com, Xilinx, Inc., 13 Apr. 2017, www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_ Sheet.pdf*


Top Level Circuit Diagram



FSM anode Diagram




RAMshifter Module Diagram