Digital Stopwatch in VHDL

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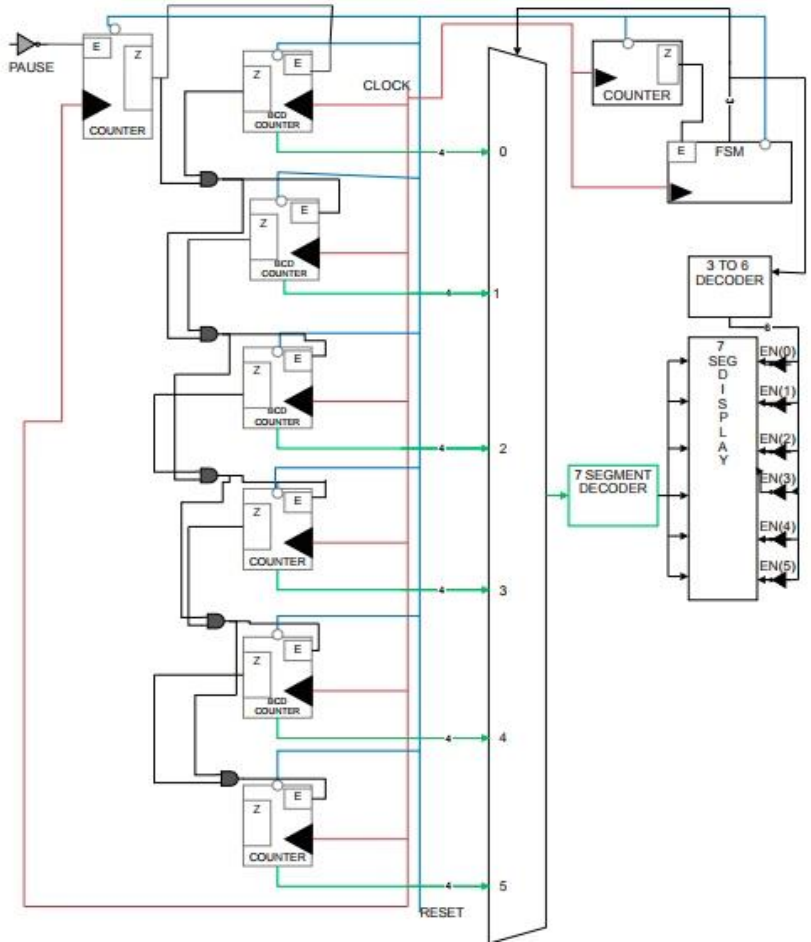
Objectives

- The objective of this project was to create a Stopwatch/Timer that is capable of displaying minutes, seconds, and hundredths of seconds on a seven-segment display.
- The user would be able to interact through the implementation of a pause, start, and reset functionality on the FPGA

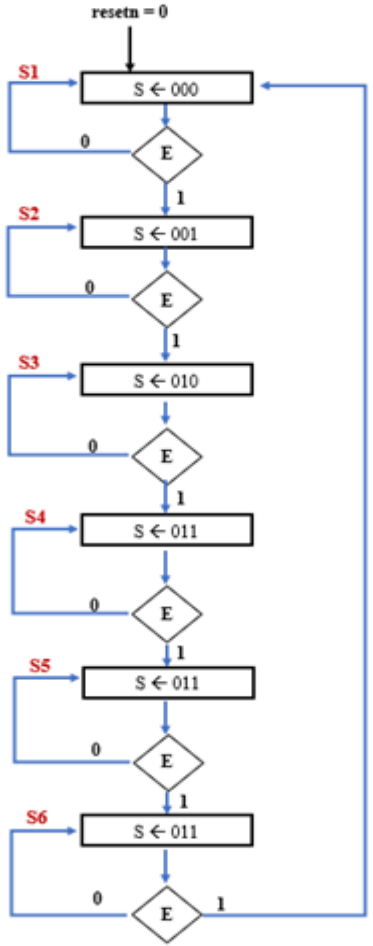
The Flowchart includes:

- Two counters
- A Multiplexer
- 2 Counter Modulo-6
- 4 Counter Modulo-10
- A 3-to-6 Decoder
- A Seven Segment Decoder
- A Final State Machine



FInal State Machine Diagram

- The final state machine was used to regulate what would be input to the 3-to-6 decoder, and thus be displayed on the seven-segment display.



Counters

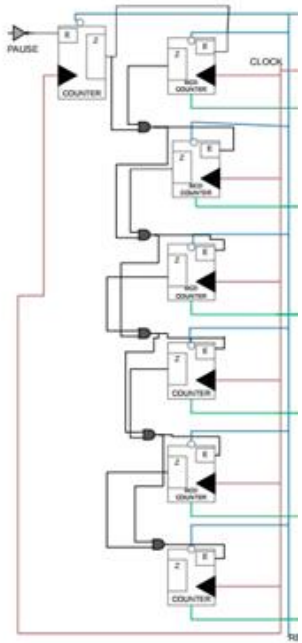
- **Clock Counters**

  The clock counters were used to regulate the signal to be output every 0.01 seconds and every 0.001 seconds

- **2 Modulo 6 and 4 Modulo 10 Counters**

  The modulo-6 counter was used to take in the signals of the first three BCD counters. It’s range covers digits 0-5.

  The modulo-10 counter was used to take in the signals of the first last BCD counter



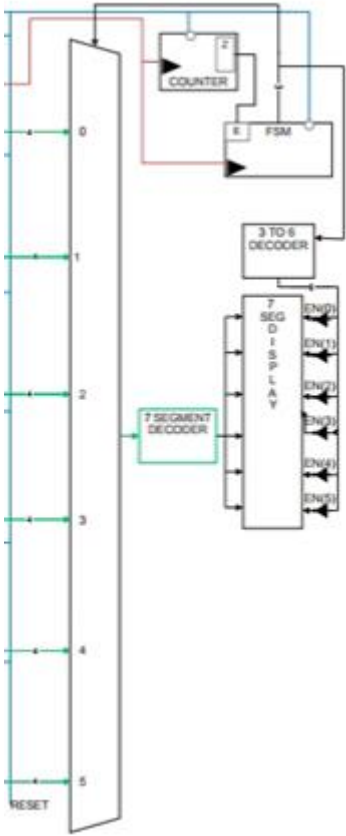
Decoders

- **3-to-6 Decoder**

A 3-to-6 decoder was used because only six digits of the seven-segment decoder were needed to display the timer/stopwatch output as its range is from 00:00:00 to 59:59:99.

- **Seven-Segment Decoder**

A seven-segment decoder was used to take in the output of the multiplexer and send it to the seven-segment display



Conclusions

Challenges

- **Using proper counters**
  - **Switched from BCD and Modulos to a Genpulse**
- **Troubleshooting**

Takeaways

- **Better understanding of VHDL**
- **Problem-solving skills**

Demonstration of Stopwatch

We will now demonstrate the final implementation of our stopwatch program .