# Light Intensity Measuring Device

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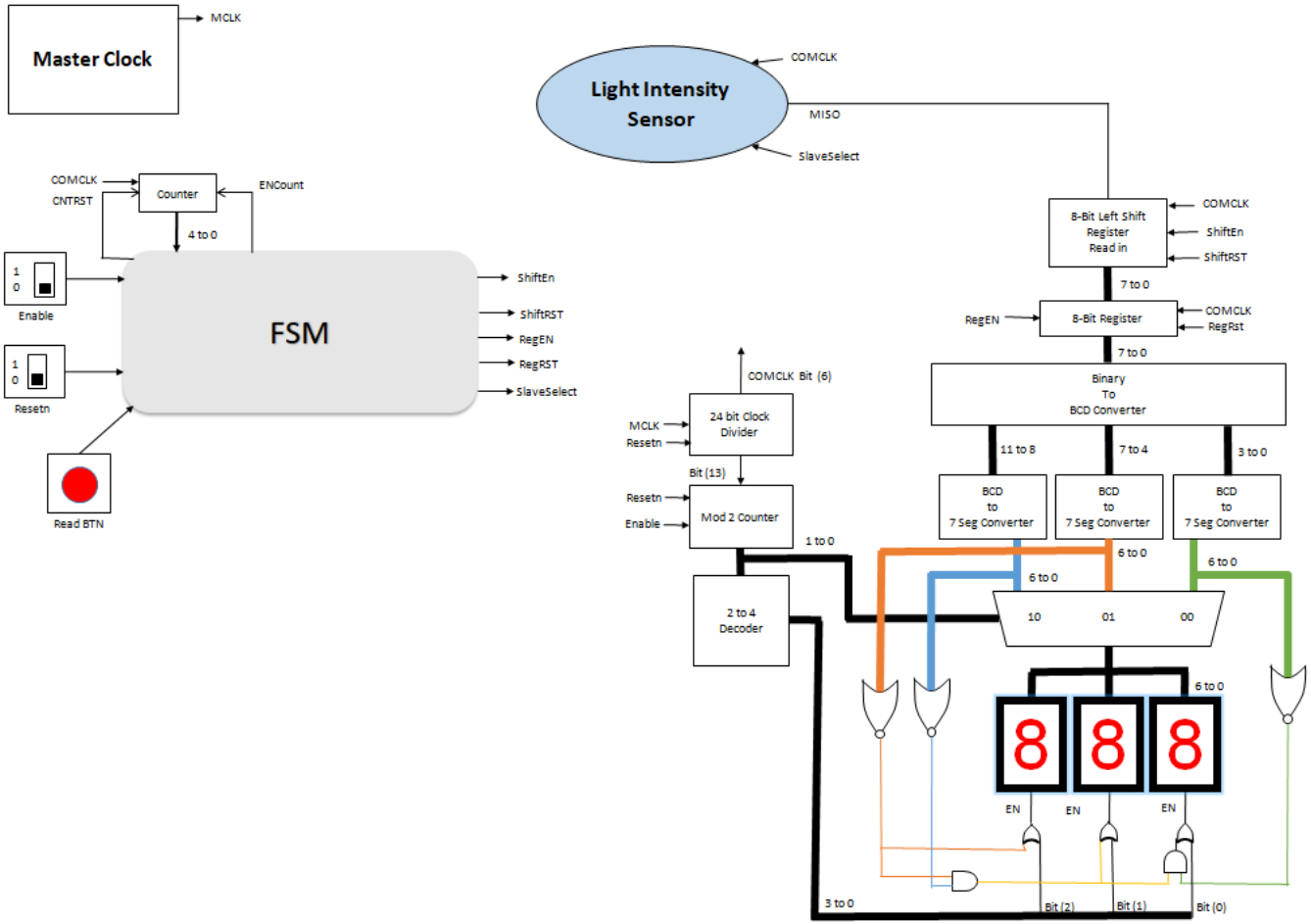
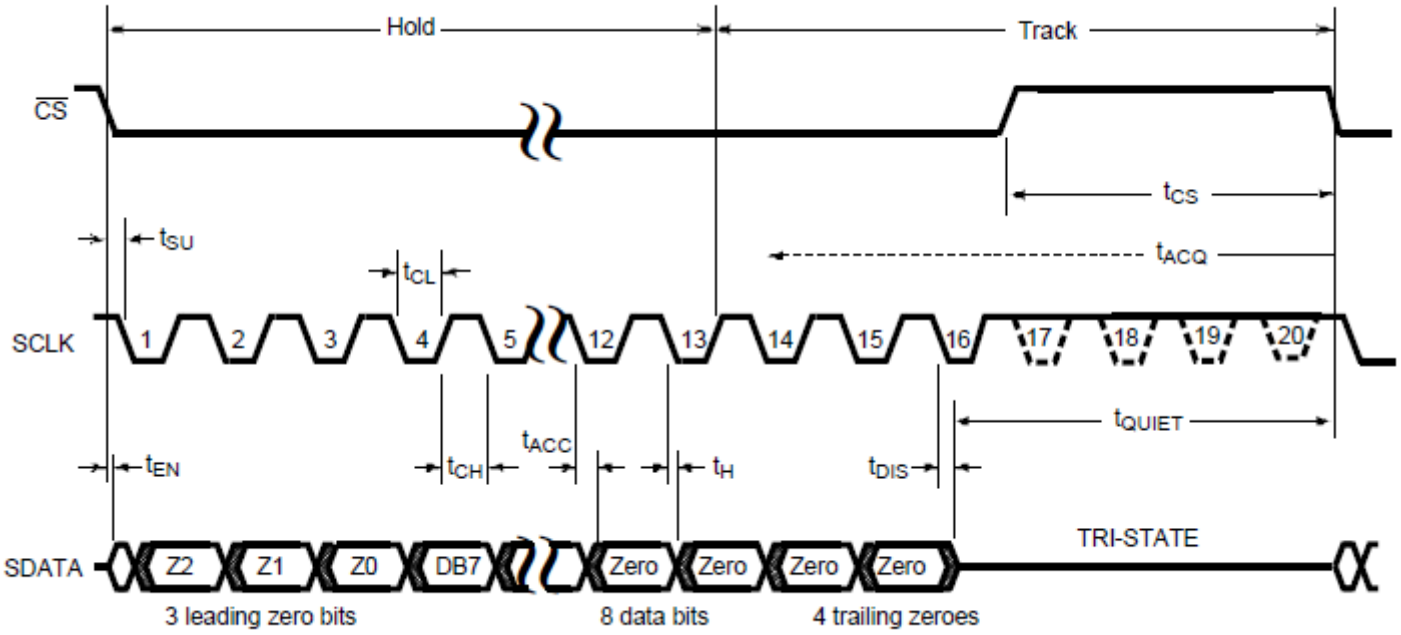
# Objective

- The objective for this project is to design and implement a **light intensity measuring device** on a NEXY-DDR board using VHDL.
- Key Features:
  - Light intensity displayed in values from 0 to 255 on seven segment display.
  - Light intensity values also represented in binary across LEDS on board.

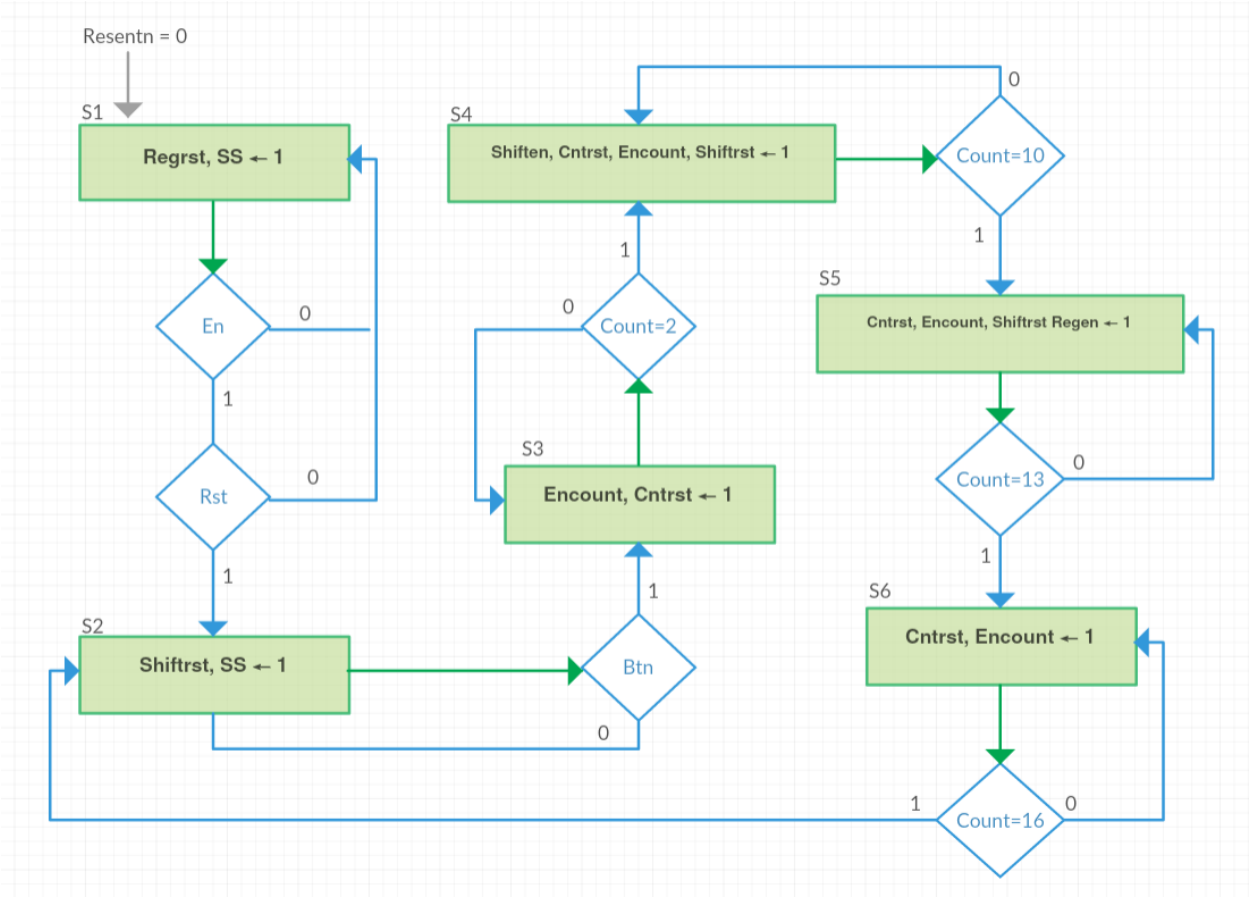
# Block Diagram



# PMOD ALS – SPI Timing Diagram



# State Diagram



# FSM

(1)

```
if resetn = '0' then y <= S1;
   elsif (clk'event and clk = '1') then
       case y is
           when S1 =>
           if En = '1' then y <= S2; else y <= S1; end if;

           when S2 =>
           if btn = '1' then y <= S3; else y <= S2; end if;

           when S3 =>
           if cycle = "00010" then y <= s4; else y <= S3; end if;

           when S4 =>
           if cycle = "01010" then y <= s5;  else y <= S4; end if;

           when S5 =>
           if cycle = "01101" then y <= s6; else y <= S5; end if;

            when S6 =>
            if cycle = "10000" then y <= s2; else y <= S6; end if;


           end case;

       end if;
```

(2)

```
Outputs: process (y)

begin

shiften <= '0';
cntrst <= '0';
encount<= '0';
shiftrst <= '0';
regen <= '0';
regrst <= '0';
slaveselect <= '1';

 case y is

 when S1 =>

 shiften <= '0';
 cntrst <= '0';
 encount<= '0';
 shiftrst <= '0';
 regen <= '0';
 regrst <= '1';
 slaveselect <= '1';
```

(3)

```
when S2 =>

shiften <= '0';
cntrst <= '0';
encount<= '0';
shiftrst <= '1';
regen <= '0';
regrst <= '0';
slaveselect <= '1';

when S3 =>

shiften <= '0';
cntrst <= '1';
encount<= '1';
shiftrst <= '1';
regen <= '0';
regrst <= '0';
slaveselect <= '0';

when S4 =>

shiften <= '1';
cntrst <= '1';
encount<= '1';
shiftrst <= '1';
regen <= '0';
regrst <= '0';
slaveselect <= '0';
```

(4)

```
when S5 =>

shiften <= '0';
cntrst <= '1';
encount<= '1';
shiftrst <= '1';
regen <= '1';
regrst <= '0';
slaveselect <= '0';

when S6 =>

shiften <= '0';
cntrst <= '1';
encount<= '1';
shiftrst <= '0';
regen <= '0';
regrst <= '0';
slaveselect <= '0';

   end case;
   end process;
end behavioral;
```