ECE 2700 Final Design Project

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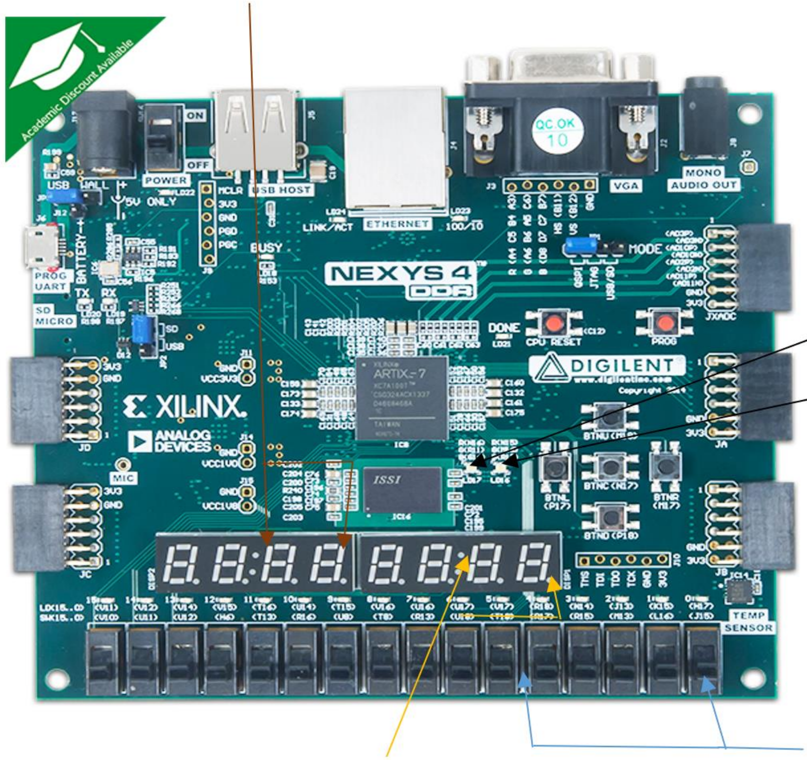
Traffic Light Controller

Anodes 5 and 4 on seven segment display

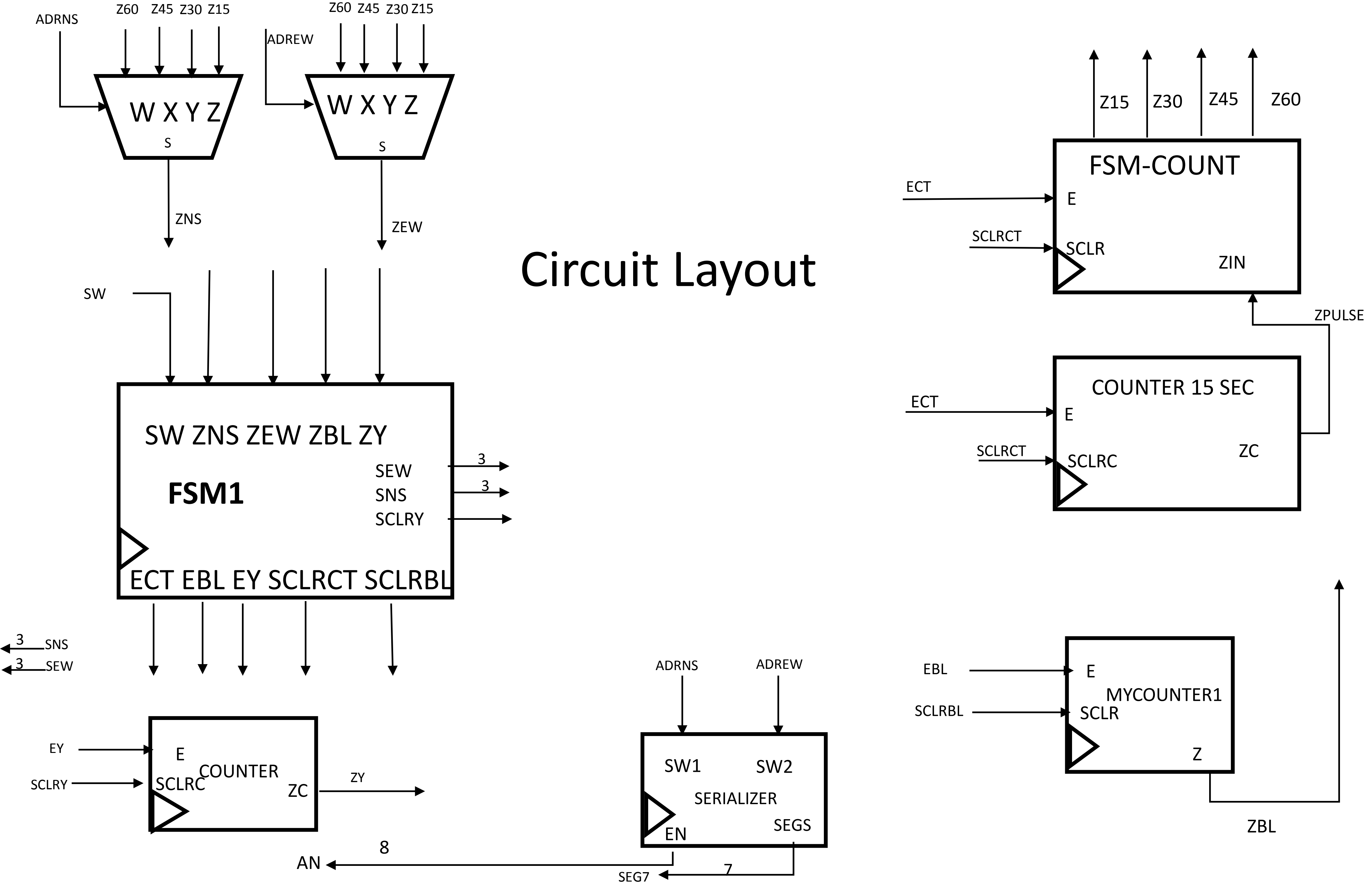


Tri-color LEDs, (traffic lights, East-West being rightmost and North-South being leftmost

Switches SW4 down to SW0, where user defines green light time and can decide operation of traffic light controller

Anodes 1 and 0 on seven segment display

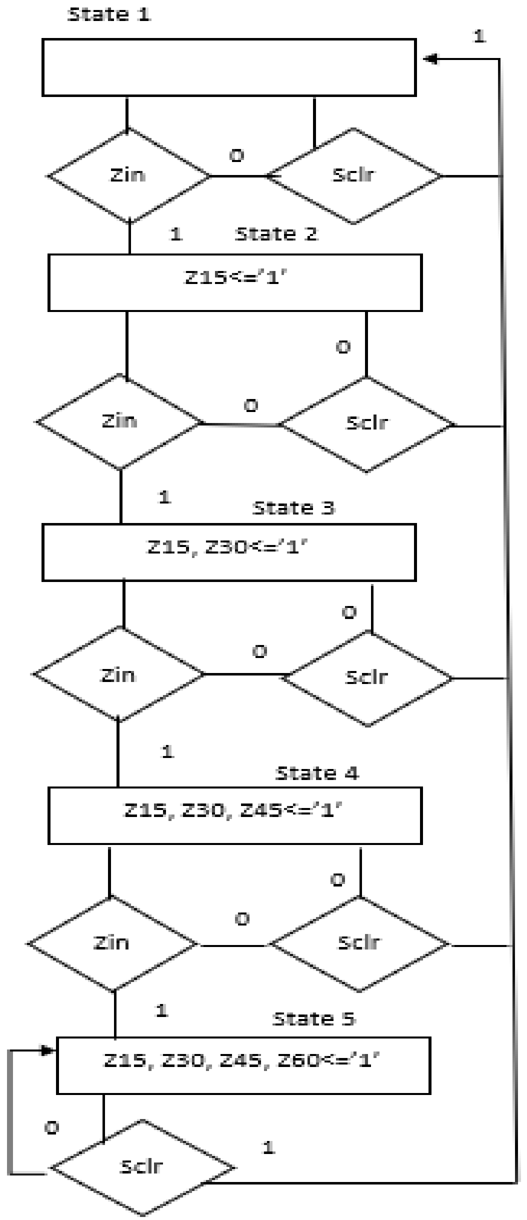
Circuit Layout

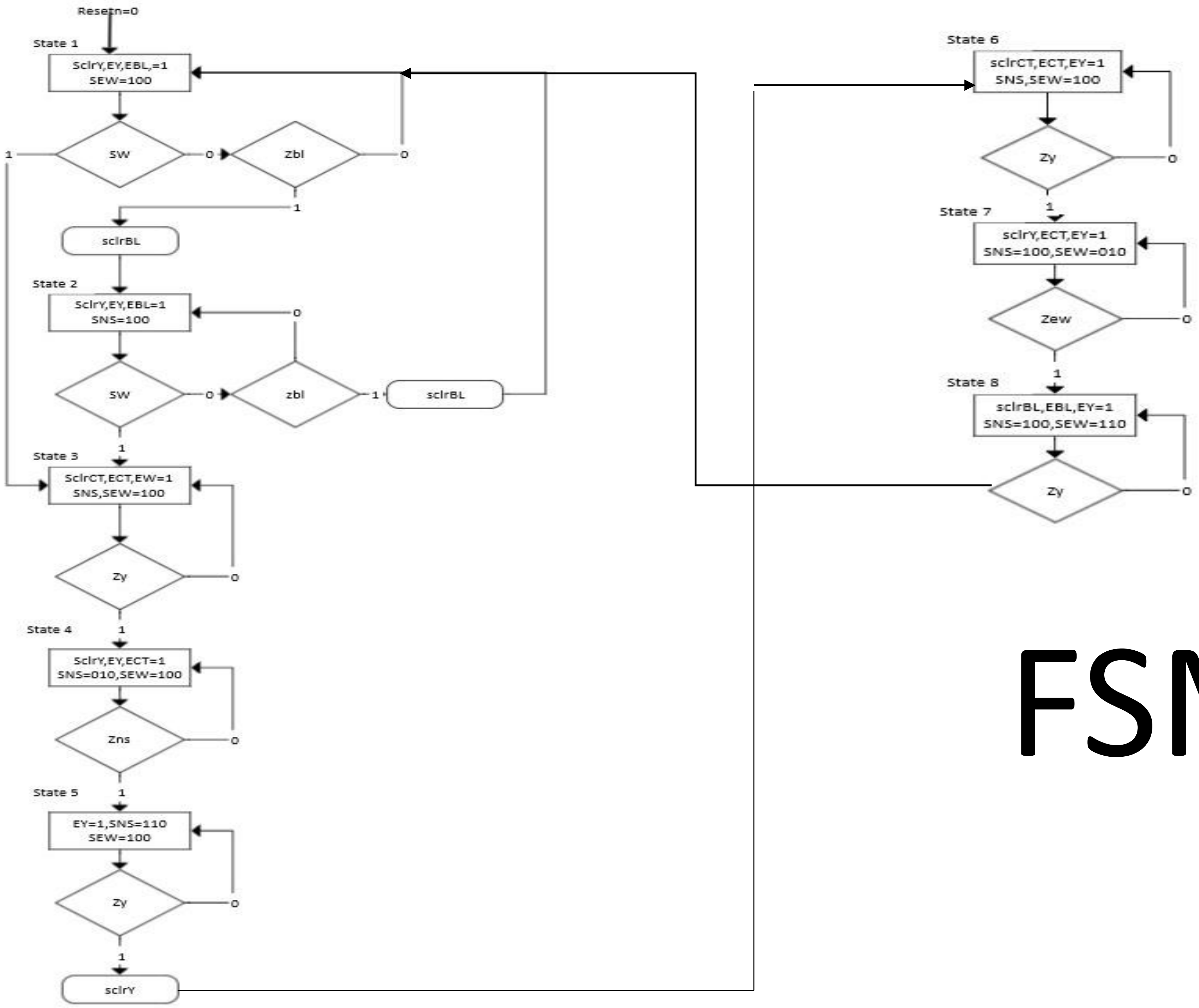


Top level description

- The Traffic Light Controller top file is composed of eight individual components.
- The main ‘brain’ of this traffic light controller is called FSM1,it provides direction and order to all other components of the circuit.
- The data path is then composed of two multiplexers, four counters, and the Serializer. These components make the traffic light controller operation possible.
- At the top level the inputs/outputs consist of: switch SW, this switch enables the user to choose between day or night traffic operations, switches ADREW and ADRNS, these switches allow for the user to define a particular amount of time (15,30,45,60)seconds that a green light will stay green for, as well as provide information to the serilalizer, which then allows for those times to be displayed on the 7-segment displays. The signals SNS and SEW represent the correct combinations of red, green, and blue in order to obtain red, yellow, and green from the tri-color LEDs. The signal SEG7 indicates the information that the 7-segment displays will show and the signal AN directs that information to display on the correct digit. (resetn and clock signals are implied here).

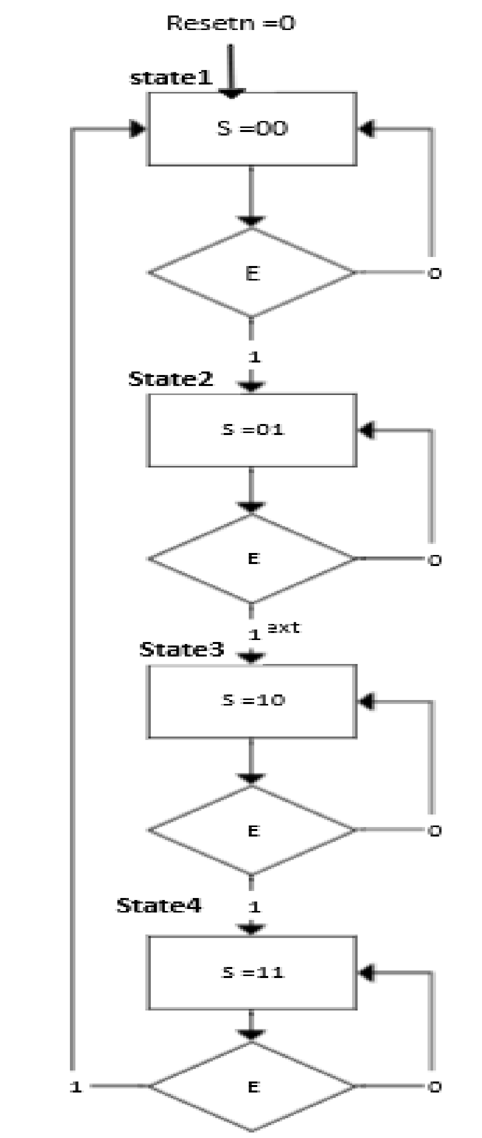
FSM_Count


State 1
1
Zin
0
Sclr
1
State 2
Z15<='1'
0
Zin
0
Sclr
1
State 3
Z15, Z30<='1'
0
Zin
0
Sclr
1
State 4
Z15, Z30, Z45<='1'
0
Zin
0
Sclr
1
State 5
Z15, Z30, Z45, Z60<='1'
0
Sclr
1


Resetn=0
State 1
SclrY,EY,EBL,=1
SEW=100
SW
Zbl
sclrBL
State 2
SclrY,EY,EBL=1
SNS=100
SW
zbl
sclrBL
State 3
SclrCT,ECT,EW=1
SNS,SEW=100
Zy
State 4
SclrY,EY,ECT=1
SNS=010,SEW=100
Zns
State 5
EY=1,SNS=110
SEW=100
Zy
sclrY
State 6
sclrCT,ECT,EY=1
SNS,SEW=100
Zy
State 7
sclrY,ECT,EY=1
SNS=100,SEW=010
Zew
State 8
sclrBL,EBL,EY=1
SNS=100,SEW=110
Zy

FSM_1

Serializer




```
-- Counter: 0.001s
gz: my_genpulse generic map (COUNT => 10**5)
    port map (clock => clock, resetn => resetn, E => '1', z => E);

   with SW1 select
   D <= "0001" when "00",
     "0011" when "01",
     "0100" when "10",
    "0110" when others;

   with SW1 select
    C <= "0101" when "00",
      "0000" when "01",
      "0101" when "10",
     "0000" when others;

   with SW2 select
     B <= "0001" when "00",
       "0011" when "01",
       "0100" when "10",
      "0110" when others;

    with SW2 select
      A <= "0101" when "00",
        "0000" when "01",
        "0101" when "10",
       "0000" when others;

with s select
        ENt <= "11111110" when "00",
               "11111101" when "01",
               "11101111" when "10",
               "11011111" when "11",
               "11111111" when others;

with s select
    omux <= A when "00",
            B when "01",
              C when "10",
              D when others;
```

RGB Leds constraints and 3 bit color representation

```
set_property -dict { PACKAGE_PIN R12   IOSTANDARD LVCMOS33 } [get_ports { SEW[0] }]; #IO_L5P_T0_D06_14 Sch=led16_b
set_property -dict { PACKAGE_PIN M16   IOSTANDARD LVCMOS33 } [get_ports { SEW[1] }]; #IO_L10P_T1_D14_14 Sch=led16_g
set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { SEW[2] }]; #IO_L11P_T1_SRCC_14 Sch=led16_r
set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { SNS[0] }]; #IO_L15N_T2_DQS_ADV_B_15 Sch=led17_b
set_property -dict { PACKAGE_PIN R11   IOSTANDARD LVCMOS33 } [get_ports { SNS[1] }]; #IO_0_14 Sch=led17_g
set_property -dict { PACKAGE_PIN N16   IOSTANDARD LVCMOS33 } [get_ports { SNS[2] }]; #IO_L11N_T1_SRCC_14 Sch=led17_r
```

Red (R)	Green (G)	Blue (B)	Resulting color
0	0	0	black
0	0	1	blue
0	1	0	green
0	1	1	cyan
1	0	0	red
1	0	1	magenta
1	1	0	yellow
1	1	1	white