7 Segment Display Banner

"Go Grizzlies"

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Abstract *– To design and implement a digital circuit that will perform the simple task of cycling a pre-determined message across a NEXYS 4 7 segment display array. This is accomplished using knowledge gained during the 2017 fall semester digital logic design course including theory of FSM design and VHDL and Verilog programming languages.*

I. Introduction

Our group decided upon designing a digital circuit that will take a preprogrammed message, in our case "Go Grizzlies" and cycle the message across the NEXYS 4 7 segment displays.

This project allowed our group to display what we have learned during our time spent in this class. This project contained shift registers, decoders, finite state machine counters, clock dividers, pulse generators, MUX and specific control over the analog displays.

We used code and information gained from the other labs of the semesters and applied them in a meaningful way to display a message that shows pride in our school.

II. Methodology

A. Design

As a group we decided that we wanted to do a simple but effective project that allowed us to display what we have learned this semester. We agreed upon a 7 segment display banner. The initial design was done by drawing out a flow chart to organize our thoughts and to outline the generic path the circuit needed to follow to accomplish our goals. This design used the NEXYS 4 onboard clock as our main outside input. By utilizing a 1 millisecond pulse generator and a 0.5 second clock divider we were able to use this on board clock to slow down the information so that it would be visible to the naked eye. The 0.5 second signal controls our message by displaying characters tied to one of 16 lines that are output of a 4 bit counter. This information is stored and shifted using 8 shift registers. The MUX which is controlled ultimately by the 1 millisecond pulse generator through a 3-8 decoder chooses which information on the registers to be synchronized with the 7 segment display.

B. Implementation

By following our flow chart outline and using assets available to us such as the TA's and Professor. We were able to design the components of our circuit and implement them in our design. Implementations of early messages were halted by the limiting restrictions caused by using a 7 segment display, we were forced to think of an engaging message that would be readable using a 7 segment display.

III. Experimental Setup

We tested the behavioral simulation of our project using Vivado 2017. By creating a relevant test bench for simulation we were able to see how the signals were being translated through the circuit and how our design would perform before writing it to the NEXYS 4 hardware.

IV. Results

We were able to successfully implement our design. The challenges that we experienced were mainly due to timing issues regarding the 4 bit counter. We were able to overcome these challenges by meeting with Professor Llamocca and reducing the speed of the counter down to 1 millisecond.

Conclusions

This project was similar to most of the labs we worked on as a class. This project allowed us to implement many different components we built throughout the semester into a way that allowed us to create our own vision and troubleshoot it until it worked properly.

References

[1] Llamocca, D. *VHDL Coding For FPGAs.* Retrieved from http://www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html

Figure. 1 7 Segment Display Restrictions

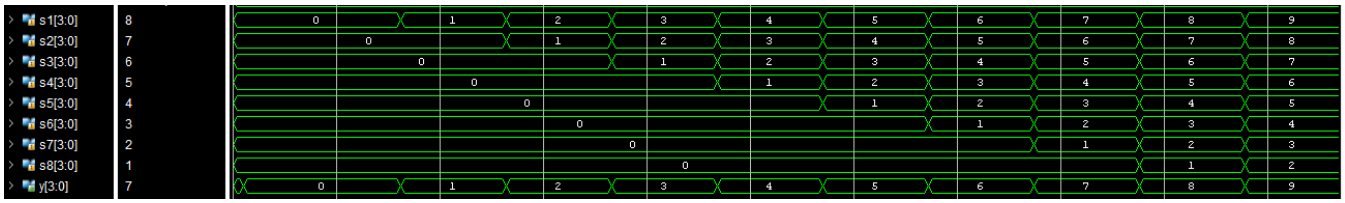

Figure 2. Shift Register Functionality Simulation

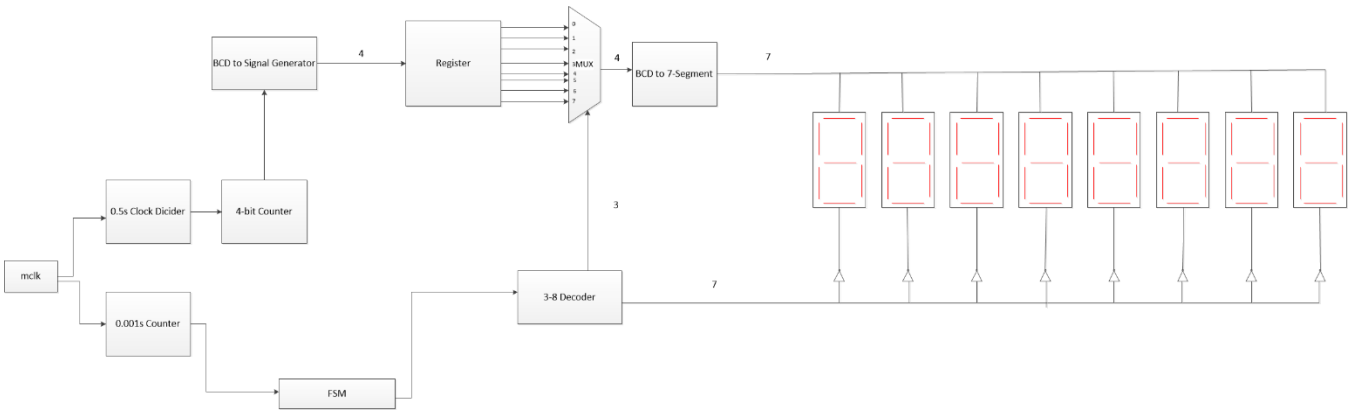

Figure 3. Top Level Design Flow Chart

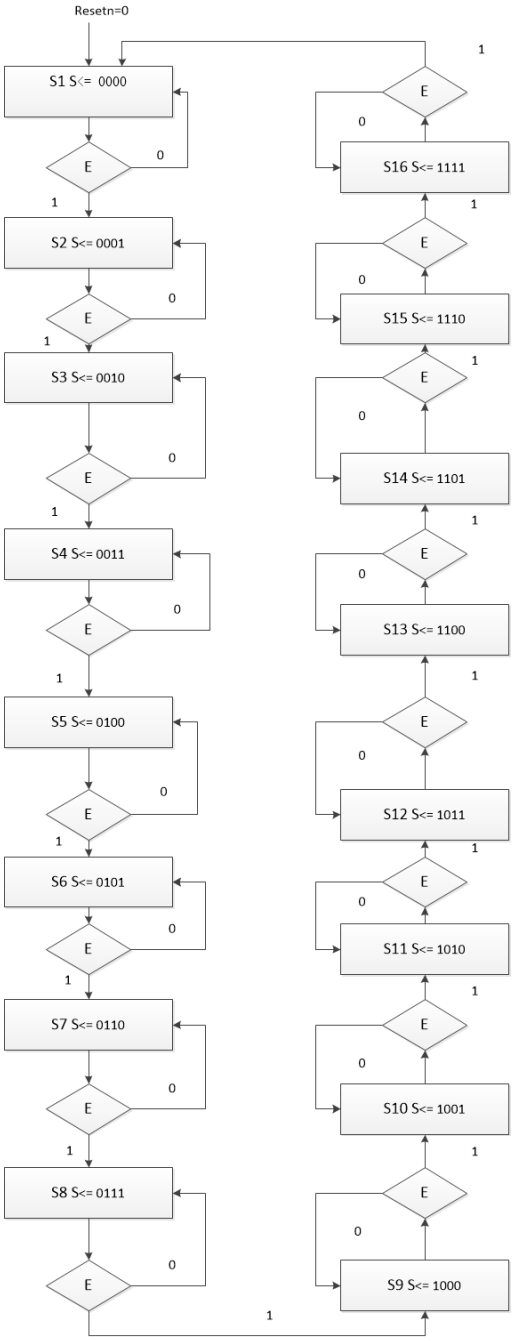

Figure 4. FSM Design