Smart Traffic Signal

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***Abstract*— Purpose of this technology is to build a traffic signal that adapts to the amount of traffic as to increase efficiency at roadway intersections. A main problem that has been observed is how to change the RGB LEDs along with counting cars at the light.**

I. Introduction

This project was pursued because we have observed a need for more efficient traffic signals and that our knowledge from class could be applied to solve such a problem. Knowledge from class was used in the design and construction processes.

A Finite State Machine (FSM) and Datapath design were first created in an attempt to understand key components necessary. Along the way, it was learned that revision is a main part of building the circuit and the VHDL modules. Much cooperative teamwork was established in order to revise the circuit and code.

The project was an overall success. The traffic light on the NEXSYS board shows that it is capable of breaking down large amounts of traffic. Hopefully, applications of this project can be used at intersections to determine the most efficient way to move traffic.

II. Methodology

A. Designing the Project

The team met several times to work on the project, starting with the design of the FSM and the Datapath, followed by meeting up to work on the VHDL modules that we knew would be needed for the project. During this time revisions and improvements were made to the design as issues that would prevent the project from functioning correctly were found.

When the team met to design the state machine, initially it was made with only two states, but it was later found that four states would be needed as the LEDs were not accounted for in the original design. The new Algorithmic State Machine Chart (ASM) can be observed in Figure 2.

B. Major Problems and Solutions

It was observed through the 7-segment display that the original up-down counters were not functioning together properly. After reaching "10" the counters became uncoordinated in various ways. The counters were eventually fixed simplifying the number of inputs and outputs, connecting their clocks to the car_counter, and allowing them to work independently of each other.

Another major problem occurred in the design phase of the project. The group believed that the Main FSM was capable of driving both the RGB LED and 7-segment display in the format we designed the data path. But it was soon found that it made better sense to make another FSM for the RGB LED and have it communicate with the Main FSM. This design worked perfectly and eventually led to the success of the project.

III. Experimental Setup

The software ISE Design Suite 14.7 is utilized to write the VHDL modules and test bench. A behavioral simulation is ran using this test bench to show that the 7-segment displays switch every millisecond. This is shown in Figure 4. Each one of the lights change at different time intervals, and these intervals were tested and verified using a stopwatch on a smart phone. Lastly, to test if this traffic signal truly helps breakdown large amounts of traffic the resetn button on the NEXSYS board resets the traffic light to Red; this allows traffic to pile up at the light. When the board is left untouched with much traffic buildup it is observed that the red light switches to green faster than normal. Therefore, the light effectively allows more cars through the light rather than allowing it to continue to pile up.

IV. Results

Figure 1 shows the data path and FSMs for the entire project, Figure 2 shows the ASM for the LEDs, our understanding of FSMs from class helped us understand how they worked and allowed us to design the ones needed for this project. In Figure 3, the ASM for the RGB LED is shown. Each state changes to the next depending on a specific time interval. In Figure 4, we can see the 1ms car counter working, the seven segment display can also be seen working as it increments up by one after 1.5ms, the LED is not shown because it would have to be simulated for 21s and the simulation time would be too long. The color change of the LED can be seen effectively in programming a NEXSYS board.

Conclusions

Our original design needed to be modified such that the up and down counters connected to the seven segment displays were independent of each other rather than connected. Each counter was connected to the same clock and

kept track of time differently, dependent on whether they were in the one's place or the ten's place. Therefore, the AND gate was removed from the design of the project. A couple of issues remain to be solved, the first being that the yellow light signal is represented by the LED turning blue. The project was left in this fashion due to simplicity, however it is possible to blend light from the two LEDs available on the NEXYS board in order to achieve a yellow light.

Another issue is the rate of speed at which traffic travelled through the stoplight. The project counts down in such a way that one car travels through the light every second, while in a real world scenario traffic would vary depending on the speed limit of the road. This would be possible to implement into the current project through the use of switches. The switches would represent different speed zones commonly seen in real world conditions and connect to the up and down counters. An extra state would have to be added to the RGB FSM checking the signals from the switches and causing the counter to count down more quickly.

Furthermore, it is possible to make the project representative of a full intersection rather than just one stoplight. In order to accomplish this, the group would have to essentially duplicate the current project and modify the added pieces to turn yellow and then red and count traffic up whenever the opposing light switched to green and traffic began counting down. Overall the project worked as designed and served to be a great application of the knowledge acquired throughout the course.

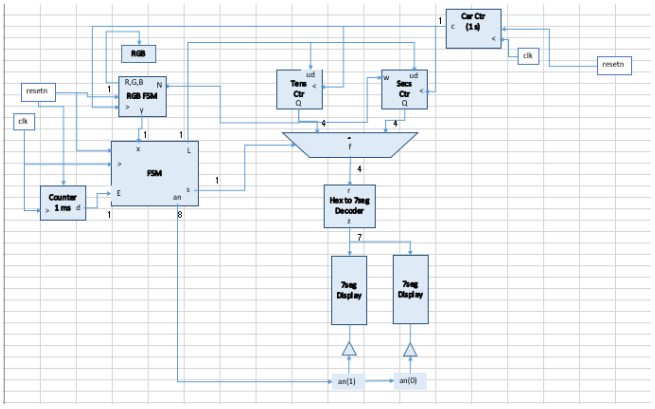

Figure 1: Current Datapath and FSM

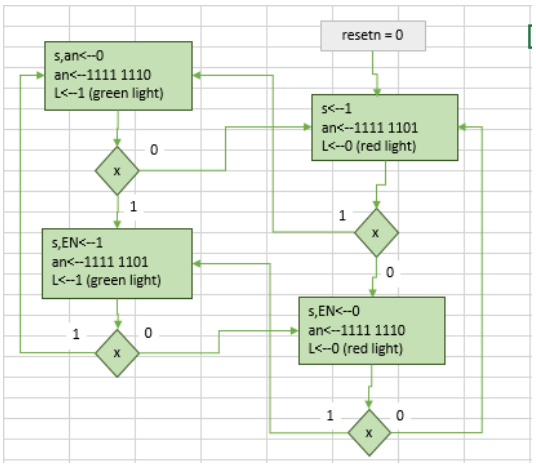

Figure 2:Main_FSM Algorithmic State Machine Chart

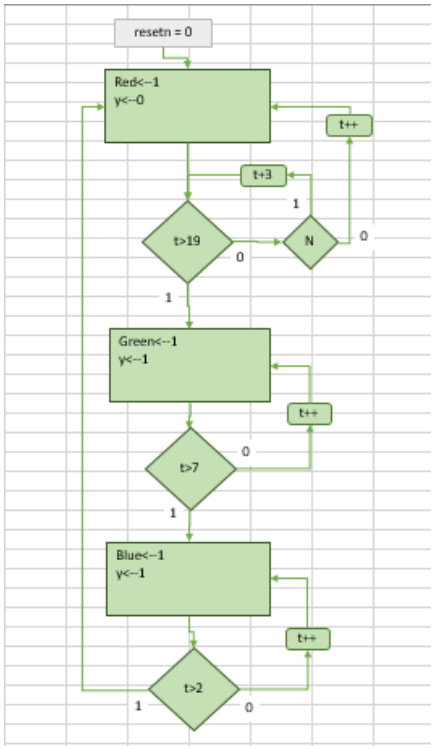

Figure 3: RGB_FSM Algorithmic State Machine Chart

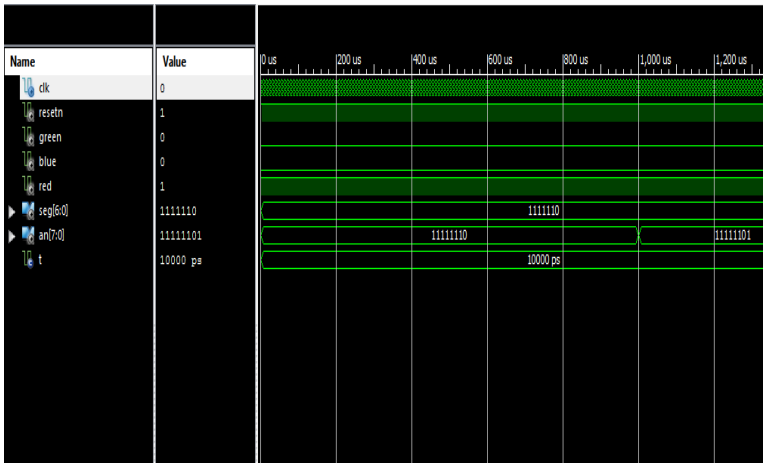

Figure 4: Behavioral Simulation