UART Communication

Separate Transmitting and Receiving Circuits

Presented by:

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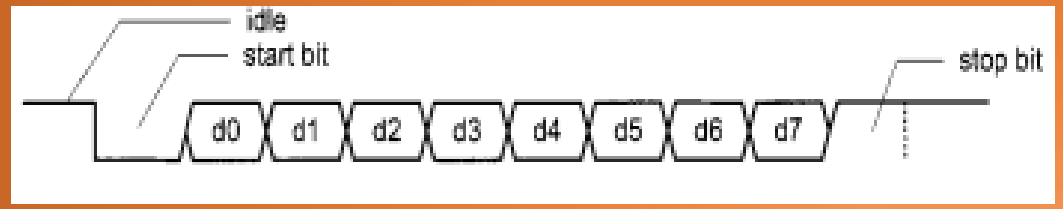
UART Communication

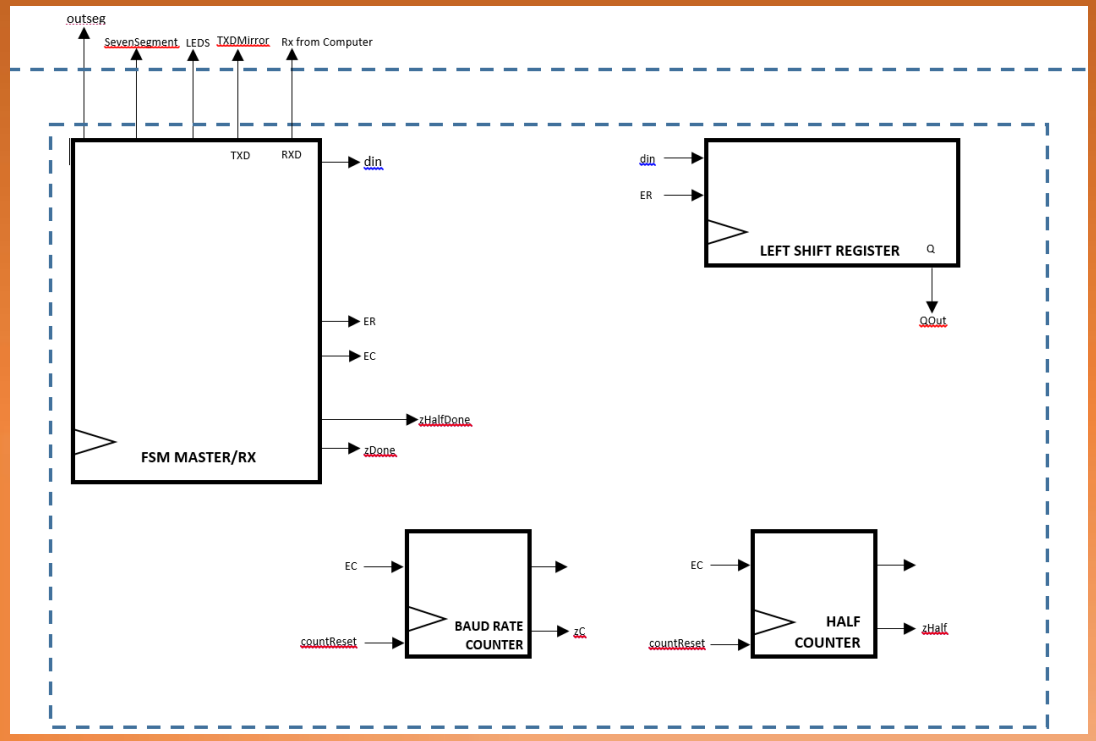
- UART (Universal Asynchronous Receiver and Transmitter) is a circuit that sends parallel data through a serial line.
- Data is usually sent in groups of 8 bits, making it ideal for ASCII communication
- Transmission of data is shown below:



- Because transmission is asynchronous, the two communicating circuits (Nexys board and computer) must agree on when data is being sent and received. The FT2232 handles this, and allows a user to select the baud rate. This project uses a baud rate of 9600 bauds.
- In order for communication to be read properly, the transmitter and receiver start sending and listening based on the idle state, start bit, and stop bit. So, each “word” contains 10 bits.

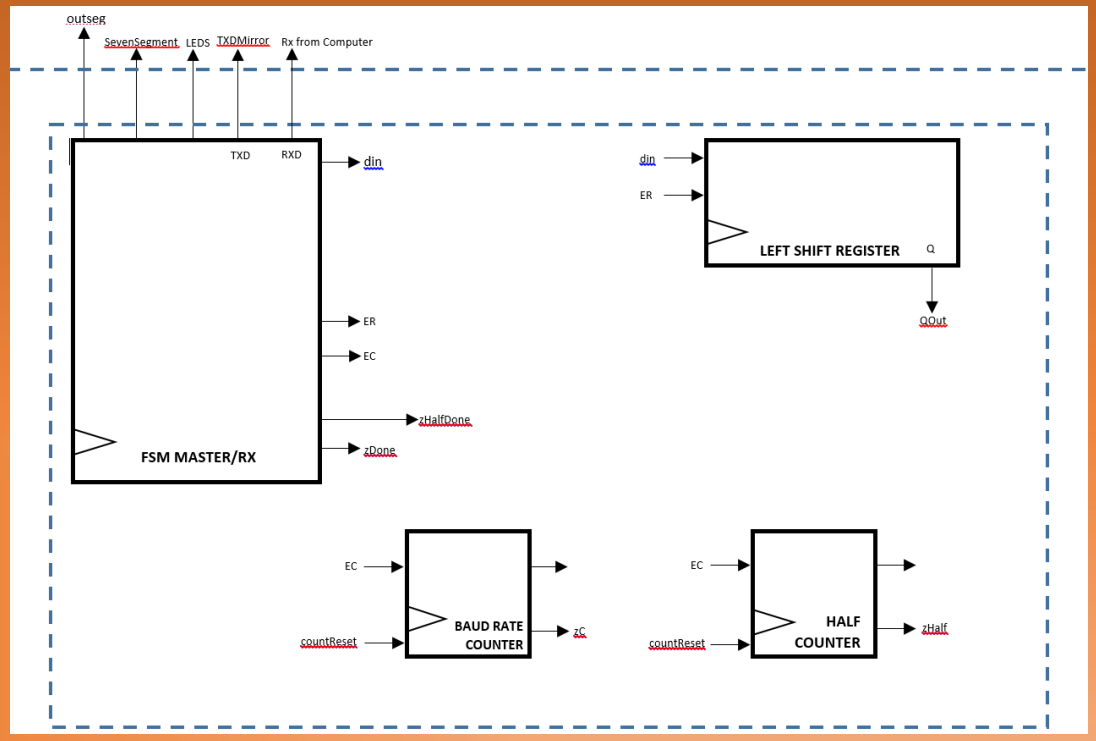
Receiving (Rx)

- The receiving circuit's structure consists of a **FSM**, **baud rate generator** (clock divider/counter circuit), **half counter**, and a **parallel access shift register.**
- **Baud Rate Generator**: Produces a pulse signal at 9600 Hz, equivalent to 9600 baud. Using a counter that counts to N = $\frac{1/9600}{10\ ns}$ = 10416, where 10 ns is equivalent to 100 MHz (the system clock), the counter circuit will produce a high when the counter reaches this number. This will determine the "length" of each bit, or how long the transmitted signal is high or low.



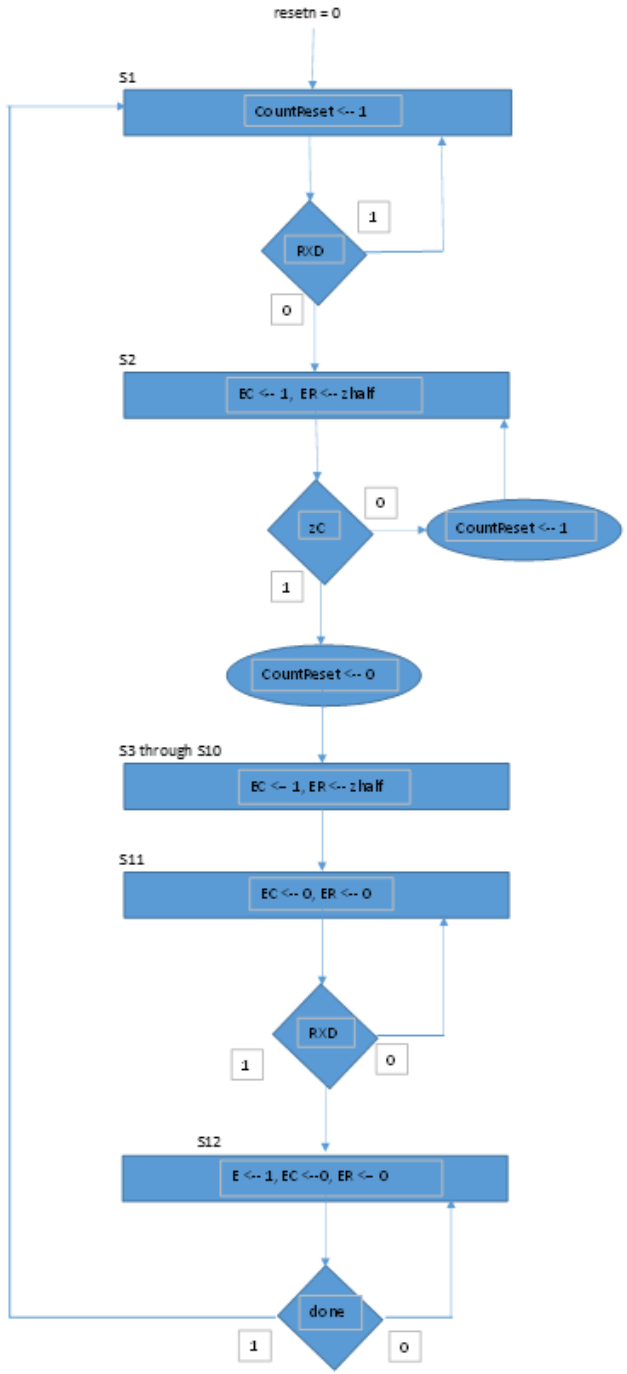
Receiving (Rx) cont.

- **Half Counter**: The half counter circuit operates like the baud rate counter, except it produces a high a little less than twice as fast as the baud rate counter. This samples near the middle of each received bit.
- **Parallel Access Shift Register**: This circuit receives the bits from the computer, loading the LSB first and MSB last, and stores them in registers to be read in parallel.



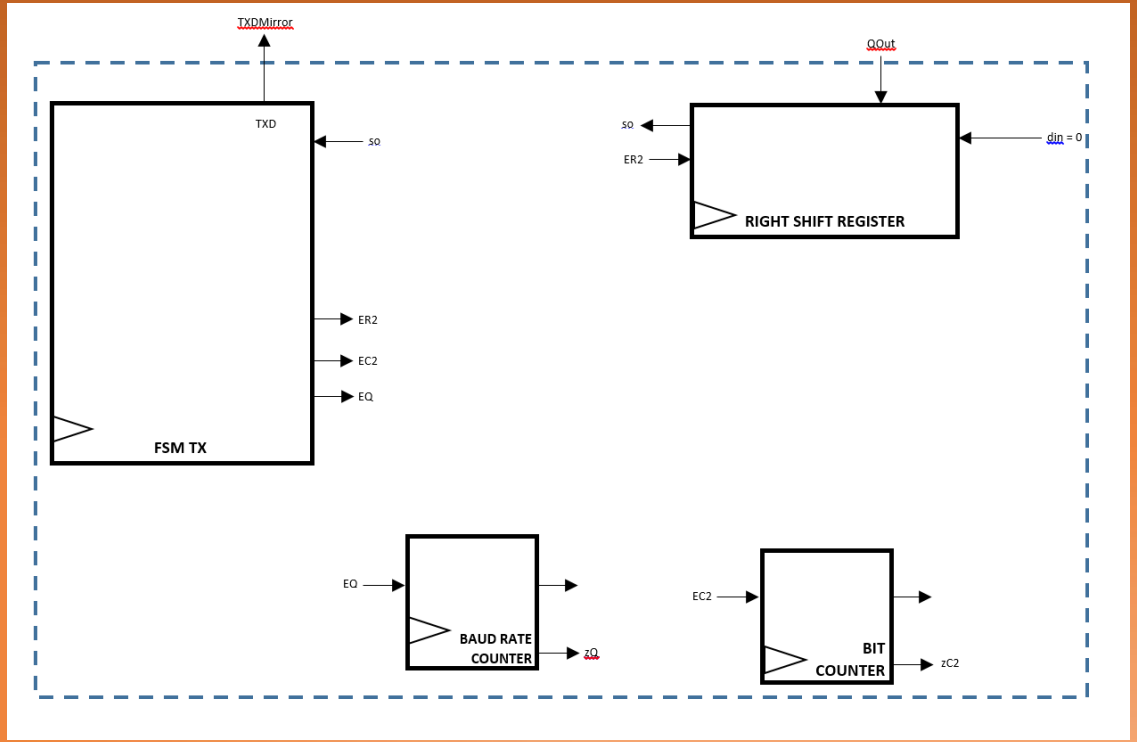
Receiving (Rx) cont.

- **FSM**: This circuit controls the process of receiving the serial information, as well as providing the clock and reset. The operation of this circuit can be seen through the ASM diagram on the right, and utilizes 12 states.



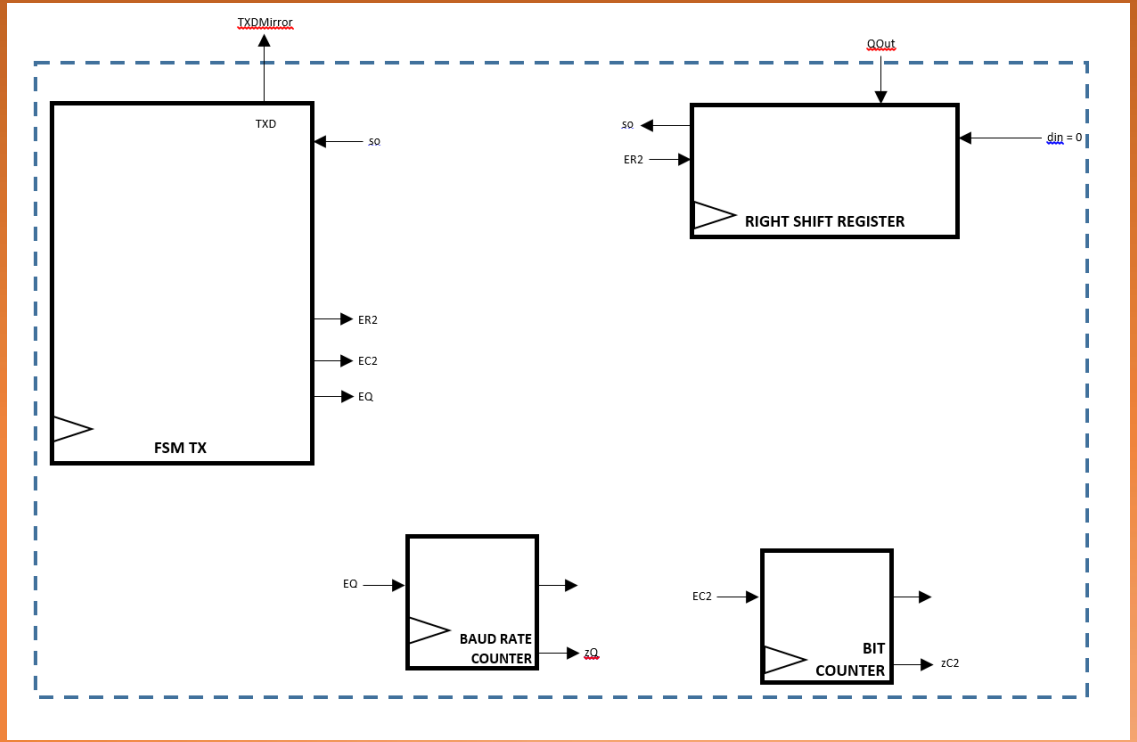
Transmitting (Tx)

- The transmitting circuit's structure consists of a **FSM**, **baud rate generator** (clock divider/counter circuit), **bit counter**, and a **Parallel Access Shift Register**.
- This circuit is similar to the Rx circuit, but it uses a bit counter instead of a half counter, the shift register loads in parallel and shifts serially, and the FSM operates differently



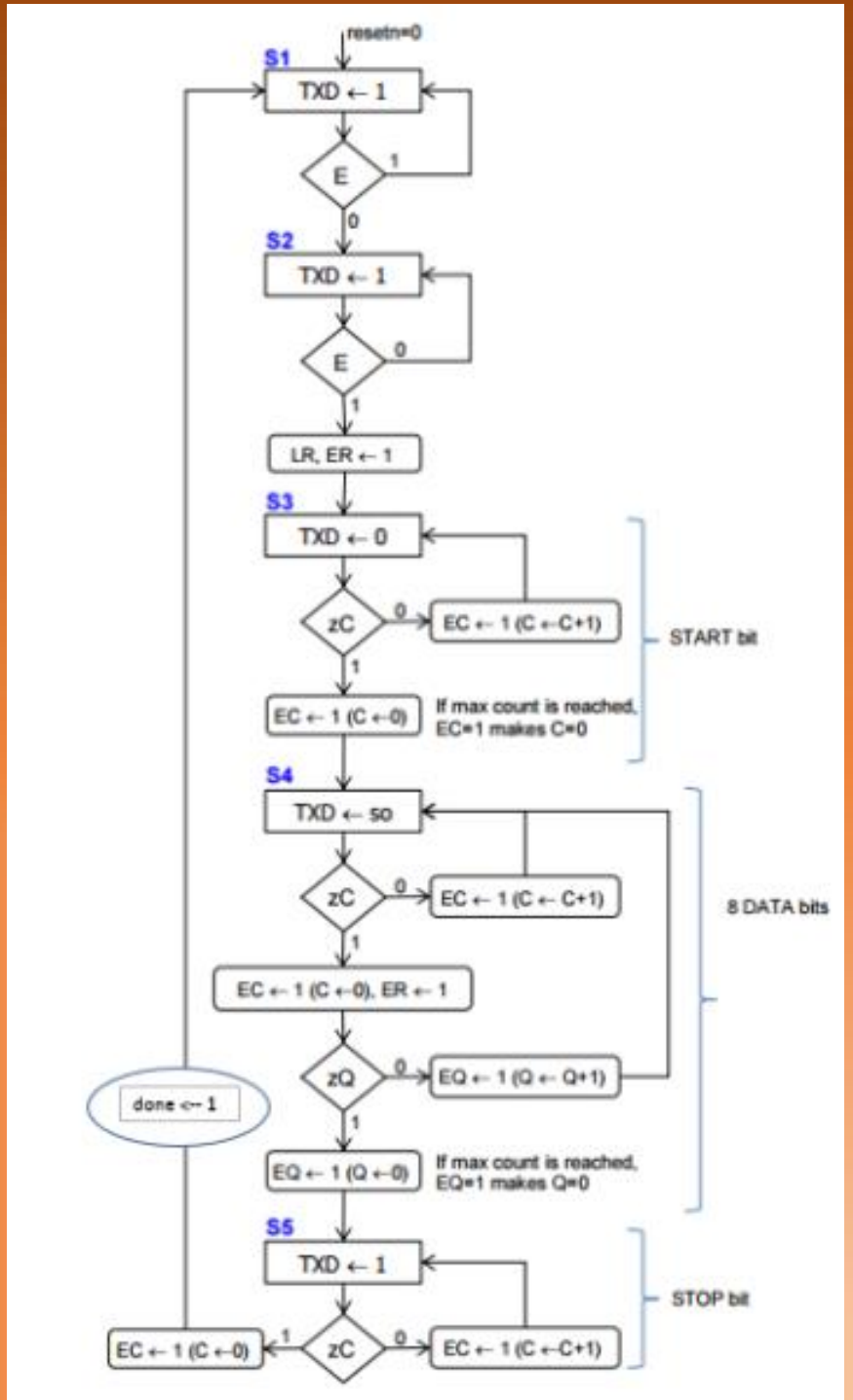
Transmitting (Tx) cont.

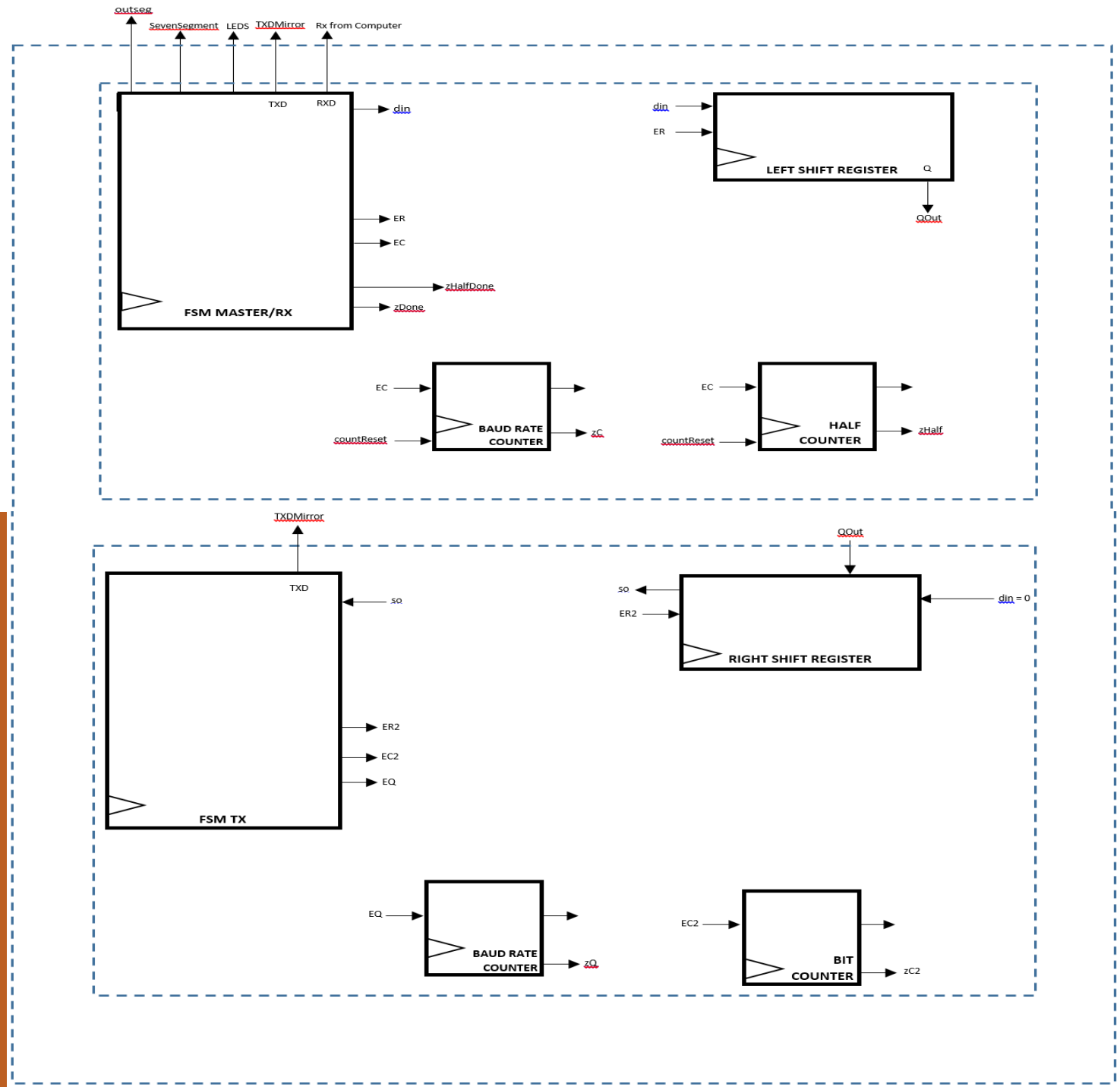
- **Bit Counter**: This circuit is a simple counter that outputs a high when its count reaches 7, and it is use to count the data bits in transmission. This tells the circuit when the transmission is over.
- **Parallel Access Shift Register**: The bits to be transmitted are loaded in parallel into this register, and then are serially shifted out, MSB first, to the computer.

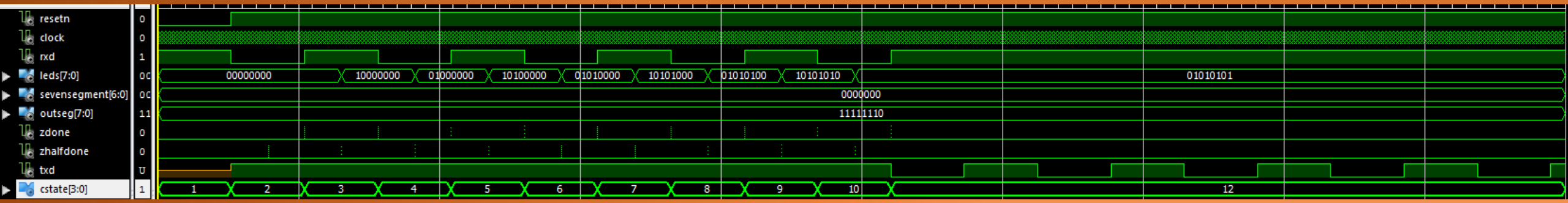


Transmission (Tx) cont.

- **FSM**: This circuit controls the process of transmitting the serial information, as well as providing the clock and reset. The operation of this circuit can be seen through the ASM diagram on the right, and utilizes 5 states.




outseg
SevenSegment
LEDS
TXDMirror
Rx from Computer
TXD
RXD
din
ER
EC
zHalfDone
zDone
FSM MASTER/RX
din
ER
LEFT SHIFT REGISTER
Q
QOut
EC
countReset
BAUD RATE COUNTER
zC
EC
countReset
HALF COUNTER
zHalf
TXDMirror
TXD
so
ER2
EC2
EQ
FSM TX
QOut
so
ER2
RIGHT SHIFT REGISTER
din = 0
EQ
BAUD RATE COUNTER
zQ
EC2
BIT COUNTER
zC2


resetn
clock
rxd
leds[7:0]
sevensegment[6:0]
outseg[7:0]
zdone
zhalfdone
txd
cstate[3:0]
00000000
10000000
01000000
10100000
01010000
10101000
01010100
10101010
01010101
0000000
11111110
1
2
3
4
5
6
7
8
9
10
12